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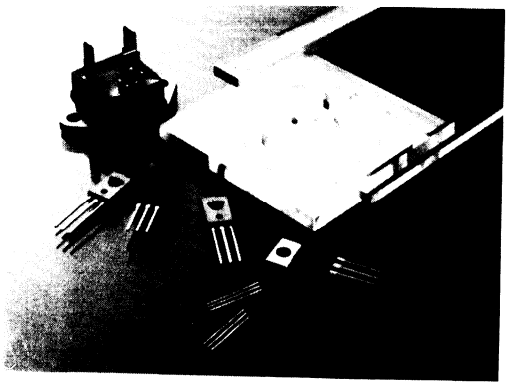
MOTOROLA Semiconductors

THYRISTOR DEVICE DATA



Theory and Applications (Chapters 1 thru 9) 1

Selector Guide 2

Data Sheets 3

Outline Dimensions and Leadform Options 4

Index and Cross Reference 5

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THYRISTOR DEVICE DATA

This manual is intended to give users of thyristors basic information on the product including applications, theory and data sheets on the broad line available from Motorola.

Motorola has a long history of supplying high quality thyristors in large volume to the power supply, industrial and lighting markets. Being the leading supplier of power devices in the world, we know how to serve the customers' needs.

The information in this book has been carefully checked and is believed to be accurate; however no responsibility is assumed for inaccuracies.

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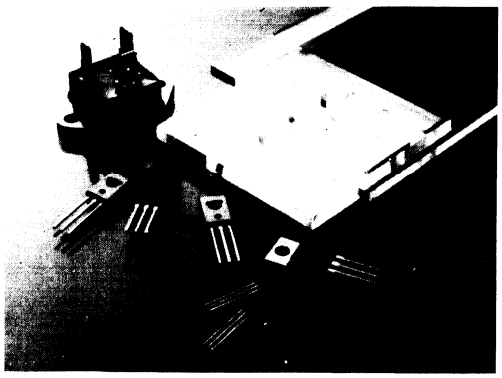


Theory and Applications (Chapters 1 thru 9)

1

	Page
Introduction	ii
Chapter 1: Symbols and Terminology	1-1-1
Chapter 2: Theory of Operation	1-2-1
Basic Behavior	1-2-1
Switching Characteristics	1-2-3
False Triggering	1-2-5
Theory of SCR Power Control	1-2-7
Triac Theory	1-2-13
Methods of Control	1-2-15
Zero Point Switching Techniques	1-2-16
Chapter 3: Thyristor Drivers and Trigger	1-3-1
Pulse Triggering of SCRs	1-3-1
Current Pulse Triggering	1-3-2
Capacitance Charge Triggering	1-3-4
Effects of Temperature	1-3-5
Reducing di/dt Effects	1-3-7
Snubbing a Thyristor	1-3-9
Protecting Sensitive Gate SCRs	1-3-11
Using Triac Drivers	1-3-14
Zero Cross vs Non-Zero Cross Triac Drivers	1-3-19
The Unijunction Transistor	1-3-21
Programmable Unijunction Transistors	1-3-30
Silicon Bilateral Switch	1-3-35
Chapter 4: New Thyristor Technologies	1-4-1
The SIDAC, A New High Voltage Bilateral Trigger	1-4-1
GTO Devices	1-4-11
Chapter 5: SCR Characteristics	1-5-1
SCR Turn-Off Time t_q	1-5-1
Parameters Affecting t_q	1-5-6
Characterizing SCRs for Crowbar Applications	1-5-11
Characterizing SCRs as Line-Type Modulators	1-5-19
Parallel Connected SCRs	1-5-24
RFI Suppression in Thyristor Circuits	1-5-28
Chapter 6: Applications	1-6-1
Phase Control with Thyristors	1-6-1
Motor Control	1-6-2
Phase Control with Trigger Devices	1-6-9
Cycle Control with Optically Isolated Triac Drivers	1-6-13
AC Power Control with Solid-State Relays	1-6-17
Triacs and Inductive Loads	1-6-20
Interfacing Digital Circuits to AC Loads	1-6-24
DC Motor Control with Thyristor Applications	1-6-33
Unijunction Transistor Applications	1-6-37
Heater Control	1-6-44
Light Dimmer	1-6-44
Voltage Regulation	1-6-46
Timer Circuits	1-6-47
Programmable Unijunction Transistor (PUT) Applications	1-6-48
VC Ramp Generator	1-6-48
Low Frequency Divider	1-6-49
Long Duration Timer	1-6-50
Phase Control	1-6-50
Voltage Regulator	1-6-51
Silicon Bilateral Switch (SBS) Applications	1-6-52
Lamp Dimmer	1-6-52
Electronic Crowbar	1-6-53
Triac Zero-Point Switch Applications	1-6-55
Temperature Control	1-6-56
Relay-Contact Protection	1-6-57
Chapter 7: Mounting Techniques for Thyristors	1-7-1
Surface Preparation	1-7-1
Thermal Compounds	1-7-2
Insulation Considerations	1-7-5
Fastening Techniques	1-7-7
Thermal System Evaluation	1-7-11
Chapter 8: Reliability and Quality	1-8-1
Thyristor Construction Through A Time Tested Design and Advanced Processing Methods	1-8-4
In-Process Controls and Inspections	1-8-4
Reliability Tests	1-8-5
Stress Testing — Power Cycling and Thermal Shock	1-8-6
Environmental Testing	1-8-8
Mechanical Testing	1-8-9
Chapter 9: Using Thyristor Die for Hybrid Assembly	1-9-1
Die Characteristics	1-9-1
Electrical Characteristics	1-9-1
Die Backing	1-9-2
Encapsulation	1-9-2
Handling and Shipping	1-9-2
Appendices	1-10-1

1

INTRODUCTION

Thyristors can take many forms, but they have certain things in common. All of them are solid state switches which act as open circuits capable of withstanding the rated voltage until triggered. When they are triggered, thyristors become low-impedance current paths and remain in that condition until the current either stops or drops below a minimum value called the holding level. Once a thyristor has been triggered, the trigger current can be removed without turning off the device.

Silicon controlled rectifiers (SCRs) and triacs are both members of the thyristor family. SCRs are unidirectional devices where triacs are bidirectional. An SCR is designed to switch load current in one direction, while a triac is designed to conduct load current in either direction.

Structurally, all thyristors consist of several alternating layers of opposite P and N silicon, with the exact structure varying with the particular kind of device. The load is applied across the multiple junctions and the trigger current is injected at one of them. The trigger current allows the load current to flow through the device, setting up a regenerative action which keeps the current flowing even after the trigger is removed.

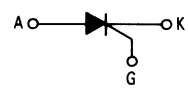
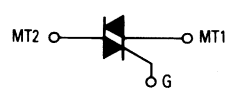
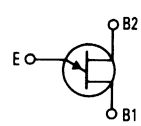
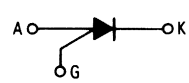
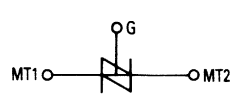
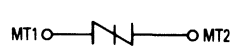
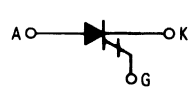
These characteristics make thyristors extremely useful in control applications. Compared to a mechanical switch, a thyristor has a very long service life and very fast turn on and turn off times. Because of their fast reaction times, regenerative action and low resistance once triggered, thyristors can be used as ac power controllers as well as simply turning devices on and off. Thyristors are used to control motors, incandescent lights and many other kinds of equipment.

Although thyristors of all sorts are generally fairly rugged, there are several points to keep in mind when designing circuits using them. One of the most important is to respect the devices' rated limits on rate of change of voltage and current (dv/dt and di/dt). If these are exceeded, the thyristor may be damaged or destroyed. On the other hand, it is important to provide a trigger pulse large enough and fast enough to turn the gate on quickly and completely. Usually the gate trigger current should be at least three times the minimum turn-on current with a pulse rise time of less than 1 microsecond and a pulse width greater than 10 microseconds. Thyristors may be driven in many different ways, including directly from transistors or logic families, by optoisolated triac drivers, unijunction transistors (UJTs), programmable unijunction transistors (PUTs) and silicon bilateral switches (SBSs). These and other design considerations are covered in this manual.

CHAPTER 1
SYMBOLS AND TERMINOLOGY

SYMBOLS

The following are the most commonly used schematic symbols for thyristors:

name of device	symbol
Silicon controlled rectifier (SCR)	
Triac	
Unijunction transistor (UJT)	
Programmable unijunction transistor (PUT)	
Silicon bilateral switch (SBS)	
Sidac	
Gate turn-off (GTO)	

THYRISTOR TERMINOLOGY

The following terms are used in SCR and TRIAC specifications:

RATINGS

These ratings are defined as maximum values. Exceeding these values can result in permanent damage or device failure.

Terminology	Symbol	Definition
	di/dt	The maximum rate of change of current the device will withstand.
FORWARD CURRENT RMS	$I_{T(RMS)}$	The maximum value of on-state rms current the device may conduct.
FORWARD PEAK GATE CURRENT	I_{GM}, I_{GFM}	The maximum gate current which may be applied to the device to cause conduction.
PEAK FORWARD SURGE CURRENT	I_{TSM}	The maximum allowable non-repetitive surge current the device will withstand at a specified pulse width.
AVERAGE ON-STATE CURRENT	$I_{T(AV)}$	The maximum average on-state current the device may conduct under stated conditions.
PEAK GATE POWER	P_{GM}	The maximum instantaneous value of gate power dissipation between gate and cathode terminal.
FORWARD AVERAGE GATE POWER	$P_{G(AV)}$	The maximum allowable value of gate power, averaged over a full cycle, that may be dissipated between the gate and cathode terminal.
CIRCUIT FUSING CONSIDERATIONS	I^2t	The maximum forward non-repetitive overcurrent capability. Usually specified for one-half cycle of 60 Hz operation.
PEAK GATE VOLTAGE	V_{GM}	The maximum peak value of voltage allowed between the gate and cathode terminal for any bias condition.
PEAK GATE VOLTAGE FORWARD	V_{FGM}, V_{GFM}	The maximum peak value of voltage allowed between the gate and cathode terminals with these terminals forward biased.
PEAK GATE VOLTAGE REVERSE	V_{RGM}, V_{GRM}	The maximum peak value of voltage allowed between the gate and cathode with these terminals reverse biased.
PEAK REPETITIVE FORWARD BLOCKING VOLTAGE (SCR)	V_{DRM}	The maximum allowed value of repetitive forward voltage which may be applied and not switch the SCR on.
PEAK REPETITIVE REVERSE BLOCKING VOLTAGE (SCR)	V_{RRM}	The maximum allowed value of repetitive reverse voltage which may be applied to the anode terminal.
PEAK REPETITIVE OFF-STATE VOLTAGE (TRIAC)	V_{DRM}	The maximum allowed value of repetitive off-state voltage which may be applied and not switch on the triac.

CHARACTERISTICS

Terminology	Symbol	Definition
PEAK FORWARD BLOCKING CURRENT (SCR)	I_{DRM}	The maximum value of current which will flow at V_{DRM} and specified temperature.
PEAK REVERSE BLOCKING CURRENT (SCR)	I_{RRM}	The maximum value of current which will flow at V_{RRM} and specified temperature.
PEAK BLOCKING CURRENT (TRIAC)	I_{DRM}	The maximum value of current which will flow for either polarity of V_{DRM} and at specified temperature.
PEAK ON-STATE VOLTAGE	V_{TM}	The maximum voltage drop across the terminals at stated conditions.
GATE TRIGGER CURRENT	I_{GT}	The maximum value of gate current required to switch the device from the off state to the on state under specified conditions.
GATE TRIGGER VOLTAGE	V_{GT}	The gate dc voltage required to produce the gate trigger current.
HOLDING CURRENT	I_H	The value of forward anode current which allows the device to remain in conduction. Below this value the device will return to a forward blocking state at prescribed gate conditions.
CRITICAL RISE OF OFF-STATE VOLTAGE	dv/dt	The minimum value of the rate of rise of forward voltage which will cause switching from the off state to the on state.
TURN-ON TIME (SCR)	t_{gt}	The time interval between a specified point at the beginning of the gate pulse and the instant when the device voltage (current) has dropped to a specified low value during the switching of an SCR from the off state to the on state by a gate pulse.
TURN-OFF TIME (SCR)	t_q	The time interval between the instant when the SCR current has decreased to zero after external switching of the SCR voltage circuit and the instant when the thyristor is capable of supporting a specified wave form without turning on.
OPERATING JUNCTION TEMPERATURE	T_J	The junction temperature of the device as a result of ambient and load conditions.
STORAGE TEMPERATURE	T_{stg}	The temperature at which the device may be stored without harm.
CASE TEMPERATURE	T_C	The temperature of the device case under specified conditions.
AMBIENT TEMPERATURE	T_A	The air temperature measured below a device in an environment of substantially uniform temperature, cooled only by natural air currents and not materially affected by radiant and reflective surfaces.

CHARACTERISTICS

Terminology	Symbol	Definition
THERMAL RESISTANCE, CASE-TO-AMBIENT	$R_{\theta CA}$	The thermal resistance (steady-state) from the device case to the ambient.
THERMAL RESISTANCE, JUNCTION-TO-AMBIENT	$R_{\theta JA}$	The thermal resistance (steady-state) from the semiconductor junction(s) to the ambient.
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R_{\theta JC}$	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the case.
THERMAL RESISTANCE, JUNCTION-TO-MOUNTING SURFACE	$R_{\theta JM}$	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the mounting surface.
TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-AMBIENT	$Z_{\theta JA(t)}$	The transient thermal impedance from the semiconductor junction(s) to the ambient.
TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE	$Z_{\theta JC(t)}$	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

Unijunction Transistor Nomenclature

Symbol	Definition
I_E	Emitter current.
I_{EO} (I_{EB2O})	Emitter reverse current. Measured between emitter and base-two at a specified voltage, and base-one open-circuit.
I_p	Peak point emitter current. The maximum emitter current that can flow without allowing the UJT to go into the negative resistance region. Peak point is the lowest current on the emitter characteristic where: $\frac{dV_{EB1}}{dI_E} = 0$
I_V	Valley point emitter current. The current flowing in the emitter when the device is biased to the valley point. Valley point is the second lowest current on the emitter characteristic where: $\frac{dV_{EB1}}{dI_E} = 0$
r_{BB}	Interbase resistance. Resistance between base-two and base-one measured at a specified interbase voltage.
V_{B2B1}	Voltage between base-two and base-one. Also called interbase voltage.
V_p	Peak point emitter voltage. The maximum voltage seen at the emitter before the UJT goes into the negative resistance region.
V_D	Forward voltage drop of the emitter junction. Also called $V_{F(EB1)}$ or V_F.
V_{EB1}	Emitter to base-one voltage.
$V_{EB1(sat)}$	Emitter saturation voltage. Forward voltage drop from emitter to base-one at a specified emitter current larger than I_V and specified interbase voltage.
V_V	Valley point emitter voltage. The voltage at which the valley point occurs with a specified V_{B2B1}.
V_{OB1}	Base-one peak voltage. The peak voltage measured across a resistor in series with base-one when the unijunction transistor is operated as a relaxation oscillator in a specified circuit.
η	Intrinsic standoff ratio. Defined by the relationship: $\eta = \frac{V_p - V_D}{V_{B2B1}}$
α_{rBB}	Interbase resistance temperature coefficient. Variation of resistance between B2 and B1 over the specified temperature range and measured at the specific interbase voltage and temperature with emitter open-circuited.
$I_{B2\ (mod)}$	Interbase modulation current. B2 current modulation due to firing. Measured at a specified interbase voltage, emitter current and temperature.

1

CHAPTER 2
THEORY OF THYRISTOR OPERATIONS

To successfully apply thyristors, an understanding of their characteristics, ratings, and limitations is imperative. In this chapter, significant thyristor characteristics, the basis of their ratings, and their relationship to circuit design are discussed.

Several different kinds of thyristors are shown in Table 2.1. Silicon Controlled Rectifiers (SCRs) are the most widely used as power control elements; triacs are quite popular in lower current (under 40 A) ac power applications. Diacs, SUSs and SBSs are most commonly used as gate trigger devices for the power control elements.

Table 2.I. Thyristor Types

*JEDEC Titles	Popular Names, Types
Reverse Blocking Diode Thyristor	†Four Layer Diode, Silicon Unilateral Switch (SUS)
Reverse Blocking Triode Thyristor	Silicon Controlled Rectifier (SCR)
Reverse Conducting Diode Thyristor	†Reverse Conducting Four Layer Diode
Reverse Conducting Triode Thyristor	Reverse Conducting SCR
Bidirectional Triode Thyristor	Triac
Turn-Off Thyristor	Gate Turn Off Switch (GTO)

*JEDEC is an acronym for the Joint Electron Device Engineering Councils, an industry standardization activity co-sponsored by the Electronic Industries Association (EIA) and the National Electrical Manufacturers Association (NEMA).

†Not generally available.

Before considering thyristor characteristics in detail, a brief review of their operation based upon the common two-transistor analogy of an SCR is in order.

BASIC BEHAVIOR

The bistable action of thyristors is readily explained by analysis of the structure of an SCR. This analysis is essentially the same for any operating quadrant of triac because a triac may be considered as two parallel SCRs oriented in opposite directions. Figure 2.1(a) shows the schematic symbol for an SCR, and Figure 2.1(b) shows the P-N-P-N structure the symbol represents. In the two-transistor model for the SCR shown in Figure 2.1(c), the interconnections of the two transistors are such that regenerative action occurs. Observe that if current is injected into any leg of the model, the gain of the transistors (if sufficiently high) causes this current to be amplified in another leg. In order for regeneration to occur, it is necessary for the sum of the common base current gains (α) of the two transistors to exceed unity. Therefore, because the junction leakage currents are relatively small and current gain is designed to be low at the leakage current level, the PNPN device remains off unless external current is applied. When sufficient trigger current is applied (to the gate, for example, in the case of an SCR) to raise the loop gain to unity, regeneration occurs and the on-state principal current is limited primarily by external circuit impedance. If the initiating trigger current is removed, the thyristor remains in the on state, providing the current level is high enough to meet the unity gain criteria. This critical current is called latching current.

In order to turn off a thyristor, some change in current must occur to reduce the loop gain below unity. From the model, it appears that shorting the gate to cathode would accomplish this. However in an actual SCR structure, the gate area is only a fraction of the cathode area and very little current is diverted by the short. In practice, the principal current must be reduced below a certain level, called holding current, before gain falls below unity and turn-off may commence.

In fabricating practical SCRs and Triacs, a "shorted emitter" design is generally used in which, schematically, a resistor is added from gate to cathode or gate to MT1. Because current is diverted from the N-base through the resistor, the gate trigger current, latching current and holding current all increase. One of the principal reasons for the shunt resistance is to improve dynamic performance at high temperatures. Without the shunt, leakage current on most high current thyristors could initiate turn-on at high temperatures.

Sensitive gate thyristors employ a high resistance shunt or none at all; consequently, their characteristics can be altered dramatically by use of an external resistance. An external resistance has a minor effect on most shorted emitter designs.

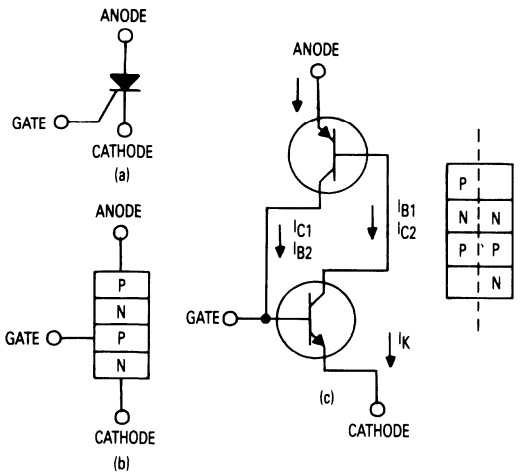


Figure 2.1. Two-transistor analogy of an SCR: (a) schematic symbol of SCR; (b) P-N-P-N structure represented by schematic symbol; (c) two-transistor model of SCR.

Junction temperature is the primary variable affecting thyristor characteristics. Increased temperatures make the thyristor easier to turn on and keep on. Consequently, circuit conditions which determine turn-on must be designed to operate at the lowest anticipated junction temperatures, while circuit conditions which are to turn off the thyristor or prevent false triggering must be designed to operate at the maximum junction temperature.

Thyristor specifications are usually written with case temperatures specified and with electrical conditions such that the power dissipation is low enough that the junction temperature essentially equals the case temperature. It is incumbent upon the user to properly account for changes in characteristics caused by the circuit operating conditions different from the test conditions.

TRIGGERING CHARACTERISTICS

Turn-on of a thyristor requires injection of current to raise the loop gain to unity. The current can take the form of current applied to the gate, an anode current resulting from leakage, or avalanche breakdown of a blocking junction. As a result, the breakover voltage of a thyristor can be varied or controlled by injection of a current at the gate terminal. Figure 2.2 shows the interaction of gate current and voltage for an SCR.

When the gate current I_g is zero, the applied voltage must reach the breakover voltage of the SCR before switching occurs. As the value of gate current is increased, however, the ability of a thyristor to support applied voltage is reduced and there is a certain value of gate current at which the behavior of the thyristor closely resembles that of a rectifier. Because thyristor turn-on, as a result of exceeding the breakover voltage, can produce high instantaneous power dissipation nonuniformly distributed over the die area during the switching transition, extreme temperatures resulting in die failure may occur unless the magnitude and rate of rise of principal current (di/dt) is restricted to tolerable levels. For normal operation, therefore, SCRs and triacs are operated at applied voltages lower than the breakover voltage, and are made to switch to the on state by gate signals high enough to assure complete turn-on

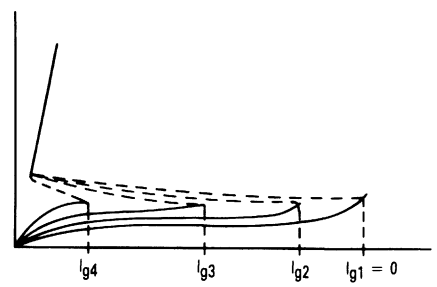


Figure 2.2. Thyristor Characteristics Illustrating Breakover as a Function of Gate Current

independent of the applied voltage. On the other hand, diacs and other thyristor trigger devices are designed to be triggered by anode breakover. Nevertheless they also have di/dt and peak current limits which must be adhered to.

A triac works the same general way for both positive and negative voltage. However since a triac can be switched on by either polarity of the gate signal regardless of the voltage polarity across the main terminals, the situation is somewhat more complex than for an SCR.

The various combinations of gate and main terminal polarities are shown in Figure 2.3. The relative sensitivity depends on the physical structure of a particular triac,

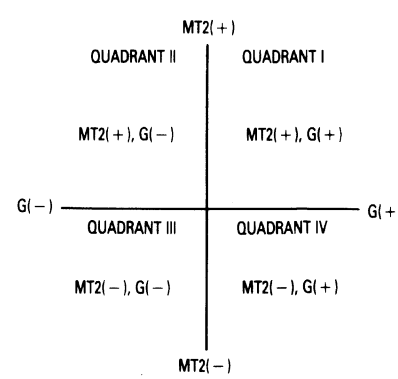


Figure 2.3. Quadrant Definitions for a Triac

but as a rule, sensitivity is highest in quadrant I and quadrant IV is generally considerably less sensitive than the others.

Gate sensitivity of a triac as a function of temperature is shown in Figure 2.4.

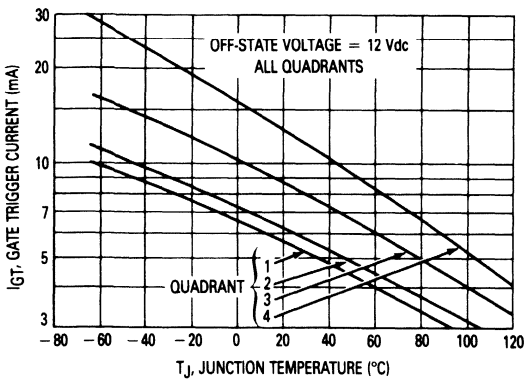


Figure 2.4. Typical Triac Triggering Sensitivity in the Four Trigger Quadrants

Since both the junction leakage currents and the current gain of the "transistor" elements increase with temperature, the magnitude of the required gate trigger current decreases as temperature increases. The gate — which can be regarded as a diode — exhibits a decreasing voltage drop as temperature increases. Thus it is important that the gate trigger circuit be designed to deliver sufficient current to the gate at the lowest anticipated temperature.

It is also advisable to observe the maximum gate current, as well as peak and average power dissipation ratings. Also in the negative direction, the maximum gate ratings should be observed. Both positive and negative gate limits are often given on the data sheets and they may indicate that protective devices such as voltage clamps and current limiters may be required in some applications. It is generally inadvisable to dissipate power in the reverse direction.

Although the criteria for turn-on have been described in terms of current, it is more basic to consider the thyristor as being charge controlled. Accordingly, as the duration of the trigger pulse is reduced, its amplitude must be correspondingly increased. Figure 2.5 shows typical behavior at various pulse widths and temperatures.

The gate pulse width required to trigger a thyristor also depends upon the time required for the anode current to reach the latching value. It may be necessary to maintain a gate signal throughout the conduction period in applications where the load is highly inductive or where the anode current may swing below the holding value within the conduction period.

When triggering an SCR with a dc current, excess leakage in the reverse direction normally occurs if the trigger signal is maintained during the reverse blocking phase of the anode voltage. This happens because the SCR operates like a remote base transistor having a gain which is generally about 0.5. When high gate drive currents are used, substantial dissipation could occur in the SCR or a significant current could flow in the load; therefore, some means usually must be provided to remove the gate signal during the reverse blocking phase.

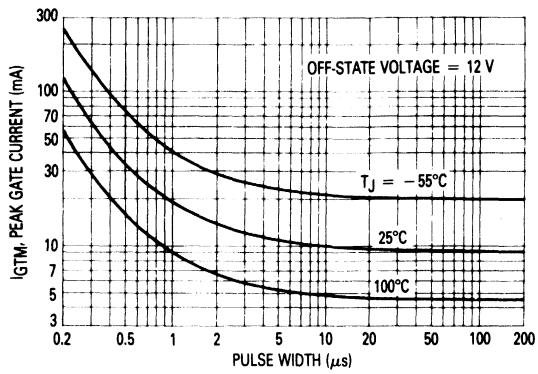


Figure 2.5. Typical Behavior of Gate Trigger Current as Pulse Width and Temperature Are Varied

LATCH AND HOLD CHARACTERISTICS

In order for the thyristor to remain in the on state when the trigger signal is removed, it is necessary to have sufficient principal current flowing to raise the loop gain to unity. The principal current level required is the latching current, I_L. Although triacs show some dependency on the gate current in quadrant II, the latching current is primarily affected by the temperature on shorted emitter structures.

In order to allow turn off, the principal current must be reduced below the level of the latching current. The current level where turn off occurs is called the holding current, I_H. Like the latching current, the holding current is affected by temperature and also depends on the gate impedance.

Reverse voltage on the gate of an SCR markedly increases the latch and hold levels. Forward bias on thyristor gates may significantly lower from the values shown in the data sheets since those values are normally given with the gate open. Failure to take this into account can cause latch or hold problems when thyristors are being driven from transistors whose saturation voltages are a few tenths of a volt.

Thyristors made with shorted emitter gates are obviously not as sensitive to the gate circuit conditions as devices which have no built-in shunt.

SWITCHING CHARACTERISTICS

When triacs or SCRs are triggered by a gate signal, the turn-on time consists of two stages: a delay time, t_d, and a rise time, t_r, as shown in Figure 2.6. The total gate controlled turn-on time, t_{gt}, is usually defined as the time interval between the 50 percent point of the leading edge

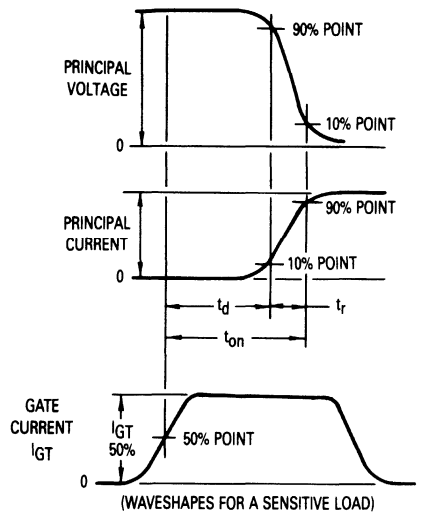


Figure 2.6. Waveshapes Illustrating Thyristor Turn-On Time For A Resistive Load

of the gate trigger voltage and 90 percent point of the principal current. The rise time t_r is the time interval required for the principal current to rise from 10 to 90 percent of its maximum value. A resistive load is usually specified.

Delay time decreases slightly as the peak off-state voltage increases. It is primarily related to the magnitude of the gate-trigger current and shows a relationship which is roughly inversely proportional.

The rise time is influenced primarily by the off-state voltage, as high voltage causes an increase in regenerative gain. Of major importance in the rise time interval is the relationship between principal voltage and current flow through the thyristor di/dt. During this time the dynamic voltage drop is high and the current density due to the possible rapid rate of change can produce localized hot spots in the die. This may permanently degrade the blocking characteristics. Therefore, it is important that power dissipation during turn-on be restricted to safe levels.

Turn-off time is a property associated only with SCRs and other unidirectional devices. (In triacs or bidirectional devices a reverse voltage cannot be used to provide circuit-commutated turn-off voltage because a reverse voltage applied to one half of the structure would be a forward-bias voltage to the other half.) For turn-off times in SCRs, the recovery period consists of two stages, a reverse recovery time and a gate or forward blocking recovery time, as shown in Figure 2.7.

When the forward current of an SCR is reduced to zero at the end of a conduction period, application of reverse voltage between the anode and cathode terminals causes reverse current flow in the SCR. The current persists until the time that the reverse current decreases to the leakage level. Reverse recovery time (t_{rr}) is usually measured from the point where the principal current changes polarity to a specified point on the reverse current waveform as indicated in Figure 2.7. During this period the anode and cathode junctions are being swept free of charge so that they may support reverse voltage. A second recovery period, called the gate recovery time, t_{gr}, must elapse for the charge stored in the forward-blocking junction to recombine so that forward-blocking voltage can be reapplied and successfully blocked by the SCR. The gate recovery time of an SCR is usually much longer than the reverse recovery time. The total time from the instant reverse recovery current begins to flow to the start of the forward-blocking voltage is referred to as circuit-commutated turn-off time t_q.

Turn-off time depends upon a number of circuit conditions including on-state current prior to turn-off, rate of change of current during the forward-to-reverse transition, reverse-blocking voltage, rate of change of reapplied forward voltage, the gate bias, and junction temperature. Increasing junction temperature and on-state current both increase turn-off time and have a more significant effect than any of the other factors. Negative gate bias will decrease the turn-off time.

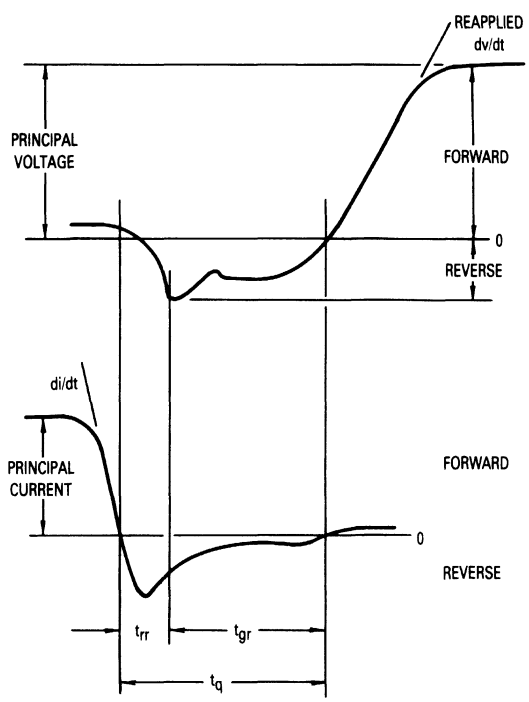


Figure 2.7. Waveshapes Illustrating Thyristor Turn-Off Time

For applications in which an SCR is used to control ac power, during the entire negative half of the sine wave a reverse voltage is applied. Turn off is easily accomplished for most devices at frequencies up to a few kilohertz. For applications in which the SCR is used to control the output of a full-wave rectifier bridge, however, there is no reverse voltage available for turn-off, and complete turn-off can be accomplished only if the bridge output is reduced close to zero such that the principal current is reduced to a value lower than the device holding current for a sufficiently long time. Turn-off problems may occur even at a frequency of 60 Hz particularly if an inductive load is being controlled.

In triacs, rapid application of a reverse polarity voltage does not cause turn-off because the main blocking junctions are common to both halves of the device. When the first triac structure (SCR-1) is in the conducting state, a quantity of charge accumulates in the N-type region as a result of the principal current flow. As the principal current crosses the zero reference point, a reverse current is established as a result of the charge remaining in the N-type region, which is common to both halves of the device. Consequently, the reverse recovery current becomes a forward current to the second half of the triac. The current resulting from stored charge causes the second half of the triac to go into the conducting state in the absence of a gate signal. Once current conduction has been established by application of a gate signal, therefore, complete loss in power control can occur as a result of interaction within the N-type base region of the triac unless sufficient time elapses or the rate of application of the reverse polarity voltage is slow enough to allow nearly all the charge to recombine in the common N-type region. Therefore, triacs are generally limited to low-frequency – 60 Hz applications. Turn-off or commutation of triacs is more severe with inductive loads than with resistive loads because of the phase lag between voltage and current associated with inductive loads. Figure 2.8 shows the waveforms for an inductive load with lagging current power factor. At the time the current reaches zero crossover (Point A), the half of the triac in conduction begins to commutate when the principal current falls below the holding current. At the instant the conducting half of the triac turns off, an applied voltage opposite the current polarity is applied across the triac terminals (Point B). Because this voltage is a forward bias to the second half of the triac, the suddenly reapplied voltage in conjunction with the remaining stored charge in the high-voltage junction reduces the over-all device capability to support voltage. The result is a loss of power control to the load, and the device remains in the conducting state in absence of a gate signal. The measure of triac turn-off ability is the rate of rise of the opposite polarity voltage it can handle without remaining on. It is called commutating dv/dt (dv/dt[c]). Circuit conditions and temperature affect dv/dt(c) in a manner similar to the way t_q is affected in an SCR.

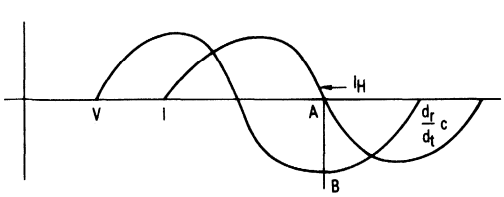


Figure 2.8. Inductive Load Waveforms

It is imperative that some means be provided to restrict the rate of rise of reapplied voltage to a value which will permit triac turn-off under the conditions of inductive load. A commonly accepted method for keeping the commutating dv/dt within tolerable levels is to use an RC snubber network in parallel with the main terminals of the triac. Because the rate of rise of applied voltage at the triac terminal is a function of the load impedance and the RC snubber network, the circuit can be evaluated under worst-case conditions of operating case temperature and maximum principal current. The values of resistance and capacitance in the snubber are then adjusted so that the rate of rise of commutating dv/dt stress is within the specified minimum limit under any of the conditions mentioned above. The value of snubber resistance should be high enough to limit the snubber capacitance discharge currents during turn-on and dampen the LC oscillation during commutation. The combination of snubber values having highest resistance and lowest capacitance that provides satisfactory operation is generally preferred.

FALSE TRIGGERING

Circuit conditions can cause thyristors to turn on in the absence of the trigger signal. False triggering may result from:

1) A high rate of rise of anode voltage, (the dv/dt effect).
2) Transient voltages causing anode breakover.
3) Spurious gate signals.

Static dv/dt effect: When a source voltage is suddenly applied to a thyristor which is in the off state, it may switch from the off state to the conducting state. If the thyristor is controlling alternating voltage, false turn-on resulting from a transient imposed voltage is limited to no more than one-half cycle of the applied voltage because turn-off occurs during the zero current crossing. However, if the principal voltage is dc voltage, the transient may cause switching to the on state and turn-off could then be achieved only by a circuit interruption.

The switching from the off state caused by a rapid rate of rise of anode voltage is the result of the internal capacitance of the thyristor. A voltage wavefront impressed across the terminals of a thyristor causes a capacitance-charging current to flow through the device which is a function of the rate of rise of applied off-state voltage ($i = C\,dv/dt$). If the rate of rise of voltage exceeds a critical value, the capacitance charging current exceeds the gate triggering current and causes device turn-on. Operation

at elevated junction temperatures reduces the thyristor ability to support a steep rising voltage dv/dt because of increased sensitivity.

dv/dt ability can be improved quite markedly in sensitive gate devices and to some extent in shorted emitter designs by a resistance from gate to cathode (or MT1) however reverse bias voltage is even more effective in an SCR. More commonly, a snubber network is used to keep the dv/dt within the limits of the thyristor when the gate is open.

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TRANSIENT VOLTAGES: — Voltage transients which occur in electrical systems as a result of disturbance on the ac line caused by various sources such as energizing transformers, load switching, solenoid closure, contractors and the like may generate voltages which are above the ratings of thyristors. Thyristors, in general, switch from the off state to the on state whenever the breakover voltage of the device is exceeded, and energy is then transferred to the load. However, unless a thyristor is specified for use in a breakover mode, care should be exercised to ensure that breakover does not occur, as some devices may incur surface damage with a resultant degradation of blocking characteristics. It is good practice when thyristors are exposed to a heavy transient environment to provide some form of transient suppression.

For applications in which low-energy, long-duration transients may be encountered, it is advisable to use thyristors that have voltage ratings greater than the highest voltage transient expected in the system. The use of voltage clipping cells (MOV or Zener) is also an effective method to hold transient below thyristor ratings. The use of an RC "snubber" circuit is effective in reducing the effects of the high-energy short-duration transients more frequently encountered. The snubber is commonly required to prevent the static dv/dt limits from being exceeded, and often may be satisfactory in limiting the amplitude of the voltage transients as well.

For all applications, the dv/dt limits may not be exceeded. This is the minimum value of the rate of rise off-state voltage applied immediately to the MT1-MT2 terminals after the principal current of the opposing polarity has decreased to zero.

SPURIOUS GATE SIGNALS: In noisy electrical environments, it is possible for enough energy to cause gate triggering to be coupled into the gate wiring by stray capacitance or electromagnetic induction. It is therefore advisable to keep the gate lead short and have the common return directly to the cathode or MT1. In extreme cases, shielded wire may be required. Another aid commonly used is to connect a capacitance on the order of 0.01 to 0.1μF across the gate and cathode terminals. This has the added advantage of increasing the thyristor dv/dt capability, since it forms a capacitive divider with the anode to gate capacitance. The gate capacitor also reduces the rate of application of gate trigger current which may cause di/dt failures if a high inrush load is present.

THYRISTOR RATINGS

To insure long life and proper operation, it is important that operating conditions be restrained from exceeding thyristor ratings. The most important and fundamental ratings are temperature and voltage which are interrelated to some extent. The voltage ratings are applicable only up to the maximum temperature ratings of a particular part number. The temperature rating may be chosen by the manufacturer to insure satisfactory voltage ratings, switching speeds, or dv/dt ability.

OPERATING CURRENT RATINGS

Current ratings are not independently established as a rule. The values are chosen such that at a practical case temperature the power dissipation will not cause the junction temperature rating to be exceeded.

Various manufacturers may choose different criteria to establish ratings. At Motorola, use is made of the thermal response of the semiconductor and worst case values of on-state voltage and thermal resistance, to guarantee the junction temperature is at or below its rated value. Values shown on data sheets consequently differ somewhat from those computed from the standard formula:

$$T_C\,(\max) = T\,(\text{rated}) - R_{\theta JC} \times P_{D(AV)}$$

where

T_C (max) = Maximum allowable case temperature

T (rated) = Rated junction temperature or maximum rated case temperature with zero principal current and rated ac blocking voltage applied.

$R_{\theta JC}$ = Junction to case thermal resistance

$P_{D(AV)}$ = Average power dissipation

The above formula is generally suitable for estimating case temperature in situations not covered by data sheet information. Worst case values should be used for thermal resistance and power dissipation.

OVERLOAD CURRENT RATINGS

Overload current ratings may be divided into two types: non-repetitive and repetitive.

Non-repetitive overloads are those which are not a part of the normal application of the device. Examples of such overloads are faults in the equipment in which the devices are used and accidental shorting of the load. Non-repetitive overload ratings permit the device to exceed its maximum operating junction temperature for short periods of time because this overload rating applies following any rated load condition. In the case of a reverse blocking thyristor or SCR, the device must block rated voltage in the reverse direction during the current overload. However, no type of thyristor is required to block off-stage voltage at any time during or immediately following the overload. Thus, in the case of a triac, the device need not block in either direction during or immediately following the overload. Usually only approximately one hundred such current overloads are permitted over the life of the device. These non-repetitive overload ratings just described may be divided into two types: multicycle (which include single cycle) and subcycle. For an SCR, the multicycle overload current rating, or surge current rating as it is commonly called, is generally presented as a curve giving the maximum peak

values of half sine wave on-state current as a function of overload duration measured in number of cycles for a 60 Hz frequency.

For a triac, the current waveform used in the rating is a full sine wave. Multicycle surge curves are used to select proper circuit breakers and series line impedances to prevent damage to the thyristor in the event of an equipment fault.

The subcycle overload or subcycle surge rating curve is so called because the time duration of the rating is usually from about one to eight milliseconds which is less than the time of one cycle of a 60 Hz power source. Overload peak current is often given in curve form as a function of overload duration. This rating also applies following any rated load condition and neither off-state nor reverse blocking capability is required on the part of the thyristor immediately following the overload current. The subcycle surge current rating may be used to select the proper current-limiting fuse for protection of the thyristor in the event of an equipment fault. Since this use of the rating is so common, manufacturers simply publish the i^2t rating in place of the subcycle current overload curve because fuses are commonly rated in terms of i^2t. The i^2t rating can be approximated from the single cycle surge rating (I_{TSM}) by using:

$$i^2t = I^2_{TSM} \times t/2$$

where the time t is the time base of the overload, i.e., 8.33 ms for a 60 Hz frequency.

Repetitive overloads are those which are an intended part of the application such as a motor drive application. Since this type of overload may occur a large number of times during the life of the thyristor, its rated maximum operating junction temperature must not be exceeded during the overload if long thyristor life is required. Since this type of overload may have a complex current waveform and duty-cycle, a current rating analysis involving the use of the transient thermal impedance characteristics is often the only practical approach. In this type of analysis, the thyristor junction-to-case transient thermal impedance characteristic is added to the user's heat dissipator transient thermal impedance characteristic. Then by the superposition of power waveforms in conjunction with the composite thermal impedance curve, the overload current rating can be obtained. The exact calculation procedure is found in the power semiconductor literature.

THEORY OF SCR POWER CONTROL

The most common form of SCR power control is phase control. In this mode of operation, the SCR is held in an off condition for a portion of the positive half cycle and then is triggered into an on condition at a time in the half cycle determined by the control circuitry (in which the circuit current is limited only by the load — the entire line voltage except for a nominal one volt drop across the SCR is applied to the load).

One SCR alone can control only one half cycle of the waveform. For full wave ac control, two SCRs are connected in inverse parallel (the anode of each connected to the cathode of the other, see Figure 2.9a). For full wave dc control, two methods are possible. Two SCRs may be used in a bridge rectifier (see Figure 2.9b) or one SCR may be placed in series with a diode bridge (see Figure 2.9c).

Figure 2.10 shows the voltage waveform along with some common terms used in describing SCR operation. Delay angle is the time, measured in electrical degrees, during which the SCR is blocking the line voltage. The period during which the SCR is on is called the conduction angle.

It is important to note that the SCR is a voltage controlling device. The load and power source determine the circuit current.

Now we arrive at a problem. Different loads respond to different characteristics of the ac waveform. Some loads are sensitive to peak voltage, some to average voltage and some to rms voltage. Figure 2.11 shows the various characteristic voltages plotted against the conduction angle for half wave and full wave circuits. These voltages have been normalized to the rms of the applied voltage. To determine the actual peak, average or rms voltage for any conduction angle, we simply multiply the normalized voltage by the rms value of the applied line voltage. (These normalized curves also apply to current in a resistive circuit.) Since the greatest majority of circuits are either 115 or 230 volt power, the curves have been redrawn for these voltages in Figure 2.12.

A relative power curve has been added to Figure 2.12 for constant impedance loads such as heaters. (Incandescent lamps and motors do not follow this curve precisely since their relative impedance changes with applied voltage.) To use the curves, we find the full wave rated power of the load, then multiply by the fraction associated with the phase angle in question. For example, a 180° conduction angle in a half wave circuit provides 0.5 x full wave full-conduction power.

An interesting point is illustrated by the power curves. A conduction angle of 30° provides only three per cent of full power in a full wave circuit, and a conduction angle of 150° provides 97 per cent of full power. Thus, the control circuit can provide 94 per cent of full power control with a pulse phase variation of only 120°. Thus, it becomes pointless in many cases to try to obtain conduction angles less than 30° or greater than 150°.

CONTROL CHARACTERISTICS

The simplest and most common control circuit for phase control is a relaxation oscillator. This circuit is shown diagrammatically as it would be used with an SCR in Figure 2.13. The capacitor is charged through the resistor from a voltage or current source until the breakover voltage of the trigger device is reached. At that time, the trigger device changes to its on state, and the capacitor is discharged through the gate of the SCR. Turn-on of the

SCR is thus accomplished with a short, high current pulse. Commonly used trigger devices are unijunction and programmable unijunction transistors, silicon bilateral switches, sidacs and optically coupled thyristors. Phase control can be obtained by varying the RC time constant of a charging circuit so that trigger device turn-on occurs at varying phase angles within the controlled half cycle.

If the relaxation oscillator is to be operated from a pure dc source, the capacitor voltage-time characteristic is shown in Figure 2.14. This shows the capacitor voltage as it rises all the way to the supply voltage through several time constants. Figure 2.14(b) shows the charge characteristic in the first time constant greatly expanded. It is this portion of the capacitor charge characteristic which is most often used in SCR and Triac control circuits.

Generally, a design starting point is selection of a capacitance value which will reliably trigger the thyristor when the capacitor is discharged. Gate characteristics and ratings, trigger device properties and the load impedance play a part in the selection. Since not all of the important parameters for this selection are completely specified, experimental determination is often the best method.

Low-current loads and strongly inductive circuits sometimes cause triggering difficulty because the gate current pulse goes away before the principal thyristor current achieves the latching value. A series gate resistor can be used to introduce a RC discharge time constant in the gate circuit and lengthen trigger pulse duration allowing more time for the main terminal current to rise to the latching value. Small thyristors will require a series gate resistance to avoid exceeding the gate ratings. The discharge time constant of a snubber, if used, can also aid latching. The duration of these capacitor discharge duration currents can be estimated by

$t_{w10} = 2.3\ RC$ where t_{w10} = time for current to decay to 10% of the peak.

For example, when an 8 volt SBS is used to discharge a 0.5 μF capacitor through a 15 ohm resistor into the gate of an SCR

$t_{w10} = (2.3)\ (15)\ (0.5) = 17.3\ \mu s.$

Because of internal voltage drops in the SBS and SCR gates, the peak current will be somewhat less than

$I_{pk} = 8/15 = 0.53$ amp.

All trigger devices require some drive current to fire. Highly sensitive devices appear to be voltage operated when the current required to fire them is insignificant. The MBS4991 SBS requires that the switching current be taken into consideration. For a given RC time constant, larger capacitors allow the use of lower value timing resistors and less sensitive trigger components.

An example will demonstrate the procedure. Assume that we wish to trigger a 2N4170 SCR with an 8 volt MBS4991. We have determined that a 1 μF capacitor will supply the necessary SCR gate current magnitude and duration while not exceeding the gate ratings. Assume a 16 volt 60 Hz dc gate power supply, 30° minimum con-

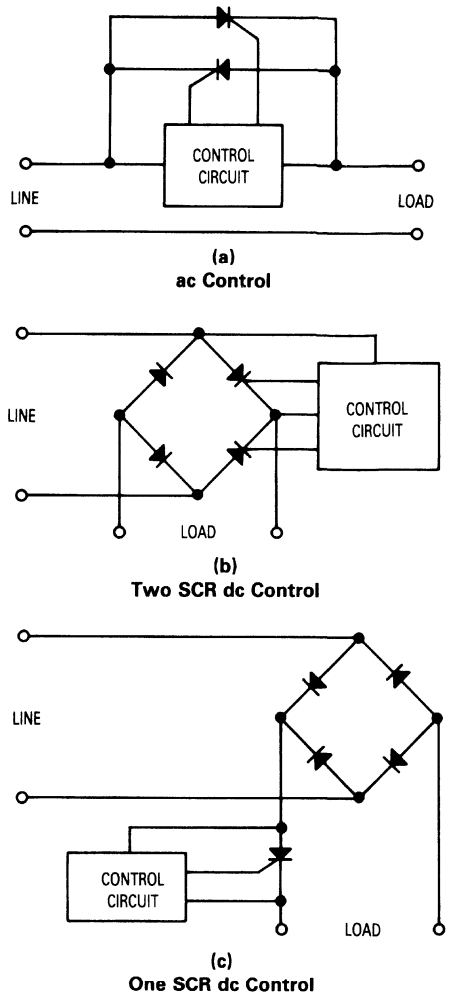


Figure 2.9. SCR Connections For Various Methods Of Phase Control

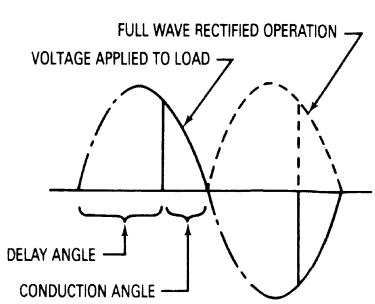


Figure 2.10. Sine Wave Showing Principles Of Phase Control

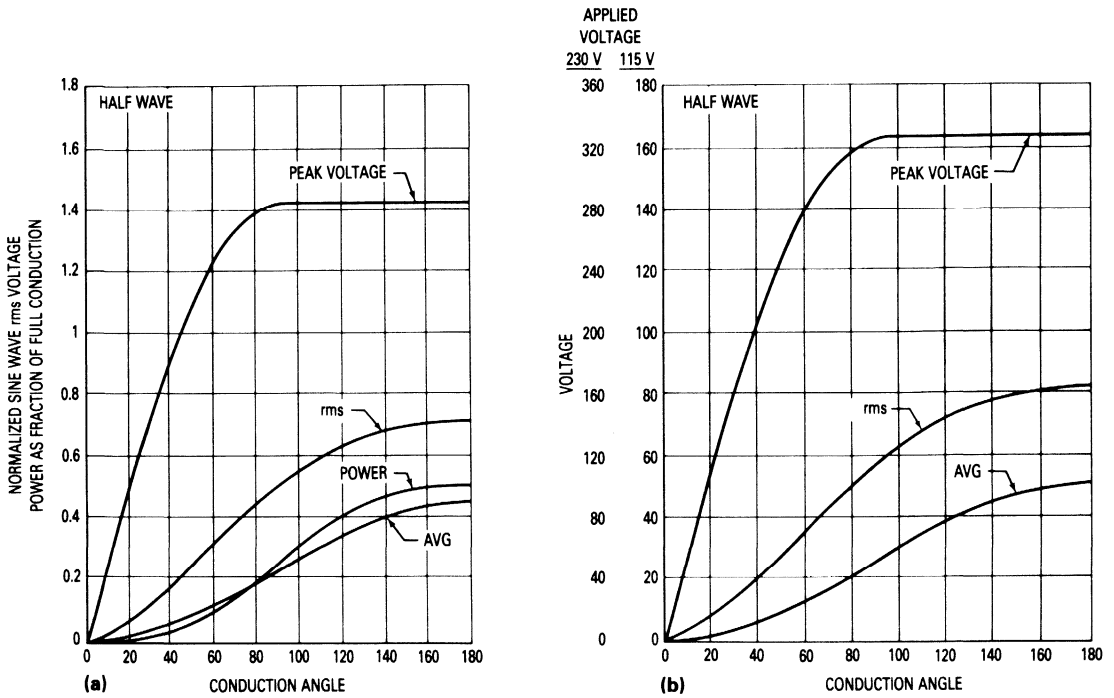


Figure 2.11. Half-Wave Characteristics Of Thyristor Power Control

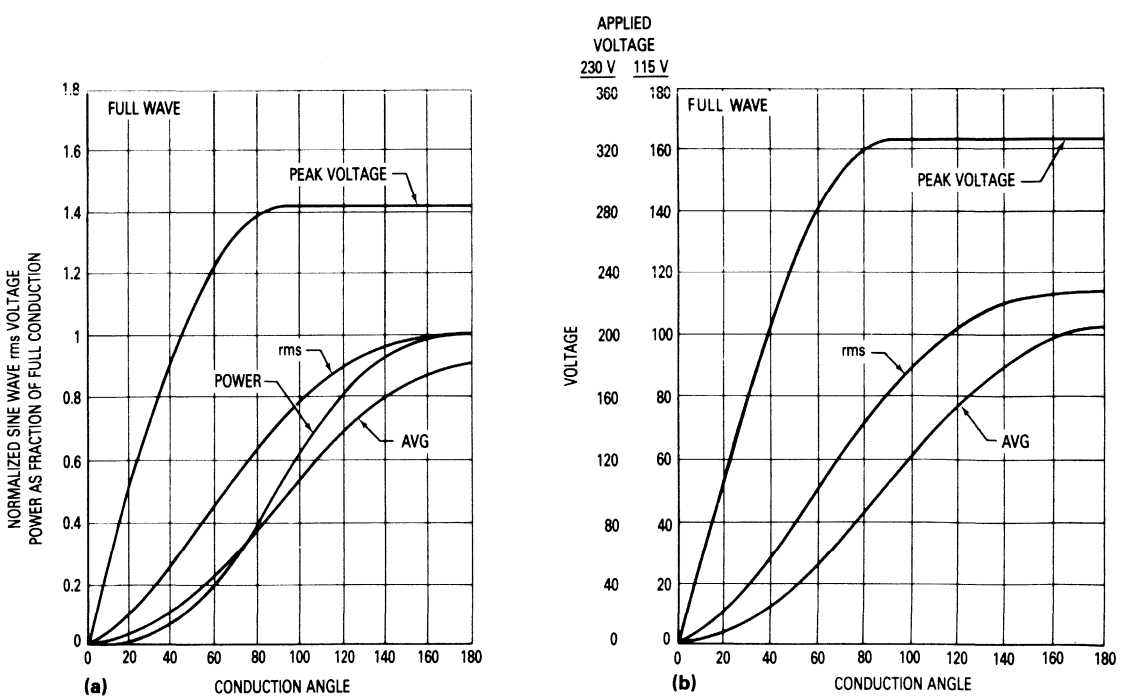


Figure 2.12. Full-Wave Characteristics Of Thyristor Power Control

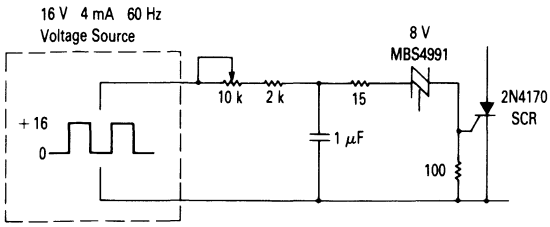


Figure 2.13. SCR Trigger Circuit

duction angle and 150° maximum conduction angle with a 60 Hz anode power source. The capacitor must charge to 8/16 or 0.5 of the available charging voltage in the desired time. Referring to Figure 2.14(b), we see that 0.5 of the charging voltage represents 0.693 time constant. The 30° conduction angle requires that the firing pulse be delayed 150° or 6.94 milliseconds (8.33 milliseconds is the period of 1/2 cycle at 60 Hz). To obtain this delay,

$$6.94 \text{ ms} = 0.693 \text{ RC}$$
$$\text{RC} = 10.01 \text{ ms.}$$

If C = 1 μF,

$$R = \frac{10 \times 10^{-3}}{1 \times 10^{-6}} = 10 \text{ k ohms.}$$

The timing resistor must be capable of supplying at least the worst case maximum SBS switching current at the peak point voltage. The available current is

$$\frac{16 \text{ V} - 8 \text{ V}}{10^4 \text{ ohms}} = 800\ \mu\text{A.}$$

This is more than the 500 μA needed by the MBS4991 at 25°C. If it were not, the design procedure would need to be repeated using larger C and smaller R. Alternatively, a more sensitive MBS4992 could be used.

To obtain minimum R, 150° conduction angle, the delay is 30° or

$$30/180 \times 8.33 = 1.39 \text{ ms}$$
$$1.39 \text{ ms} = 0.693 \text{ RC}$$
$$\text{RC} = 2.01 \text{ ms}$$

$$R = \frac{2.01 \times 10^{-3}}{1 \times 10^{-6}} = 2000 \text{ ohms.}$$

A 10 k potentiometer with a 2 k series resistor will serve this purpose.

In this application, the trigger circuit is reset by line crossing each half cycle. Consequently, SBS latching after firing is permissible. If the device were used as a free running oscillator, it would be necessary for the peak point current to be less than the minimum holding current specification of the SBS at maximum operating temperature. Timing accuracy requires the 16 V source to be capable of supplying the worst case required current. In the example, the initial instantaneous capacitor charging current will be 16 V/2 k = 8 mA. The gate load line must also enclose the peak point voltage. The SBS clamps the capacitor voltage when it breaks over causing little or no further change in the voltage across the capacitor. Consequently, all of the available current at that time (16 V–8 V)/2 k = 4 mA) diverts through the SBS causing it to fire.

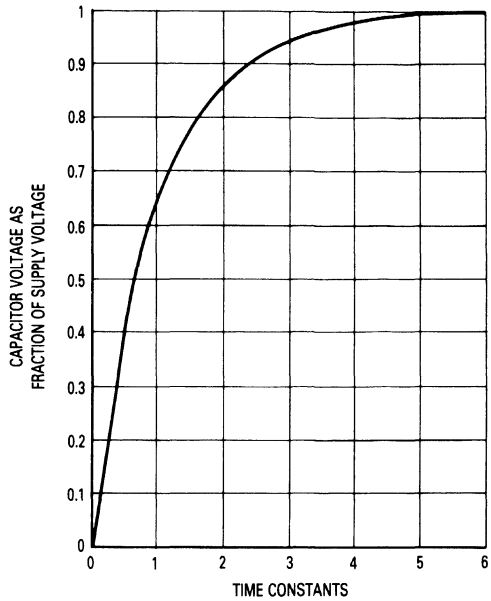


Figure 2.14(a). Capacitor Charging From dc Source

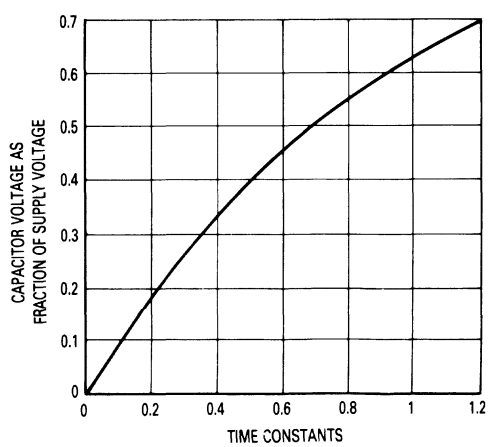


Figure 2.14(b). Expanded Scale

In many of the recently proposed circuits for low cost operation, the timing capacitor of the relaxation oscillator is charged through a rectifier and resistor using the ac power line as a source. Calculations of charging time with this circuit become exceedingly difficult, although they are still necessary for circuit design. The curves of Figure 2.15 simplify the design immensely. These curves show the voltage-time characteristic of the capacitor charged from one half cycle of a sine wave. Voltage is normalized

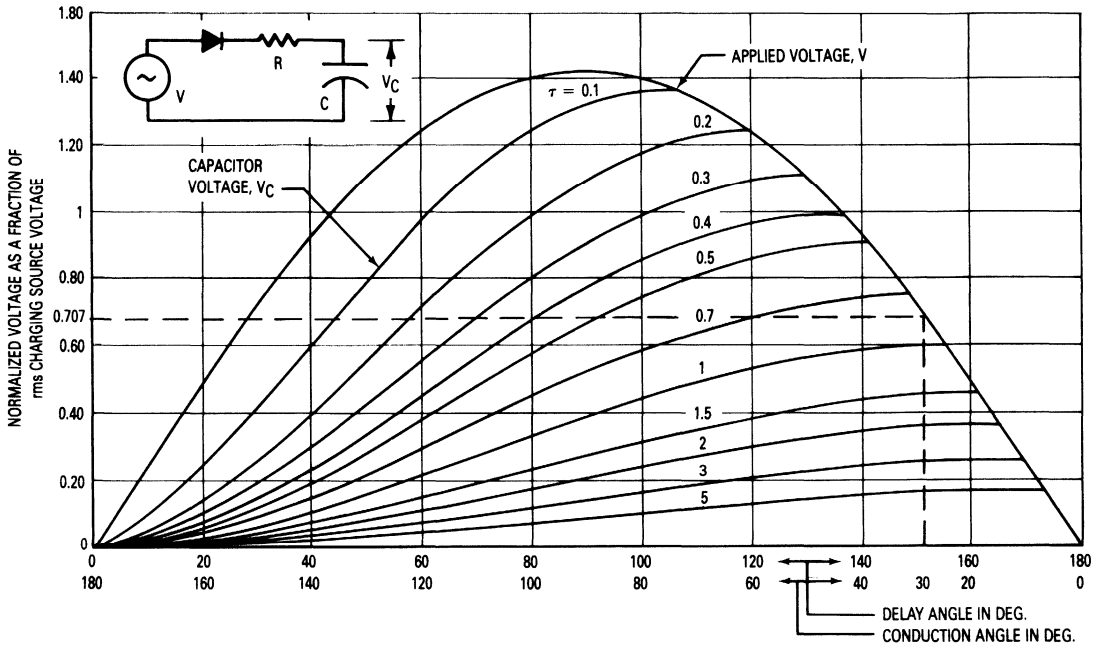


Figure 2.15(a). Capacitor Voltage When Charged

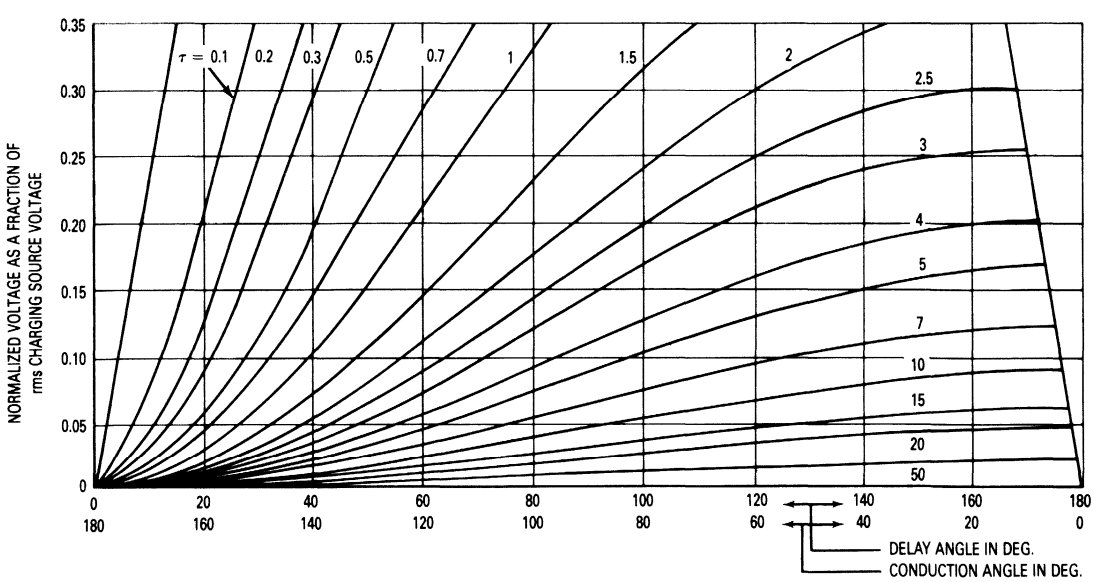


Figure 2.15(b). Expansion of Figure 2.15(a)

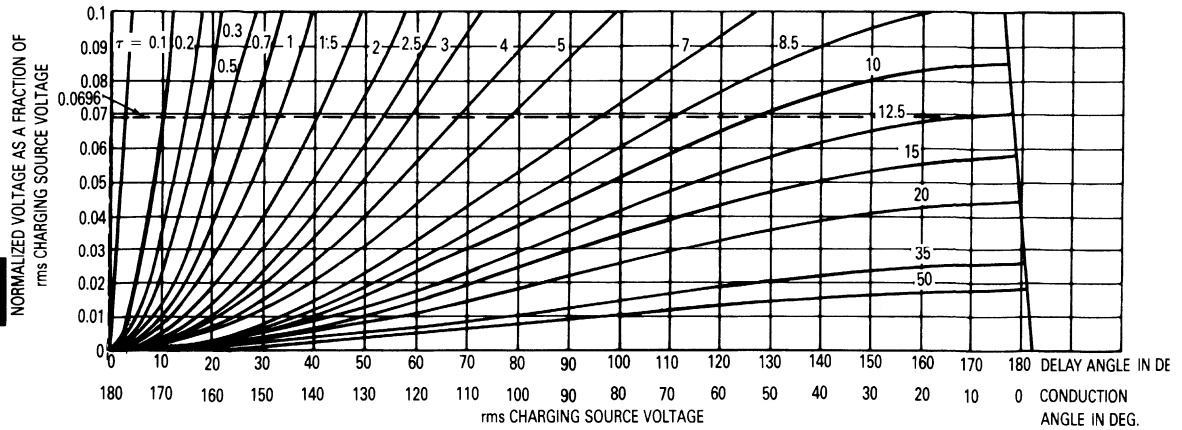


Figure 2.15(c). Expansion of Figure 2.15(b)

to the rms value of the sine wave for convenience of use. The parameter of the curves is a new term, the ratio of the RC time constant to the period of one half cycle, and is denoted by the Greek letter τ. It may most easily be calculated from the equation

$\tau = 2RCf$. Where: R = resistance in Ohms
C = capacitance in Farads
f = frequency in Hertz.

To use the curves when starting the capacitor charge from zero each half cycle, a line is drawn horizontally across the curves at the relative voltage level of the trigger breakdown compared to the rms sine wave voltage. The τ is determined for maximum and minimum conduction angles and the limits of R may be found from the equation for τ.

An example will again clarify the picture. Consider the same problem as the previous example, except that the capacitor charging source is the 115 Vac, 60 Hz power line.

The ratio of the trigger diode breakover voltage to the RMS charging voltage is then

$8/115 = 69.6 \times 10^{-3}$.

A line drawn at 0.0696 on the ordinate of Figure 2.15(c) shows that for a conduction angle of 30°, $\tau = 12$, and for a conduction angle of 150°, $\tau = 0.8$. Therefore, since R $= \tau/(2CF)$

$$R_{max} = \frac{12}{2(1.0\times10^{-6})60} \text{ 100 k ohms,}$$

$$R_{min} = \frac{0.8}{2(1\times10^{-6})60} = \text{6667 ohms.}$$

These values would require a potentiometer of 100 k in series with a 6.2 k minimum fixed resistance.

The timing resistor must be capable of supplying the highest switching current allowed by the SBS specification at the switching voltage.

When the conduction angle is less than 90°, triggering takes place along the back of the power line sine wave and maximum firing current thru the SBS is at the start of SBS breakover. If this current does not equal or exceed "Is" the SBS will fail to trigger and phase control will be lost. This can be prevented by selecting a lower value resistor and larger capacitor. The available current can be determined from Figure 2.15(a). The vertical line drawn from the conduction angle of 30° intersects the applied voltage curve at 0.707. The instantaneous current at breakover is then

$I = (0.707\times115^{-8})/100\text{ k} = 733\ \mu A$.

When the conduction angle is greater than 90°, triggering takes place before the peak of the sine wave. If the current thru the SBS does not exceed the switching current at the moment of breakover, triggering may still take place but not at the predicted time because of the additional delay for the rising line voltage to drive the SBS current up to the switching level. Usually long conduction angles are associated with low value timing resistors making this problem less likely. The SBS current at the moment of breakover can be determined by the same method described for the trailing edge.

It is advisable to use a shunt gate-cathode resistor across sensitive gate SCR's to provide a path for leakage currents and to insure that firing of the SCR causes turn-on of the trigger device and discharge of the gate circuit capacitor.

Figure 2.16(a) shows a simple dc full wave control circuit. R_{GK} is optional on non-sensitive gate parts. Figure 2.16(b) shows an ac control derived from that of Figure 2.16(a). Figure 2.16(c) is a double time constant circuit featuring low hysteresis.

TRIAC THEORY

The triac is a three-terminal ac semiconductor switch which is triggered into conduction when a low-energy signal is applied to its gate. Unlike the silicon controlled rectifier or SCR, the triac will conduct current in either direction when turned on. The triac also differs from the SCR in that either a positive or negative gate signal will trigger the triac into conduction. The triac may be thought of as two complementary SCRs in parallel.

The triac offers the circuit designer an economical and versatile means of accurately controlling ac power. It has several advantages over conventional mechanical switches. Since the triac has a positive "on" and a zero-current "off" characteristic, it does not suffer from the contact bounce or arcing inherent in mechanical switches. The switching action of the triac is very fast compared to conventional relays, giving more accurate control. A triac can be trigged by dc, ac, rectified ac or pulses. Because of the low energy required for triggering a triac, the control circuit can use any of a number of low-cost solid-state devices presently on the market such as transistors, unijunction transistors, bilateral switches, four-layer diodes and sensitive-gate SCRs and optically coupled drivers.

CHARACTERISTICS OF THE TRIAC

Figure 2.17(a) shows the triac symbol and its relationship to a typical package. Since the triac is a bilateral device, the terms "anode" and "cathode" used for unilateral devices have no meaning. Therefore, the terminals are simply designated by MT1, MT2, and G, where MT1 and MT2 are the current-carrying terminals, and G is the gate terminal used for triggering the triac. To avoid confusion, it has become standard practice to specify all currents and voltages using MT1 as the reference point.

The basic structure of a triac is shown in Figure 2.17(b). This drawing shows why the symbol adopted for the triac consists of two complementary SCRs with a common gate. The triac is a five-layer device with the region between MT1 and MT2 being a P-N-P-N switch (SCR) in parallel with a N-P-N-P switch (complementary SCR). Also, the structure gives some insight into the triac's ability to be triggered with either a positive or negative gate signal. The region between MT1 and G consists of two complementary diodes. A positive or negative gate signal will forward-bias one of these diodes causing the same transistor action found in the SCR. This action breaks down the blocking junction regardless of the polarity of

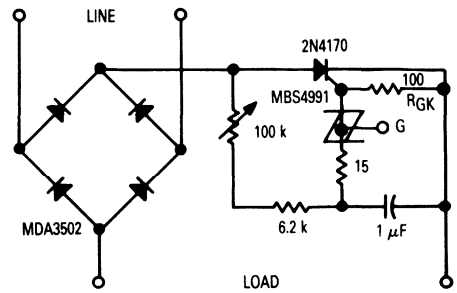


Figure 2.16(a). Simple dc Power Control Circuit

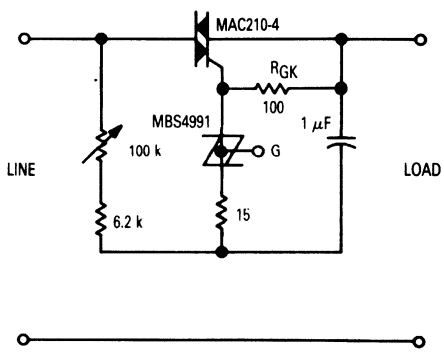


Figure 2.16(b). Simple Full-Wave Power Control

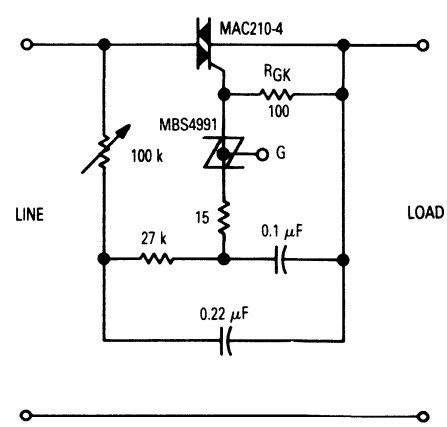


Figure 2.16(c). Full Range ac Power Control

MT1. Current flow between MT2 and MT1 then causes the device to provide gate current internally. It will remain on until this current flow is interrupted.

The voltage-current characteristic of the triac is shown in Figure 2.18 where, as previously stated, MT1 is used as the reference point. The first quadrant, Q-I, is the region where MT2 is positive with respect to MT1 and quadrant III is the opposite case. Several of the terms used in characterizing the triac are shown on the figure. V_{DRM} is the breakover voltage of the device and is the highest voltage the triac may be allowed to block in either direction. If this voltage is exceeded, even transiently, the triac may go into conduction without a gate signal. Although the triac is not damaged by this action if the current is limited, this situation should be avoided because control of the triac is lost. A triac for a particular application should have V_{DRM} at least as high as the peak of the ac waveform to be applied so reliable control can be maintained. The holding current (I_H) is the minimum value of current necessary to maintain conduction. When the current goes below I_H, the triac ceases to conduct and reverts to the blocking state. I_{DRM} is the leakage current of the triac with V_{DRM} applied from MT2 to MT1 and is several orders of magnitude smaller than the current rating of the device. The figure shows the characteristic of the triac without a gate signal applied but it should be noted that the triac can be triggered into the on state at any value of voltage up to V_{DRM} by the application of a gate signal. This important characteristic makes the triac very useful.

Since the triac will conduct in either direction and can be triggered with either a positive or negative gate signal there are four possible triggering modes (Figure 2.3):

Quadrant I; MT2(+), G(+), positive voltage and positive gate current. Quadrant II; MT2(+), G(−), positive voltage and negative gate current. Quadrant III; MT2(−), G(−), negative voltage and negative gate current. Quadrant IV; MT2(−), G(+), negative voltage and positive gate current.

Present triacs are most sensitive in quadrants I and III, slightly less so in quadrant II, and much less sensitive in quadrant IV. Therefore it is not recommended to use quadrant IV unless special circumstances dictate it.

An important fact to remember is that since a triac can conduct current in both directions, it has only a brief interval during which the sine wave current is passing through zero to recover and revert to its blocking state. For this reason, reliable operation of present triacs is limited to 60 Hz line frequency and lower frequencies.

For inductive loads, the phase-shift between the current and voltage means that at the time the current falls below I_H and the triac ceases to conduct, there exists a certain voltage which must appear across the triac. If this voltage appears too rapidly, the triac will resume conduction and control is lost. In order to achieve control with certain inductive loads, the rate of rise in voltage (dv/dt) must be limited by a series RC network across the triac. The capacitor will then limit the dv/dt across the triac. The resistor is necessary to limit the surge of current from the capacitor when the triac fires, and to damp the ringing of the capacitance with the load inductance.

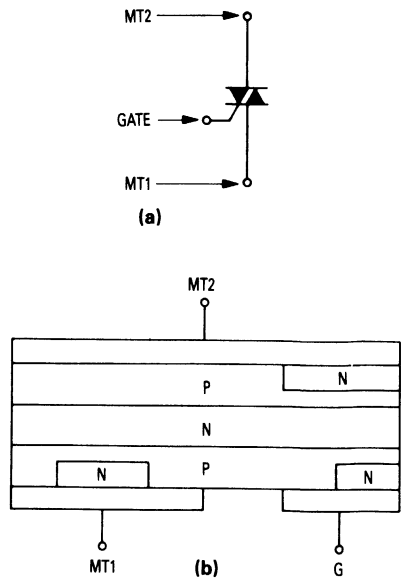


Figure 2.17. Triac Structure and Symbol

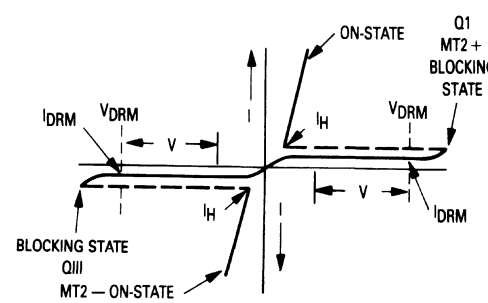


Figure 2.18. Triac Voltage-Current Characteristic

METHODS OF CONTROL

AC SWITCH

A useful application of the triac is as a direct replacement for an ac mechanical relay. In this application, the triac furnishes on-off control and the power-regulating ability of the triac is not utilized. The control circuitry for this application is usually very simple, consisting of a source for the gate signal and some type of small current switch, either mechanical or electrical. The gate signal can be obtained from a separate source or directly from the line voltage at terminal MT2 of the triac.

PHASE CONTROL

An effective and widely-used method of controlling the average power to a load through the triac is by phase control. Phase control is a method of utilizing the triac to apply the ac supply to the load for a controlled fraction of each cycle. In this mode of operation, the triac is held in an off or open condition for a portion of each positive and negative cycle, and then is triggered into an on condition at a time in the half cycle determined by the control circuitry. In the on condition, the circuit current is limited only by the load — i.e., the entire line voltage (less the forward drop of the triac) is applied to the load.

Figure 2.19 shows the voltage waveform along with some common terms used in describing triac operation. Delay angle is the angle, measured in electrical degrees, during which the triac is blocking the line voltage. The period during which the triac is on is called the conduction angle.

It is important to note that the triac is either off (blocking voltage) or fully on (conducting). When it is in the on condition, the circuit current is determined only by the load and the power source.

As one might expect, in spite of its usefulness, phase control is not without disadvantages. The main disadvantage of using phase control in triac applications is the generation of electro-magnetic interference (EMI). Each time the triac is fired the load current rises from zero to the load-limited current value in a very short time. The resulting di/dt generates a wide spectrum of noise which may interfere with the operation of nearby electronic equipment unless proper filtering is used.

ZERO POINT SWITCHING

In addition to filtering, EMI can be minimized by zero-point switching, which is often preferable. Zero-point switching is a technique whereby the control element (in this case the triac) is gated on at the instant the sine wave voltage goes through zero. This reduces, or eliminates, turn-on transients and the EMI. Power to the load is controlled by providing bursts of complete sine waves to the load as shown in Figure 2.20. Modulation can be on a random basis with an on-off control, or a proportioning basis with the proper type of proportional control.

In order for zero-point switching to be effective, it must indeed be *zero point* switching. If a triac is turned on with as little as 10 volts across it into a load of a few-hundred watts, sufficient EMI will result to nullify the advantages of adopting zero-point switching in the first place.

BASIC TRIAC AC SWITCHES

Figure 2.21 shows methods of using the triac as an on-off switch. These circuits are useful in applications where simplicity and reliability are important. As previously stated, there is no arcing with the triac, which can be very important in some applications. The circuits are for resistive loads as shown and require the addition of a dv/dt network across the triac for inductive loads. Figure 2.21(a) shows low-voltage control of the triac. When switch S1 is closed, gate current is supplied to the triac from the 10 volt battery. In order to reduce surge current failures during turn on (t_{on}), this current should be 5 to 10 times the maximum gate current (I_{GT}) required to trigger the triac.

The triac turns on and remains on until S1 is opened. This circuit switches at zero current except for initial turn on. S1 can be a very-low-current switch because it carries only the triac gate current.

Figure 2.21(b) shows a triac switch with the same characteristics as the circuit in Figure 2.21(a) except the need for a battery has been eliminated. The gate signal is obtained from the voltage at MT2 of the triac prior to turn on.

The circuit shown in Figure 2.21(c) is a modification of Figure 2.21(b). When switch S1 is in position one, the triac receives no gate current and is non-conducting. With S1 in position two, circuit operation is the same as that for Figure 2.21(b). In position three, the triac receives gate current only on positive half cycles. Therefore, the triac conducts only on positive half cycles and the power to the load is half wave.

Figure 2.21(d) shows ac control of the triac. The pulse can be transformer coupled to isolate power and control circuits. Peak current should be 10 times $I_{GT(max)}$ and the RC time constant should be 5 times $t_{on(max)}$. A high frequency pulse (1 to 5 kHz) is often used to obtain zero point switching.

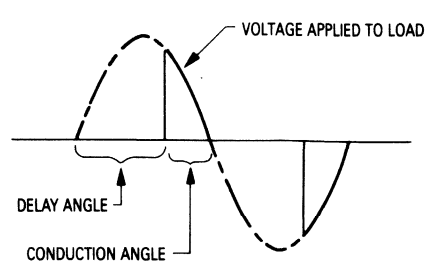


Figure 2.19. Sine Wave Showing Principles of Phase Control

ZERO POINT SWITCHING TECHNIQUES

Zero-point switches are highly desirable in many applications because they do not generate electro-magnetic interference (EMI). A zero-point switch controls sine-wave power in such a way that either complete cycles or half cycles of the power supply voltage are applied to the load as shown in Figure 2.22. This type of switching is primarily used to control power to resistive loads such as heaters. It can also be used for controlling the speed of motors if the duty cycle is modulated by having short bursts of power applied to the load and the load characteristic is primarily inertial rather than frictional. Modulation can be on a random basis with an on-off control, or on a proportioning basis with the proper type of proportioning control.

In order for zero-point switching to be effective, it must be true zero-point switching. If an SCR is turned on with an anode voltage as low as 10 volts and a load of just a few hundred watts, sufficient EMI will result to nullify the advantages of going to zero-point switching in the first place. The thyristor to be turned on must receive gate drive exactly at the zero crossing of the applied voltage.

The most successful method of zero-point thyristor control is therefore, to have the gate signal applied before the zero crossing. As soon as the zero crossing occurs, anode voltage will be supplied and the thyristor will come on. This is effectively accomplished by using a capacitor to derive a 90° leading gate signal from the power line source. However, only one thyristor can be controlled from this phase-shifted signal, and a slaving circuit is necessary to control the other SCR to get full-wave power control. These basic ideas are illustrated in Figure 2.23. The slaving circuit fires only on the half cycle after the firing of the master SCR. This guarantees that only complete cycles of power will be applied to the load. The gate signal to the master SCR receives all the control; a convenient control method is to replace the switch with a

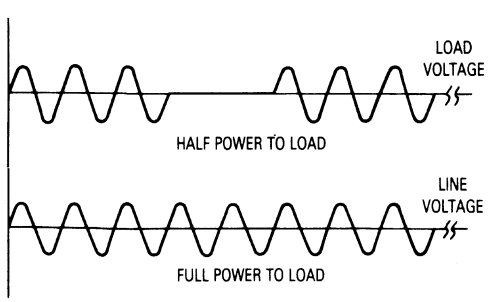
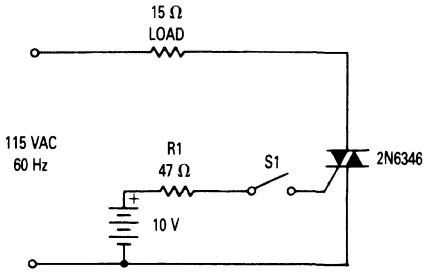
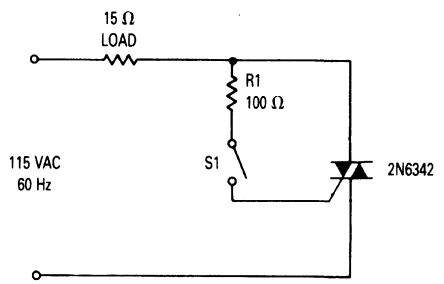


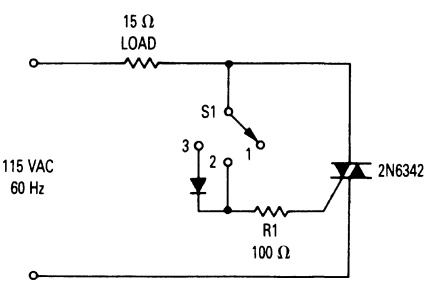
Figure 2.20. Sine Wave Showing Principles of Zero-Point Switching



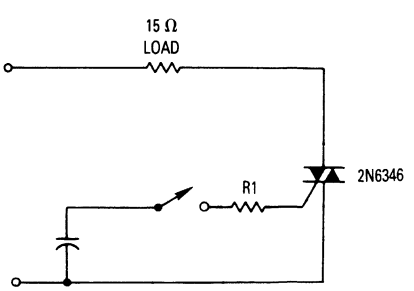
(a): Low Voltage Controlled Triac Switch



(b): Triac ac Static Contractor



(c): 3 Position Static Switch



(d): AC Controlled Triac Switch

Figure 2.21. Triac Switches

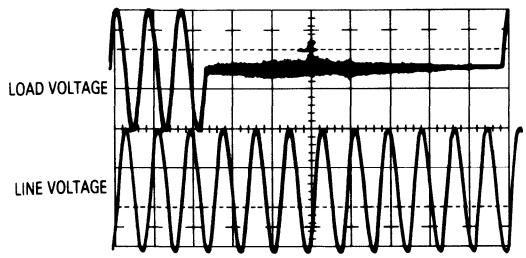


Figure 2.22. Load Voltage and Line Voltage for 25% Duty Cycle

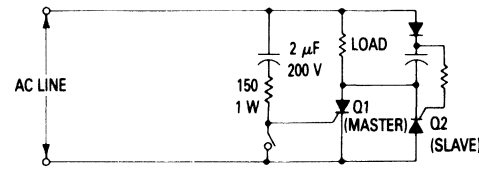


Figure 2.23. Slave and Master SCRs for Zero-Point Switching

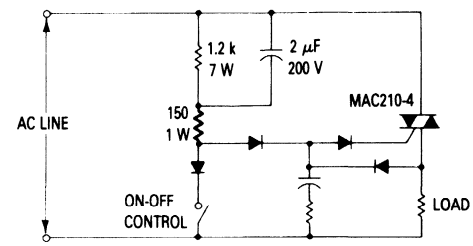


Figure 2.24. Triac Zero-Point Switch

low-power transistor, which can be controlled by bridge-sensing circuits, manually controlled potentiometers, or various other techniques.

A basic SCR is very effective and trouble free. However, it can dissipate considerable power. This must be taken into account in designing the circuit and its packaging.

In the case of triacs, a slaving circuit is also usually required to furnish the gate signal for the negative half cycle. However, triacs can use slave circuits requiring less power than do SCRs as shown in Figure 2.23. Other considerations being equal, the easier slaving will sometimes make the triac circuit more desirable than the SCR circuit.

Besides slaving circuit power dissipation, there is another consideration which should be carefully checked when using high-power zero-point switching. Since this is on-off switching, it abruptly applies the full load to the power line every time the circuit turns on. This may cause a temporary drop in voltage which can lead to erratic operation of other electrical equipment on the line (light dimming, TV picture shrinkage, etc.). For this reason, loads with high cycling rates should not be powered from the same supply lines as lights and other voltage-sensitive devices. On the other hand, if the load cycling rate is slow, say once per half minute, the loading flicker may not be objectionable on lighting circuits.

A note of caution is in order here. The full-wave zero-point switching control illustrated in Figure 2.23 should not be used as a half-wave control by removing the slave SCR. When the slave SCR in Figure 2.23 is removed, the master SCR has positive gate current flowing over approximately 1/4 of a cycle while the SCR itself is in the reverse-blocking state. This occurs during the negative half cycle of the line voltage. When this condition exists, Q1 will have a high leakage current with full voltage applied and will therefore be dissipating high power. This will cause excessive heating of the SCR and may lead to its failure. If it is desirable to use such a circuit as a half-wave control, then some means of clamping the gate signal during the negative half cycle must be devised to inhibit gate current while the SCR is reverse blocking. The circuits shown in Figures 2.25 and 2.26 do not have this disadvantage and may be used as half-wave controls.

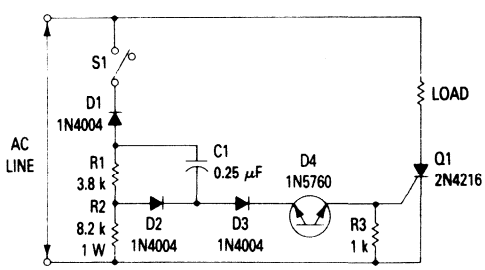


Figure 2.25. Sensitive-Gate Switch

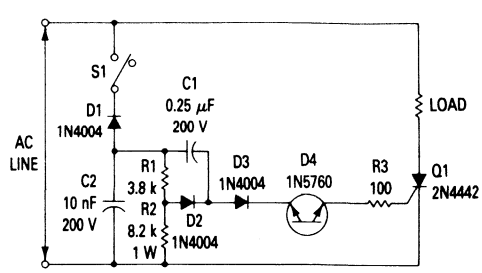


Figure 2.26. Zero-Point Switch

OPERATION

The zero-point switches shown in Figures 2.25 and 2.26 are used to insure that the control SCR turns on at the start of each positive alternation. In Figure 2.25 a pulse is generated before the zero crossing and provides a small amount of gate current when line voltage starts to go positive. This circuit is primarily for sensitive-gate SCRs. Less-sensitive SCRs, with their higher gate currents, normally require smaller values for R1 and R2 and the result can be high power dissipation in these resistors. The circuit of Figure 2.26 uses a capacitor, C2, to provide a low-impedance path around resistors R1 and R2 and can be used with less-sensitive, higher-current SCRs without increasing the dissipation. This circuit actually oscillates near the zero crossing point and provides a series of pulses to assure zero-point switching.

The basic circuit is that shown in Figure 2.25. Operation begins when switch S1 is closed. If the positive alternation is present, nothing will happen since diode D1 is reverse biased. When the negative alternation begins, capacitor C1 will charge through resistor R2 toward the limit of voltage set by the voltage divider consisting of resistors R1 and R2. As the negative alternation reaches its peak, C1 will have charged to about 40 volts. Line voltage will decrease but C1 cannot discharge because diode D2 will be reverse biased. It can be seen that C1 and three-layer diode D4 are effectively in series with the line. When the line drops to 10 volts, C1 will still be 40 volts positive with respect to the gate of Q1. At this time D4 will see about 30 volts and will trigger. This allows C1 to discharge through D3, D4, the gate of Q1, R2, and R1. This discharge current will continue to flow as the line voltage crosses zero and will insure that Q1 turns on at the start of the positive alternation. Diode D3 prevents reverse gate-current flow and resistor R3 prevents false triggering.

The circuit in Figure 2.26 operates in a similar manner up to the point where C1 starts to discharge into the gate. The discharge path will now be from C1 through D3, D4, R3, the gate of Q1, and capacitor C2. C2 will quickly charge from this high pulse of current. This reduces the voltage across D4 causing it to turn off and again revert to its blocking state. Now C2 will discharge through R1 and R2 until the voltage on D4 again becomes sufficient to cause it to break back. This repetitive exchange of charge from C1 to C2 causes a series of gate-current pulses to flow as the line voltage crosses zero. This means that Q1 will again be turned on at the start of each positive alternation as desired. Resistor R3 has been added to limit the peak gate current.

AN SCR SLAVING CIRCUIT

An SCR slaving circuit will provide full-wave control of an ac load when the control signal is available to only one of a pair of SCRs. An SCR slaving circuit is commonly used where the master SCR is controlled by zero-point switching. Zero-point switching causes the load to receive a full cycle of line voltage whenever the control signal is applied. The duty cycle of the control signal therefore determines the average amount of power supplied to the load. Zero-point switching is necessary for large loads such as electric heaters because conventional phase-shift techniques would generate an excessive amount of electro-magnetic interference (EMI).

This particular slaving circuit has two important advantages over standard RC discharge slaving circuits. It derives these advantages with practically no increase in price by using a low-cost transistor in place of the current-limiting resistor normally used for slaving. The first advantage is that a large pulse of gate current is available at the zero-crossing point. This means that it is not necessary to select sensitive-gate SCRs for controlling power. The second advantage is that this current pulse is reduced to zero within one alternation. This has a couple of good effects on the operation of the slaving SCR. It prevents gate drive from appearing while the SCR is reverse-biased, which would produce high power dissipation within the device. It also prevents the slaved SCR from being turned on for additional half cycles after the drive is removed from the control SCR.

OPERATION

The SCR slaving circuit shown in Figure 2.27 provides a single power pulse to the gate of SCR Q2 each time SCR Q1 turns on, thus turning Q2 on for the half cycle following the one during which Q1 was on. Q2 is therefore turned on only when Q1 is turned on, and the load can be controlled by a signal connected to the gate of Q1 as shown in the schematic. The control signal can be either dc or a power pulse. If the control signal is synchronized with the power line, this circuit will make an excellent zero-point switch. During the time that Q1 is on, capacitor C1 is charged through R1, D1 and Q1. While C1 is being charged, D1 reverse-biases the base-emitter junction of Q3, thereby holding it off. The charging time constant, R1, C1, is set long enough that C1 charges for practically the entire half cycle. The charging rate of C1 follows an "S" shaped curve, charging slowly at first, then faster as the supply voltage peaks, and finally slowly again as the supply voltage decreases. When the supply voltage falls below the voltage across C1, diode D1 becomes reverse biased and the base-emitter of Q3 becomes forward biased. For the values shown, this occurs approximately 6° before the end of the half cycle con-

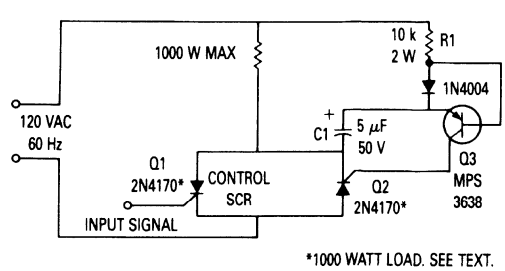


Figure 2.27. SCR Slave Circuit

duction of Q1. The base current is derived from the energy stored in C1. This turns on Q3, discharging C1 through Q3 and into the gate of Q2. As the voltage across C1 decreases, the base drive of Q3 decreases and somewhat limits the collector current. The current pulse must last until the line voltage reaches a magnitude such that latching current will exist in Q2. The values shown will deliver a current pulse which peaks at 100 mA and has a magnitude greater than 50 mA when the anode-cathode voltage of Q2 reaches plus 10 volts. This circuit completely discharges C1 during the half cycle that Q2 is on. This eliminates the possibility of Q2 being slaved for additional half cycles after the drive is removed from Q1. The peak current and the current duration are controlled by the values of R1 and C1. The values chosen provide sufficient drive for "shorted emitter" SCRs which typically require 10 to 20 mA to fire. The particular SCR used must be capable of handling the maximum current requirements of the load to be driven; the 8 ampere, 200 V SCRs shown will handle a 1000 watt load.

CHAPTER 3
THYRISTOR DRIVERS AND TRIGGERS

1

Triggering a thyristor requires meeting its gate energy specifications and there are many ways of doing this. In general, the gate should be driven hard and fast to ensure complete gate turn on and thus minimize di/dt effects. Usually this means a gate current of at least three times the gate turn on current with a pulse rise of less than one microsecond and a pulse width greater than 10 microseconds. The gate can also be driven by a dc source as long as the average gate power limits are met.

Some of the methods of driving the gate include:

1) Direct drive from logic families of transistors
2) Opto triac drivers
3) Unijunction transistors (UJTs) and programmable unijunction transistors (PUTs)
4) Silicon bilateral switches (SBSs)
5) SIDACs

In this chapter we will discuss all of these, as well as some of the important design and application considerations in triggering thyristors in general. In the chapter on applications, we will also discuss some additional considerations relating to drivers and triggers in specific applications.

PULSE TRIGGERING OF SCRs

GATE TURN-ON MECHANISM

The turn-on of PNPN devices has been discussed in many papers where it has been shown that the condition of switching is given by $\frac{dv}{di} = 0$ (i.e., $\alpha_1 + \alpha_2 = 1$, where α_1 and α_2 are the current amplification factors of the two "transistors." However, in the case of an SCR connected to a reverse gate bias, the device can have $\alpha_1 + \alpha_2 = 1$ and still stay in the blocking state. The condition of turn-on is actually $\alpha_1 + \alpha_2 > 1$.

The current amplification factor, α, increases with emitter current; some typical curves are shown in Figure 3.1. The monotonical increase of α with I_E of the device in the blocking state makes the regeneration of current (i.e., turn-on) possible.

Using the two transistor analysis, the anode current, I_A, can be expressed as a function of gate current, I_G, as:

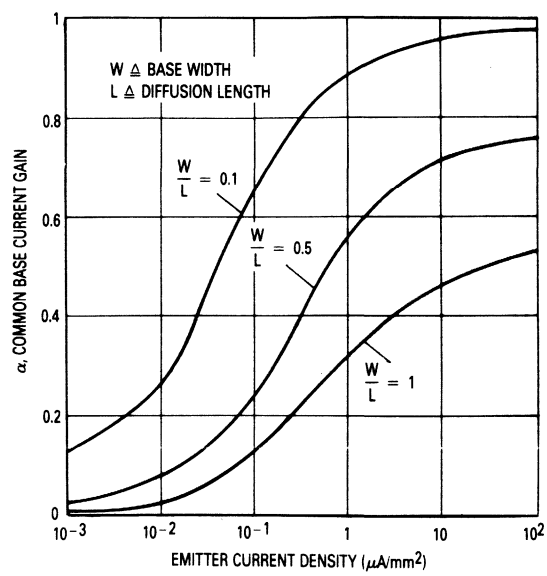


Figure 3.1. Typical Variation of Transistor α with Emitter Current Density

$$I_A = \frac{\alpha_2 I_G + I_{CS1} + I_{CS2}}{1 - \alpha_1 - \alpha_2} \quad (1)$$

Definitions and derivations are given in Appendix I. Note that the anode current, I_A, will increase to infinity as $\alpha_1 + \alpha_2 = 1$. This analysis is based upon the assumption that no majority carrier current flows out of the gate circuit. When no such assumption is made, the condition for turn-on is given by:

$$\frac{I_K}{I_A} = \frac{1 - \alpha_1}{\alpha_2} \quad (2)$$

which corresponds to $\alpha_1 + \alpha_2 > 1$ (see Appendix I).

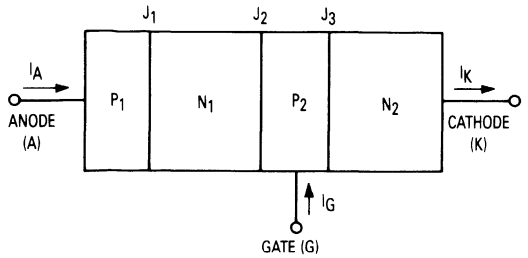


Figure 3.2. Schematic Structure of an SCR, Positive Currents Are Defined as Shown by the Arrows

Current regeneration starts when charge or current is introduced through the gate (Figure 3.2). Electrons are injected from the cathode across J_3; they travel across the P_2 "base" region to be swept out by the collector junction, J_2, and thrown into the N_1 base. The increase of majority carrier electrons in region N_1 decreases the potential in region N_1, so that holes from P_1 are injected across the junction J_1, into the N_1 "base" region to be swept across J_2, and thrown into the P_2 "base" region. The increase in the potential of region P_2 causes more electrons to be injected into P_2, thereby repeating the cycle. Since α increases with the emitter current, an increase of regeneration takes place until $\alpha_1 + \alpha_2 > 1$. Meanwhile, more carriers are collected than emitted from either of the emitters. The continuity of charge flow is violated and there is an electron build-up on the N_1 side of J_2, and a hole build-up on the P_2 side. When the inert impurity charges are compensated for by injected majority carriers, the junction J_2 becomes forward biased. The collector emits holes back to J_1 and electrons to J_3 until a steady state continuity of charge is established.

During the regeneration process, the time it takes for a minority carrier to travel across a base region is the transit time, t, which is given approximately as:

$$t_1 = \frac{W_i^2}{2D_i} \quad \text{where } W_i = \text{base width}, \; D_i = \text{diffusion length} \qquad (3)$$

(The subscript "i" can be either 1 or 2 to indicate the appropriate base.) The time taken from the start of the gate trigger to the turn-on of the device will be equal to some multiple of the transit time.

CURRENT PULSE TRIGGERING

Current pulse triggering is defined as supplying current through the gate to compensate for the carriers lost by recombination in order to provide enough current to sustain increasing regeneration. If the gate is triggered with a current pulse, shorter pulse widths require higher currents as shown by Figure 3.3(a). Figure 3.3(a) seems to indicate there is a constant amount of charge required to trigger on the device when I_G is above a threshold level. When the charge required for turn-on is plotted versus pulse current or pulse width, there is an optimum range of current levels or pulse widths for which the charge is minimum, as shown in region A of Figure 3.3(b) and (c). Region C shows that for lower current levels (i.e., longer minimum pulse widths) more charge is required to trigger on the device. Region B shows increasing charge required as the current gets higher and the pulse width smaller.

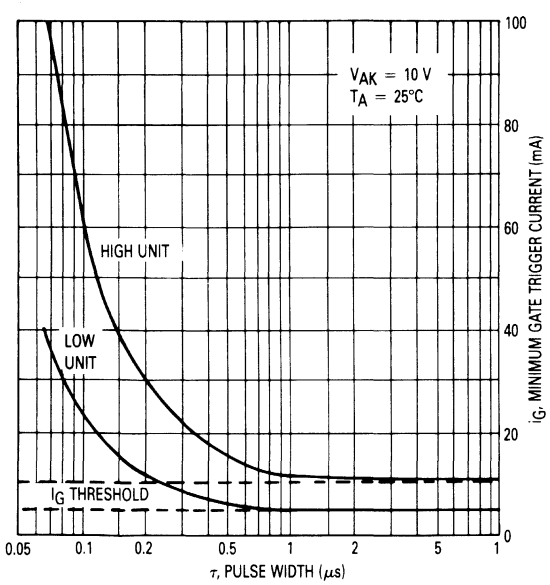


Figure 3.3(a). Typical Variation of Minimum Gate Current Required to Trigger

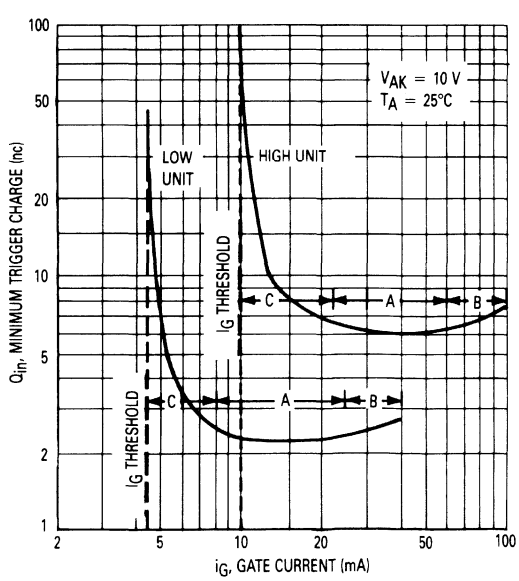


Figure 3.3(b). Variation of Charge versus Gate Current

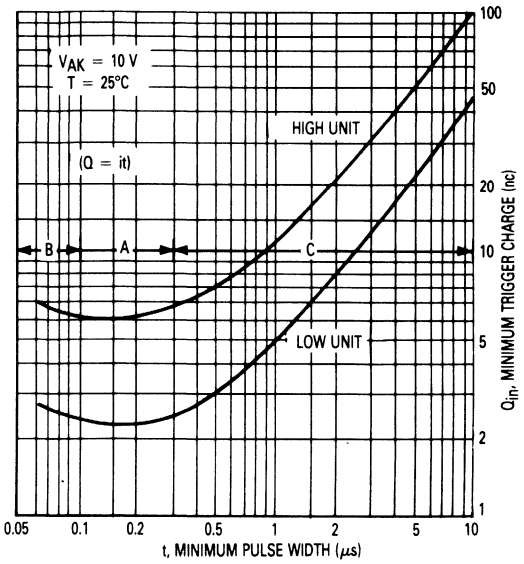


Figure 3.3(c). Variation of Charge versus Minimum Pulse Width

The charge characteristic curves can be explained qualitatively by the variation of current amplification (α_T) with respect to emitter current. A typical variation of α_1 and α_2 for a thyristor is shown in Figure 3.4(a). From Figure 3.4(a), it can be deduced that the total current amplification factor, $\alpha_T = \alpha_1 + \alpha_2$, has a characteristic curve as shown in Figure 3.4(b). (The data does not correspond to the data of Figure 3.3 — they are taken for different types of devices.)

The gate current levels in region A of Figure 3.3 correspond to the emitter (or anode) currents for which the slope of the α_T curve is steepest (Figure 3.4(b)). In region A the rate that α_T builds up with respect to changes of I_E (or I_A) is high, little charge is lost by recombination, and therefore, a minimum charge is required for turn-on.

In region C of Figure 3.3, lower gate current corresponds to small I_E (or I_A) for which the slope of α_T, as well as α_T itself, is small. It takes a large change in I_E (or I_A) in order to build up α_T. In this region, a lot of the charge supplied through the gate is lost by recombination. The charge required for turn-on increases markedly as the gate current is decreased to the threshold level. Below this threshold, the device will not turn on regardless of how long the pulse width becomes. At this point, the slope of α_T is equal to zero; all of the charge supplied is lost completely in recombination or drained out through gate-cathode shunt resistance. A qualitative analysis of variation of charge with pulse width at region A and C is discussed in Appendix II.

In region B, as the gate current level gets higher and the pulse width smaller, there are two effects that contribute to an increasing charge requirement to trigger-on the device: (1) the decreasing slope of α_T and, (2) the transit time effect. As mentioned previously, it takes some multiple of the transit time for turn-on. As the gate pulse width decreases to N ($t_{N1} + t_{P2}$) or less, (where N is a positive real number, t_{N1} = transit time of base N_1, and

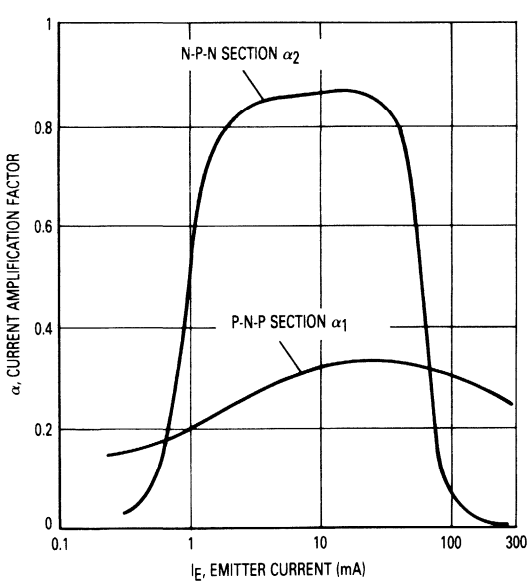


Figure 3.4(a). The Variation of α_1 and α_2 with Emitter Current for the Two Sections of Two Typical Silicon Controlled Rectifiers

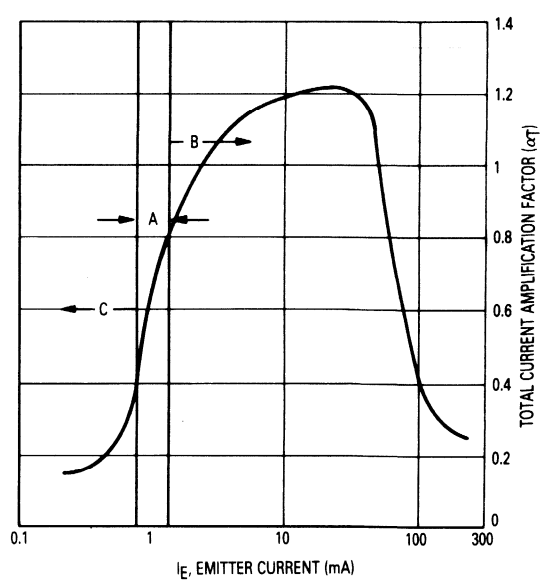


Figure 3.4(b). Typical Variation of α_T versus Emitter Current

t_{P2} = transit time of base P2) the amount of current required to turn-on the device should be large enough to flood the gate to cathode junction nearly instantaneously with a charge which corresponds to I_E (or I_A) high enough to give $\alpha_T > 1$.

CAPACITANCE CHARGE TRIGGERING

Using a gate trigger circuit as shown in Figure 3.5, the charge required for turn-on increases with the value of capacitance used as shown in Figure 3.7. Two reasons may account for the increasing charge characteristics:

1) An effect due to threshold current.
2) An effect due to variation of gate spreading resistance.

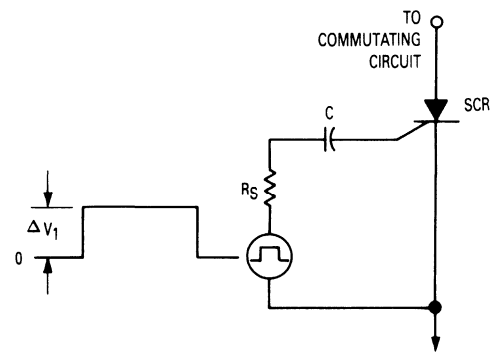


Figure 3.5. Gate Circuit of Capacitance Charge Triggering

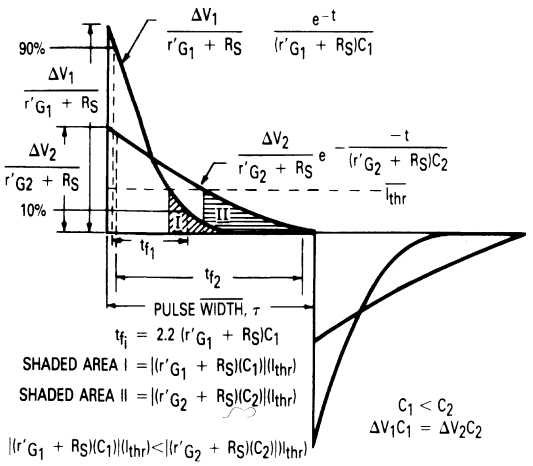


Figure 3.6. Gate Current Waveform in Capacitance Charge Triggering

Consider the gate current waveform in Figure 3.6; the triggering pulse width is made large enough such that $\tau >> t_{fi}$; the threshold trigger current is shown as I_{thr}. All of the charge supplied at a transient current level less than I_{thr} is lost by recombination, as shown in the shaded regions.

The gate spreading resistance (r'_G) of the gate junction varies inversely with peak current; the higher the peak current, the smaller the gate spreading resistance. Variation of gate spreading resistance measured by the method of Time Domain Reflectometry is plotted in Figure 3.8.

From the data of Figure 3.7, it is clear that for larger values of capacitance a lower voltage level is required for turn-on. The peak current of the spike in Figure 3.6 is given by $I_{pk} = \frac{\Delta V}{R_s + r'_G}$; the smaller ΔV, the smaller I_{pk}. Smaller I_{pk} in turn yields large r'_G, so that r'_G is dependent on the value of capacitance used in capacitance charge triggering. This reasoning is confirmed by measuring the fall time of the gate trigger voltage and calculating the transient gate spreading resistance, r'_G, from: $R_s + r'_G = \frac{t_f}{2.2\,C}$. Results are plotted in Figure 3.9.

As expected, r'_G increases with increasing values of capacitance used. Referring back to Figure 3.6, for the same amount of charge ($C\,\Delta V$), the larger the $(R_s + r'_G)C$ time constant of the current spike, the more charge under the threshold level is lost in recombination. Increasing the value of C will increase the time constant more rapidly than if r'_G were invariant. Therefore, increasing the value of C should increase the charge lost as shown in Figure 3.7. Note that a two order of magnitude increase in capacitance increased the charge by less than 3:1.

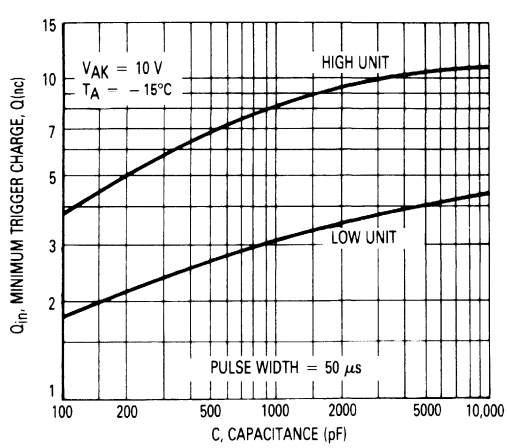


Figure 3.7. Variation of Trigger Charge versus Capacitance Used

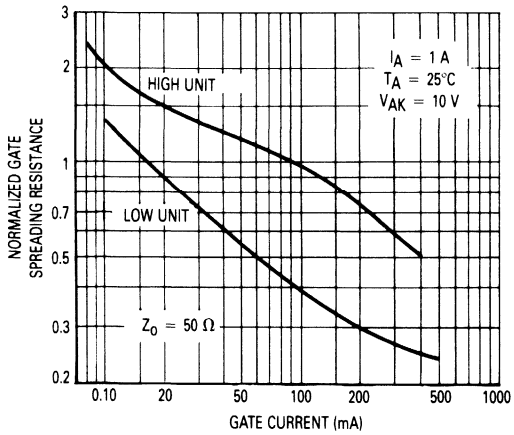


Figure 3.8. Variation of Gate Spreading Resistance versus Gate Peak Current

EFFECT OF TEMPERATURE

The higher the temperature, the less charge required to turn on the device, as shown in Figure 3.10. At the range of temperatures where the SCR is operated the life time of minority carriers increases with temperature; therefore less charge into the gate is lost in recombination.

As analyzed in Appendix II, there are three components of charge involved in gate triggering: (1) Q_r, charge lost in recombination, (2) Q_{dr}, charge drained out through the built-in gate-cathode shunt resistance, (3) Q_{tr}, net charge for triggering. All of them are temperature dependent. Since the temperature coefficient of voltage across a p-n junction is small, Q_{dr} may be considered invariant of temperature. At the temperature range of operation, the temperature is too low to give rise to significant impurity gettering, lifetime increases with temperature causing Q_r to decrease with increasing temperature. Also, Q_{tr} decreases with increasing temperature because at a constant current the α_T of the device in the blocking state increases with temperature;[7] in other words, to attain $\alpha_T = 1$ at an elevated temperature, less anode current, hence gate current [see equation (3) of Appendix I], is needed; therefore, Q_{tr} decreases. The input charge, being equal to the sum of Q_{tr}, Q_r, and Q_{dr}, decreases with increasing temperature.

The minimum current trigger charge decreases roughly exponentially with temperature. Actual data taken on an MCR729 deviate somewhat from exponential trend (Figure 3.10). At higher temperatures, the rate of decrease is less; also for different pulse widths the rates of decrease of Q_{in} are different; for large pulse widths the recombination charge becomes more significant than that of small pulse widths. As the result, it is expected and Figure 3.10 shows that Q_{in} decreases more rapidly with temperature at high pulse widths. These effects are analyzed in Appendix II [equation (10)]. The theory and experiment agree reasonably well.

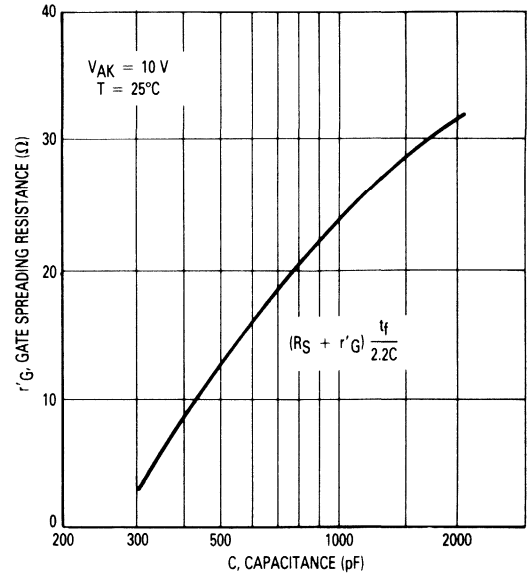


Figure 3.9. Variation of Transient Base Spreading Resistance versus Capacitance

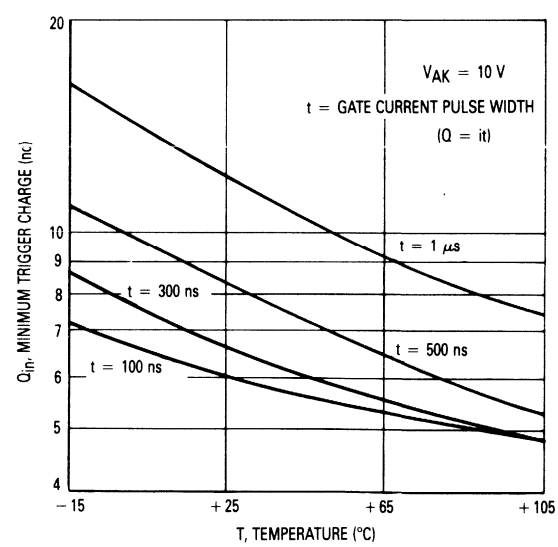


Figure 3.10. Variation of Q versus Temperature

EFFECT OF BLOCKING VOLTAGE

An SCR is an avalanche mode device; the turn-on of the device is due to multiplication of carriers in the middle collector junction. The multiplication factor is given by the empirical equation

$$M = \frac{1}{1 - (\frac{V}{V_B})^n} \qquad (6)$$

where

M ≡ Multiplication factor

V ≡ Voltage across the middle "collector" junction (voltage at which the device is blocking prior to turn-on)

V_B ≡ Breakdown voltage of the middle "collector" junction

n ≡ Some positive number

Note as V is increased, M also increases and in turn α increases (the current amplification factor $\alpha = \gamma\delta\beta M$ where γ ≡ Emitter efficiency, β ≡ Base transport factor, and δ ≡ Factor of recombination).

The larger the V, the larger is α_T. It would be expected for the minimum gate trigger charge to decrease with increasing V. Experimental results show this effect (see Figure 3.11). For the MCR729, the gate trigger charge is only slightly affected by the voltage at which the device is blocking prior to turn-on; this reflects that the exponent, n, in equation (6) is small.

EFFECT OF GATE CIRCUIT

As mentioned earlier, to turn on the device, the total amplification factor must be greater than unity. This means that if some current is being drained out of the gate which bleeds the regeneration current, turn-on will be affected. The higher the gate impedance, the less the gate trigger charge. Since the regenerative current prior to turn-on is small, the gate impedance only slightly affects the required minimum trigger charge; but in the case of over-driving the gate to achieve fast switching time, the gate circuit impedance will have noticeable effect.

EFFECT OF INDUCTIVE LOAD

The presence of an inductive load tends to slow down the change of anode current with time, thereby causing the required charge for triggering to increase with the value of inductance. For dc or long pulse width current triggering, the inductive load has little effect, but its effect increases markedly at short pulse widths, as shown in Figure 3.12. The increase in charge occurs because at short pulse widths, the trigger signal has decreased to a negligible value before the anode current has reached a level sufficient to sustain turn-on.

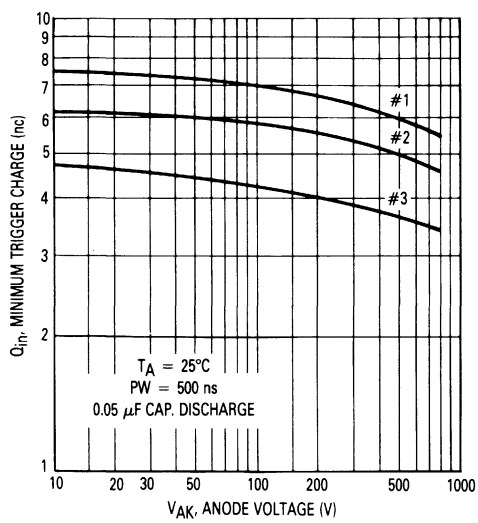


Figure 3.11. Variation of Current Trigger Charge versus Blocking Voltage Prior to Turn-On

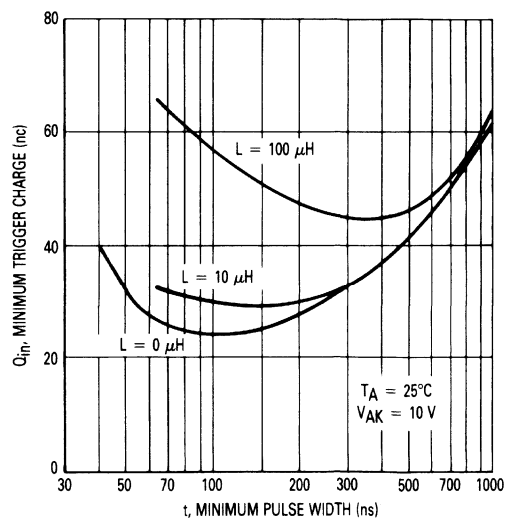


Figure 3.12. Effect of Inductance Load on Triggering Charge

USING NEGATIVE BIAS AND SHUNTING

Almost all SCR's exhibit some degree of turn-off gain. At normal values of anode current, negative gate current will not have sufficient effect upon the internal feedback loop of the device to cause any significant change in anode current. However, it does have a marked effect at low anode current levels; it can be put to advantage by using it to modify certain device parameters. Specifically, turn-off time may be reduced and hold current may be increased. Reduction of turn-off time and increase of hold current are useful in such circuits as inverters or in full-wave phase control circuits in which inductance is present.

Negative gate current may, of course, be produced by use of an external bias supply. It may also be produced by taking advantage of the fact that during conduction the gate is positive with respect to the cathode and providing an external conduction path such as a gate-to-cathode resistor. All Motorola SCR's, with the exception of sensitive gate devices, are constructed with a built in gate-to-cathode shunt, which produces the same effect as negative gate current. Further change in characteristics can be produced by use of an external shunt. Shunting does not produce as much of a change in characteristics as does negative bias, since the negative gate current, even with an external short circuit, is limited by the lateral resistance of the base layer. When using external negative bias the current must be limited, and care must be taken to avoid driving the gate into the avalanche region.

The effects of negative gate current are not shown on the device specification sheets. The curves in Figure 3.13 represent measurements made on a number of SCRs, and should therefore not be considered as spec limits. They do, however, show definite trends. For example, all of the SCRs showed an improvement in turn-off time of about one-third by using negative bias up to the point where no further significant improvement was obtained.

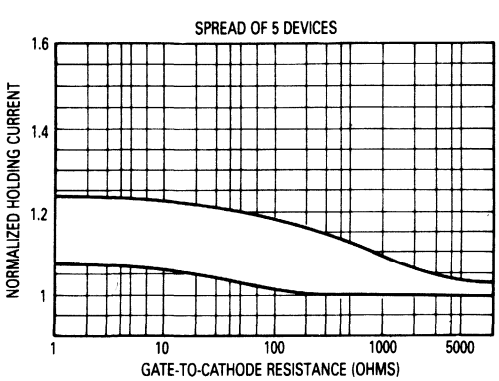


Figure 3.13(a). 2N4199 Normalized Holding Current versus Gate-to-Cathode Resistance

The increase in hold current by use of an external shunt resistor ranged typically between 5 and 75 percent, whereas with negative bias, the range of improvement ran typically between 2-1/2 and 7 times the open gate value. Note that the holding current curves are normalized and are referred to the open gate value.

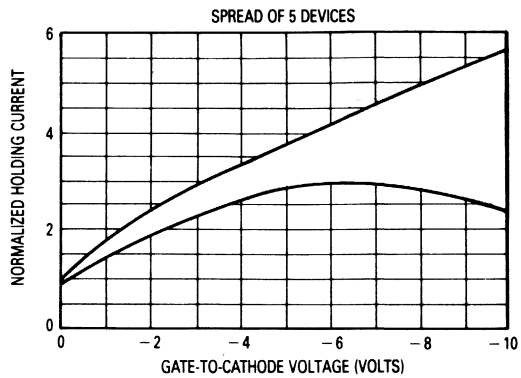


Figure 3.13(b). 2N4199 Normalized Holding Current versus Gate-to-Cathode Voltage

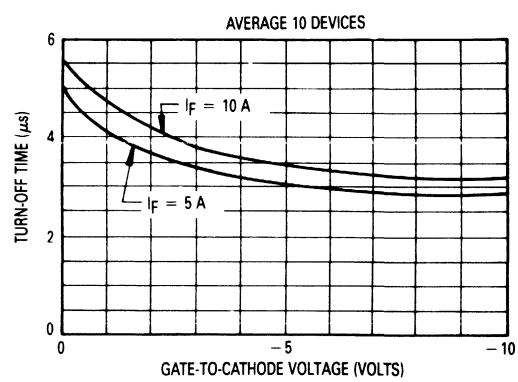


Figure 3.13(c). 2N4199 Turn-Off Time versus Bias

REDUCING di/dt — EFFECT FAILURES

Figure 3.14 shows a typical SCR structural cross section (not to scale). Note that the collector of transistor 1 and the base of transistor 2 are one and the same layer. This is also true for the collector of transistor 2 and the base of transistor 1. Although for optimum performance as an SCR the base thicknesses are great compared to a normal transistor, nevertheless, base thickness is still small compared to the lateral dimensions. When applying positive bias to the gate, the transverse base resistance, spreading resistance or r_b' will cause a lateral voltage drop which

will tend to forward bias those parts of the transistor 1 emitter-junction closest to the base contact (gate) more heavily, or sooner than the portions more remote from the contact area. Regenerative action, consequently will start in an area near the gate contact, and the SCR will turn on first in this area. Once on, conduction will propagate across the entire junction.

LAYER	T_2	T_1
NO. 4		(E)
NO. 3	(C)	(B)
NO. 2	(B)	(C)
NO. 1	(E)	

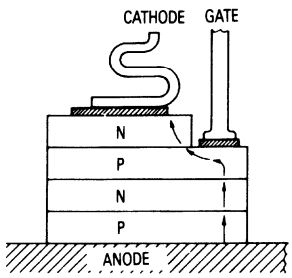


Figure 3.14(a). Construction of Typical SCR

TYPICAL SCR CONSTRUCTION SHOWING THE DIE IN PROPER SCALE . . .

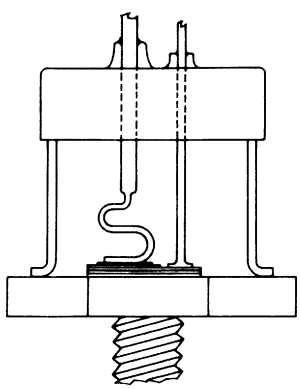


Figure 3.14 (b)

The phenomenon of di/dt failure is related to the turn-on mechanism. Let us look at some of the external factors involved and see how they contribute. Curve 3.15(a) shows the fall of anode-to-cathode voltage with time. This fall follows a delay time after the application of the gate bias. The delay time and fall time together are called turn-on time, and, depending upon the device, will take anywhere from tens of nanoseconds up to a few microseconds. The propagation of conduction across the entire junction requires a considerably longer time. The time required for propagation or equalization of conduction is represented approximately by the time required for the anode-to-cathode voltage to fall from the 10 percent point to its steady state value for the particular value of anode current under consideration (neglecting the change due to temperature effects). It is during the interval of time between the start of the fall of anode-to-cathode voltage and the final equalization of conduction that the SCR is most susceptible to damage from excessive current.

Let us superimpose a current curve (b) on the anode-to-cathode voltage versus time curve to better understand this. If we allow the current to rise rapidly to a high value we find by multiplying current and voltage that the instantaneous dissipation curve (c) reaches a peak which may be hundreds of times the steady state dissipation level for the same value of current.

At the same time it is important to remember that the dissipation does not take place in the entire junction, but is confined at this time to a small volume. Since temperature is related to energy per unit volume, and since the energy put into the device at high current levels may be very large while the volume in which it is concentrated is very small, very high spot temperatures may be achieved. Under such conditions, it is not difficult to attain temperatures which are sufficient to cause localized melting of the device.

Even if the peak energy levels are not high enough to be destructive on a single-shot basis, it must be realized that since the power dissipation is confined to a small area, the power handling capabilities of the device are lessened. For pulse service where a significant percentage of the power per pulse is dissipated during the fall-time interval, it is not acceptable to extrapolate the steady state power dissipation capability on a duty cycle basis to obtain the allowable peak pulse power.

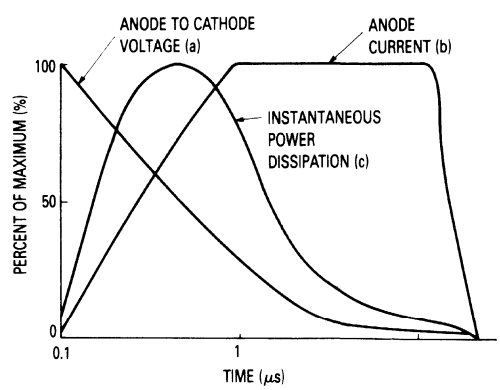


Figure 3.15. Typical Conditions — Fast-Rise, High Current Pulse

The final criterion for the limit of operation is junction temperature. For reliable operation the instantaneous junction temperature must always be kept below the maximum junction temperature as stated on the manufacturer's data sheet. Some SCR data sheets at present include information on how to determine the thermal response of the junction to current pulses. This information is not useful, however, for determining the limitations of the device before the entire junction is in conduction, because they are based on measurements made with the entire junction in conduction.

At present, there is no known technique for making a reasonably accurate measurement of junction temperature in the time domain of interest. Even if one were to devise a method for switching a sufficiently large current in a short enough time, one would still be faced with the problem of charge storage effects in the device under test masking the thermal effects. Because of these and other problems, it becomes necessary to determine the device limitations during the turn-on interval by destructive testing. The resultant information may be published in a form such as a maximum allowable current versus time, or simply as a maximum allowable rate of rise of anode current (di/dt).

Understanding the di/dt failure mechanism is part of the problem. To the user, however, a possible cure is infinitely more important. There are three approaches that should be considered.

Because of the lateral base resistance the portion of the gate closest to the gate contact is the first to be turned on because it is the first to be forward biased. If the minimum gate bias to cause turn-on of the device is used, the spot in which conduction is initiated will be smallest in size. By increasing the magnitude of the gate trigger pulse to several times the minimum required, and applying it with a very fast rise time, one may considerably increase the size of the spot in which conduction starts. Figure 3.16(a) illustrates the effect of gate drive on voltage fall time and Figure 3.16(b) shows the improvement in instantaneous dissipation. We may conclude from this that overdriving the gate will improve the di/dt capabilities of the device, and we may reduce the stress on the device by doing so.

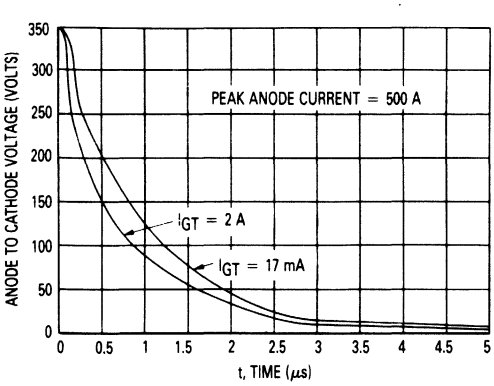


Figure 3.16(a). Effect of Gate Drive on Fall Time

A very straightforward approach is to simply slow down the rate of rise of anode current to insure that it stays within the device ratings. This may be done simply by adding some series inductance to the circuit.

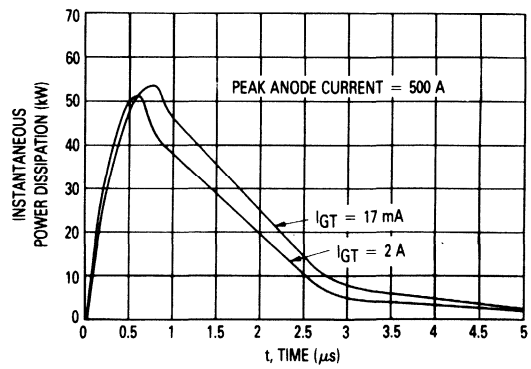


Figure 3.16(b). Effect of Gate Drive On Turn-On Dissipation

If the application should require a rate of current rise beyond the rated di/dt limit of the device, then another approach may be taken. The device may be turned on to a relatively low current level for a sufficient time for a large part of the junction to go into conduction; then the current level may be allowed to rise much more rapidly to very high levels. This might be accomplished by using a delay reactor as shown in Figure 3.17. Such a reactor would be wound on a square loop core so that it would have sharp saturation characteristic and allow a rapid current rise. It is also possible to make use of a separate saturation winding. Under these conditions, if the delay is long enough for the entire junction to go into conduction, the power handling capabilities of the device may be extrapolated on a duty cycle basis.

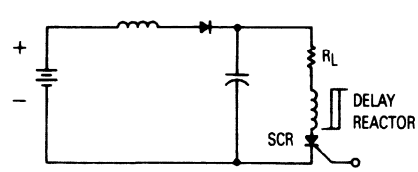


Figure 3.17. Typical Circuit Use of a Delay Reactor

WHY AND HOW TO SNUB THYRISTORS

Inductive loads (motors, solenoids, etc.) present a problem for the power triac because the current is not in phase with the voltage. An important fact to remember is that since a triac can conduct current in both directions, it has only a brief interval during which the sine wave current is passing through zero to recover and revert to its blocking state. For inductive loads, the phase shift between voltage and current means that at the time the current of the power handling triac falls below the holding current and the triac ceases to conduct, there exists a certain voltage which must appear across the triac. If this voltage appears too rapidly, the triac will resume con-

duction and control is lost. In order to achieve control with certain inductive loads, the rate of rise in voltage (dv/dt) must be limited by a series RC network placed in parallel with the power triac as shown in Figure 3.18. The capacitor C_S will limit the dv/dt across the triac.

The resistor R_S is necessary to limit the surge current from C_S when the triac conducts and to damp the ringing of the capacitance with the load inductance L_L. Such an RC network is commonly referred to as a "snubber."

Figure 3.19 shows current and voltage waveforms for the power triac. Commutating dv/dt for a resistive load is typically only 0.13 V/μs for a 240 V, 50 Hz line source and 0.063 V/μs for a 120 V, 60 Hz line source. For inductive loads the "turn-off" time and commutating dv/dt stress are more difficult to define and are affected by a number of variables such as back EMF of motors and the ratio of inductance to resistance (power factor). Although it may appear from the inductive load that the rate or rise is extremely fast, closer circuit evaluation reveals that the commutating dv/dt generated is restricted to some finite value which is a function of the load reactance L_L and the device capacitance C but still may exceed the triac's critical commutating dv/dt rating which is about 50 V/μs. It is generally good practice to use an RC snubber network across the triac to limit the rate of rise (dv/dt) to a value below the maximum allowable rating. This snubber network not only limits the voltage rise during commutation but also suppresses transient voltages that may occur as a result of ac line disturbances.

There are no easy methods for selecting the values for R_S and C_S of a snubber network. The circuit of Figure 3.18 is a damped, tuned circuit comprised of R_S, C_S, R_L and L_L, and to a minor extent the junction capacitance of the triac. When the triac ceases to conduct (this occurs every half cycle of the line voltage when the current falls below the holding current), the triac receives a step impulse of line voltage which depends on the power factor of the load. A given load fixes R_L and L_L; however, the circuit designer can vary R_S and C_S. Commutating dV/dt can be lowered by increasing C_S while R_S can be increased to decrease resonant "over ringing" of the tuned circuit.

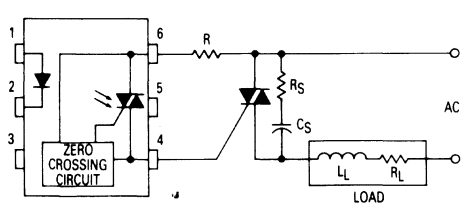


Figure 3.18. Triac Driving Circuit — with Snubber

BASIC CIRCUIT ANALYSIS

Figure 3.20 shows an equivalent circuit used for analysis, in which the triac has been replaced by an ideal switch. When the triac is in the blocking or non-conducting state, represented by the open switch, the circuit is a standard RLC series network driven by an ac voltage source. The following differential equation can be obtained by summing the voltage drops around the circuit:

$$(R_L + R_S)\, i(t) + L\frac{di(t)}{dt} + \frac{q_C(t)}{C_S} = V_M \sin(\omega t + \phi) \qquad (2)$$

in which i(t) is the instantaneous current after the switch opens, $q_C(t)$ is the instantaneous charge on the capacitor, V_M is the peak line voltage, and ϕ is the phase angle by which the voltage leads the current prior to opening of the switch. After differentiation and rearrangement, the equation becomes a standard second-order differential equation with constant coefficients.

With the imposition of the boundary conditions that $i(o) = 0$ and $q_C(o) = 0$ and with selected values for R_L, L, R_S and C_S, the equation can be solved, generally by the use of a computer. Having determined the magnitude

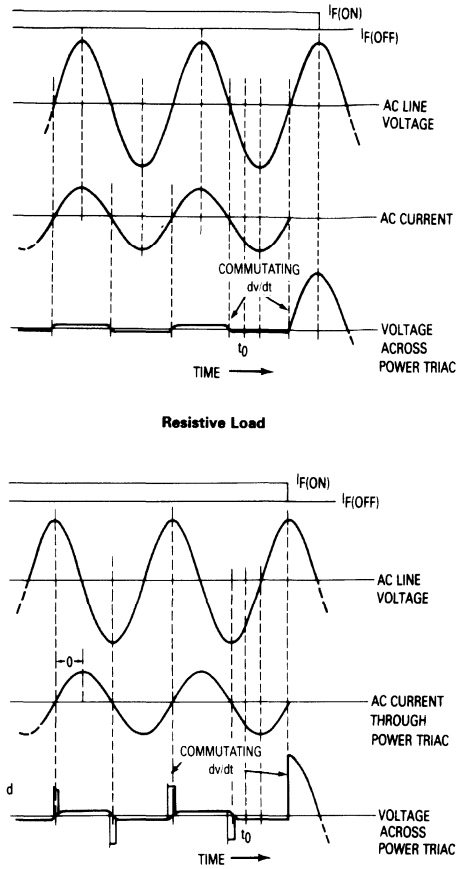


Figure 3.19. Current and Voltage Waveforms During Commutation

and time of occurrence of the peak voltage across the thyristor, it is then possible to calculate the values and times of the voltages at 10% and 63% of the peak value. This is necessary in order to compute the dv/dt stress as defined by the following equation:

$$\frac{dv}{dt} = \frac{V_2 - V_1}{t_2 - t_1}$$

where V_1 and t_1 are the voltage and time at the 10% point and V_2 and t_2 are the voltage and time at the 63% point.

Solution of the differential equation for assumed load conditions will give the circuit designer a starting point for selecting R_S and C_S.

Because the design of a snubber is contingent on the load, it is almost impossible to simulate and test every possible combination under actual operating conditions. It is advisable to measure the peak amplitude and rate of rise of voltage across the triac by use of an oscilloscope, then make the final selection of R_S and C_S experimentally. Additional comments about circuit values for SCRs and Triacs are made in Chapter 6.

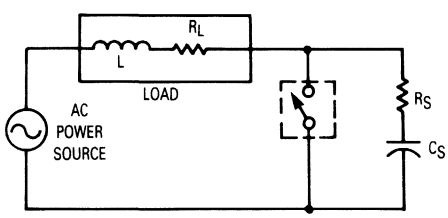


Figure 3.20. Equivalent Circuit used for Analysis

PROTECTING SENSITIVE GATE SCRs

In applications of sensitive gate SCRs such as the Motorola 2N6236, the gate-cathode resistor, R_{GK} (Figure 3.21) is an important factor. Its value affects, in varying degrees, such parameters as I_{GT}, V_{DRM}, dv/dt, I_H, leakage current, and noise immunity.

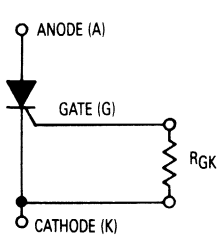


Figure 3.21. Gate-Cathode Resistor, R_{GK}

SCR CONSTRUCTION

The initial step in making an SCR is the creation, by diffusion, of P-type layers in N-type silicon base material. Prior to the advent of the all-diffused SCR, the next step was to form the gate-cathode P-N junction by alloying in a gold-antimony foil. This produced a silicon P-N junction of the regrown type over most of the junction area. However, a resistive rather than semiconductor junction would form where the molten alloy terminated at the surface. This formed an internal R_{GK}, looking in at the gate-cathode terminals, that reduced the "sensitivity" of the SCR.

Modern practice is to produce the gate-cathode junction by masking and diffusing, a much more controllable process. It produces a very clean junction over the entire junction area with no unwanted resistive paths. Good dv/dt performance by larger SCRs, however, requires resistive paths distributed over the junction area. These are diffused in as emitter shorts and naturally desensitize the device. Smaller SCRs may rely on an external R_{GK} for adequate dv/dt performance; an all-diffused SCR without emitter shorts will have sensitive gate characteristics. Figure 3.22(a) shows a cross-section of the simple construction found in small sensitive gate SCRs. Figure 3.22(b) depicts shorted emitter construction.

The sensitive gate SCR, therefore, is an all-diffused design with no emitter shorts. It has a very high impedance path in parallel with the gate-cathode P-N diode; the better the process is the higher this impedance, until a very good device cannot block voltage in the forward direction without an external R_{GK}. This is so simple because thermally generated leakage currents flowing from the anode into the gate junction are sufficient to turn on the SCR. The value for R_{GK} is usually one kilohm and its presence and value affects many other parameters.

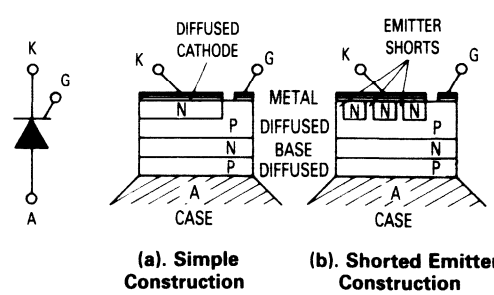


Figure 3.22. Sensitive Gate SCR Construction

FORWARD BLOCKING VOLTAGE AND CURRENT, V_{DRM} AND I_{DRM}

The 2N6236 family is specified to have an I_{DRM}, or anode-to-cathode leakage current, of less than 200 μA at maximum operating junction temperature and rated V_{DRM}. This leakage current increases if R_{GK} is omitted and, in fact, the device may well be able to regenerate and turn on. Tests were run on several 2N6239 devices to establish the dependency of the leakage current on R_{GK} and to determine its relationship with junction tem-

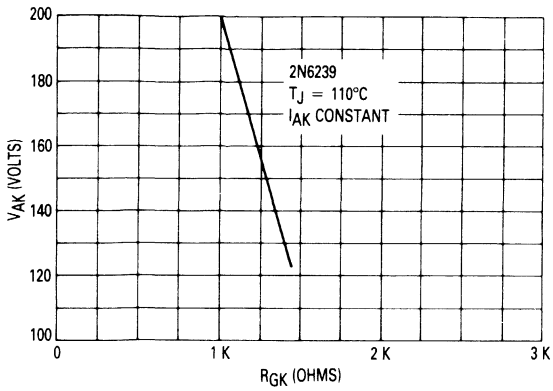


Figure 3.23(a). V_{AK} versus R_{GK} (Typical) for Constant Leakage Current

perature, T_J, and forward voltage V_{AK} (Figure 3.23a).

Figure 3.23(d) is a plot of V_{AK}, forward voltage, versus R_{GK} taken at the maximum rated operating junction temperature of 110°C. With each device the leakage current, I_{AK}, is set for a V_{AK} of 200 V, then V_{AK} reduced and R_{GK} varied to re-establish the same leakage current. The plot shows that the leakage current is *not* strongly voltage dependent or, conversely, R_{GK} may *not* be increased for derate.

While the leakage current is not voltage dependent, it is very temperature dependent. The plot in Figure 3.23(b) of T_J, junction temperature, versus R_{GK} taken at V_{DRM}, the maximum forward blocking voltage shows this dependence. For each device (2N6329 again) the leakage current, I_{AK}, was measured at the maximum operating junction temperature of 110°C, then the junction temperature was reduced and R_{GK} varied to re-establish that same leakage current. The plot shows that the leakage current is strongly dependent on junction temperature. Conversely R_{GK} may be increased for derated temperature.

To summarize, the leakage current in a sensitive gate SCR is much more temperature sensitive than voltage sensitive. Operation at lower junction temperatures allows an increase in the gate-cathode resistor which makes the SCR-resistor combination more "sensitive."

RATE-OF-RISE OF ANODE VOLTAGE, dv/dt

An SCR's junctions exhibit capacitance due to the separation of charge when the device is in a blocking state. If an SCR is subjected to forward dv/dt, this capacitance can couple sufficient current into the SCR's gate to turn it on, as shown in Figure 3.23(c). R_{GK} acts as a diversionary path for the dv/dt current. (In larger SCRs, where the lateral gate resistance of the device limits the influence of R_{GK}, this path is provided by the resistive emitter shorts mentioned previously.) The gate-cathode resistor, then, might be expected to have some effect on the dv/dt performance of the SCR. Using the 2N6241 as an example, a plot of dv/dt versus R_{GK}, in Figure 3.23(d), shows a very strong relationship indeed. If R_{GK} is increased, dv/dt performance suffers and if R_{GK} is reduced, the dv/dt performance improves. Reverse biasing the gate also improves dv/dt performance as might be expected and, on the 2N6241 the improvement is by a factor of about 50 when the gate is reverse biased by one volt.

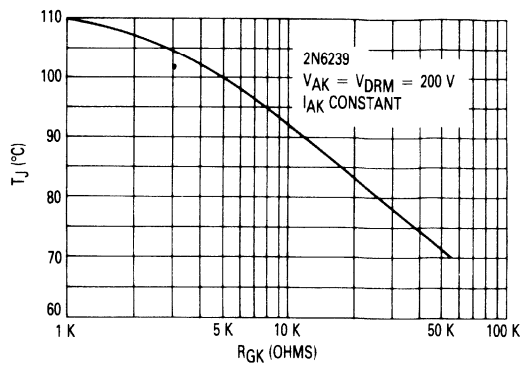


Figure 3.23(b). T_J versus R_{GK} (Typical) for Constant Leakage Current

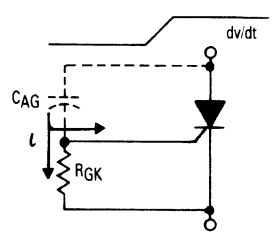


Figure 3.23(c). dv/dt Firing of an SCR

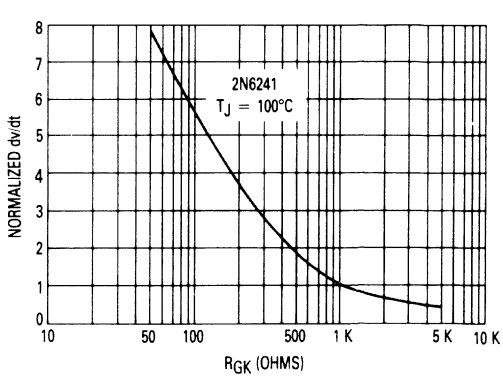


Figure 3.23(d). dv/dt versus R_{GK} (Typical)

GATE CURRENT, I_{GT}

The total gate current that a gating circuit must supply is the sum of the current that the device itself requires to fire and the current flowing to circuit ground through R_{GK}, as shown in Figure 3.24. I_{GT}, the current required by the device so that it may fire, is usually specified by the device manufacturer as a maximum at some temperature (for the 2N6236 series it is 500 μA maximum at −40°C). The current flowing through R_{GK} is defined by the resistor value and by the *gate-to-cathode voltage* that the SCR needs to fire. This is 1 V maximum at −40°C for the 2N6236 series, for example.

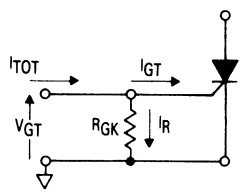


Figure 3.24. SCR and R_{GK} "Gate" Currents

The gate-cathode junction is a P-N silicon junction and thus has roughly the same temperature coefficient as a silicon diode, −2 mV/°C. Figure 3.25 is a typical plot of V_{GT} versus temperature for sensitive gate SCRs.

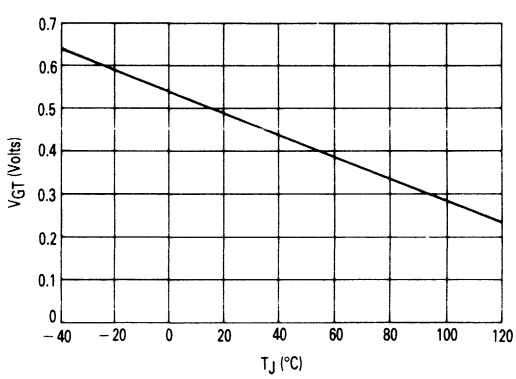


Figure 3.25. V_{GT} versus T_J (Typical)

GATE CURRENT, $I_{GT(min)}$

SCR manufacturers sometimes get requests for a sensitive-gate SCR specified with an $I_{GT(min)}$, that is, the maximum gate current that will *not* fire the device. This requirement conflicts with the basic function of a sensitive gate SCR, which is to fire at zero or very low gate current, $I_{GT(max)}$. Production of devices with a measurable $I_{GT(min)}$ is at best difficult and deliveries can be sporadic!

One reason for an $I_{GT(min)}$ requirement might be some measurable off-state gating circuit leakage current, perhaps the collector leakage of a driving transistor. Such current can readily be bypassed by a suitably chosen R_{GK}. The V_{GT} of the SCR at the temperature in question can be estimated from Figure 3.25, an Ohm's Law calculation made, and the resistor installed to define this "won't fire" current. This is a repeatable design well in the control of the equipment designer.

HOLDING CURRENT, I_H

The holding current of an SCR is the minimum anode current required to maintain the device in the on state. It is usually specified as a maximum for a series of devices (for instance, 5 mA maximum at 25°C for the 2N6236 series). A particular device will turn off somewhere between this maximum and zero anode current and there is perhaps a 20-to-1 spread in each lot of devices.

Figure 3.26 shows the holding current increasing with decreasing R_{GK} as the resistor siphons off more and more of the regeneratively produced gate current when the device is in the latched condition.

NOISE IMMUNITY

Changes in electromagnetic and electrostatic fields coupled into wires or printed circuit lines can trigger these sensitive devices, as can logic circuit glitches. The result is more serious than with a transistor since an SCR will latch on. Careful wire harness design (twisted pairs and adequate separation from high-power wiring) and printed circuit layout (gate and return runs adjacent to one another) can minimize potential problems. Another help is the gate-cathode resistor since, with a one-kilohm resistor, 100 μA to 1 mA of noise current is required to generate sufficient voltage to fire the device. To serve this purpose R_{GK} must be mounted right at the gate-cathode terminals of the SCR.

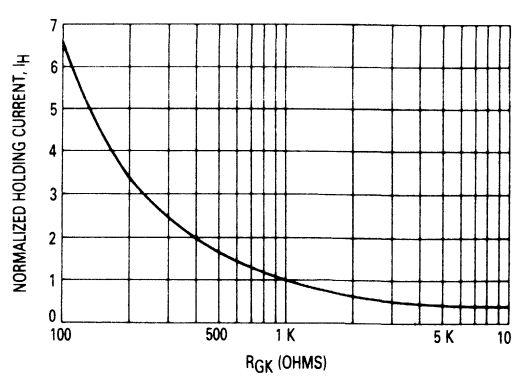


Figure 3.26. I_H versus R_{GK} (Typical)

DRIVERS: THE MOC3011 NON-ZERO CROSSING TRIAC DRIVER

The MOC3011 non-zero crossing triac driver consists of a gallium arsenide infrared LED optically exciting a silicon detector chip, which is especially designed to drive triacs controlling loads on a 115 Vac power line. The detector chip is a complex device which functions in much the same manner as a small triac, generating the signals necessary to drive the gate of a larger triac. The MOC3011 shows a low power exciting signal to drive a high power load with a very small number of components, and at the same time provides practically complete isolation of the driving circuitry from the power line.

The construction of the MOC3011 follows the same highly successful coupler technology used in Motorola's broad line of plastic couplers (Figure 3.27). The planar lead frame with a plastic "dome" undermold provides a stable dielectric capable of sustaining 7.5 kV between the input and output sides of the device. The detector chip is passivated with silicon nitride and uses Motorola's annular ring to maintain stable breakdown parameters.

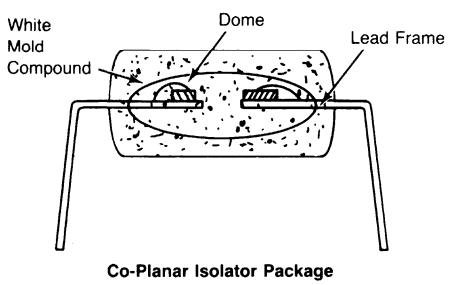


Figure 3.27. Motorola "Dome" Coupler Package

BASIC ELECTRICAL DESCRIPTION

The GaAs LED has nominal 1.3 V forward drop at 10 mA and a reverse breakdown voltage greater than 3 V. The maximum current to be passed through the LED is 50 mA.

The detector has a minimum blocking voltage of 250 Vdc in either direction in the off state. In the on state, the detector will pass 100 mA in either direction with less than 3 V drop across the device. Once triggered into the on (conducting) state, the detector will remain there until the current drops below the holding current (typically 100 μA) at which time the detector reverts to the off (non-conducting) state. The detector may be triggered into the on state by exceeding the forward blocking voltage, by voltage ramps across the detector at rates exceeding the static dv/dt rating, or by photons from the LED. The LED is guaranteed by the specifications to trigger the detector into the on state when 10 mA or more is passed through the LED. A similar device, the MOC3010, has exactly the same characteristics except it requires 15 mA to trigger.

Since the MOC3011 looks essentially like a small optically triggered triac, we have chosen to represent it as shown on Figure 3.28.

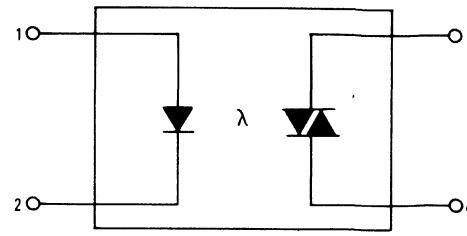


Figure 3.28. Schematic Representation of MOC3011 and MOC3010

TRIAC DRIVING REQUIREMENTS

Figure 3.29 shows a simple triac driving circuit using the MOC3011. The maximum surge current rating of the MOC3011 sets the minimum value of R1 through the equation:

$$R1(min) = V_{in(pk)}/1.2\ A$$

If we are operating on the 115 Vac nominal line voltage, $V_{in(pk)} = 180$ V, then

$$R1(min) = V_{in(pk)}/1.2\ A = 150 \text{ ohms.}$$

In practice, this would be a 150 or 180 ohm resistor. If the triac has $I_{GT} = 100$ mA and $V_{GT} = 2$ V, then the voltage V_{in} necessary to trigger the triac will be given by $V_{inT} = R1 \cdot I_{GT} + V_{GT} + V_{TM} = 20$ V.

RESISTIVE LOADS

When driving resistive loads, the circuit of Figure 3.29 may be used. Incandescent lamps and resistive heating elements are the two main classes of resistive loads for which 115 Vac is utilized. The main restriction is that the triac must be properly chosen to sustain the proper inrush loads. Incandescent lamps can sometimes draw a peak current known as "flashover" which can be extremely high, and the triac should be protected by a fuse or rated high enough to sustain this current.

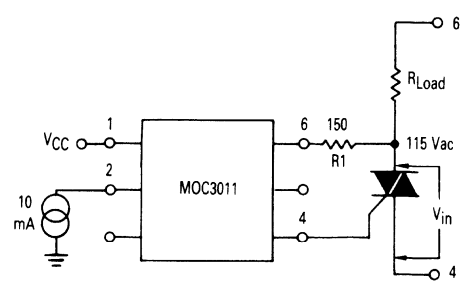


Figure 3.29. Simple Triac Gating Circuit

LINE TRANSIENTS — STATIC dv/dt

Ocassionally transient voltage disturbance on the ac line will exceed the static dv/dt rating of the MOC3011. In this case, it is possible that the MOC3011 and the associated triac will be triggered on. This is usually not a problem, except in unusually noisy environments, because the MOC3011 and its triac will commute off at the next zero crossing of the line voltage, and most loads are not noticeably affected by an occasional single half-cycle of applied power. See Figure 3.31 for typical dv/dt versus temperature curves.

INDUCTIVE LOADS — COMMUTATING dv/dt

Inductive loads (motors, solenoids, magnets, etc.) present a problem both for triacs and for the MOC3011 because the voltage and current are not in phase with each other. Since the triac turns off at zero current, it may be trying to turn off when the applied current is zero but the applied voltage is high. This appears to the traic like a sudden rise in applied voltage, which turns on the triac if the rate of rise exceeds the commutating dv/dt of the triac or the static dv/dt of the MOC3011.

SNUBBER NETWORKS

The solution to this problem is provided by the use of snubber networks to reduce the rate of voltage rise seen by the device. In some cases, this may require two snubbers — one for the triac and one for the MOC3011. The triac snubber is dependent upon the triac and load used. In many applications the snubber used for the MOC3011 will also adequately protect the triac.

In order to design a snubber properly, one should know the power factor of the reactive load, which is defined as the cosine of the phase shift caused by the load. Unfortunately, this is not always known, and this makes snubbing network design somewhat empirical. However a method of designing a snubber network may be defined, based upon a typical power factor. This can be used as a "first cut" and later modified based upon experiment.

Assume an inductive load with a power factor of PF = 0.1 is to be driven. The triac might be trying to turn off when the applied voltage is given by

$$V_{to} = V_{pk}\sin\phi \approx V_{pk} \approx 180\ \text{V}$$

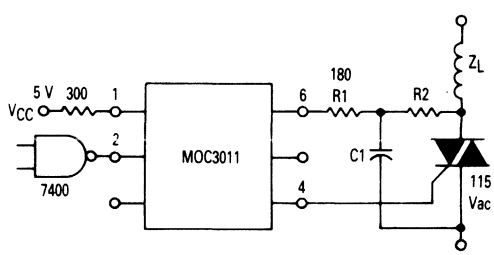
First, one must choose R1 (Figure 3.30) to limit the peak capacitor discharge current through the MOC3011. This resistor is given by

$$R1 = V_{pk}/I_{max} = 180/1.2\ \text{A} = 150\ \Omega$$

A standard value, 180 ohm resistor can be used in practice for R1.

It is necessary to set the time constant for $\tau = R_2C$. Assuming that the triac turns off very quickly, we have a peak rate of rise at the MOC3011 given by

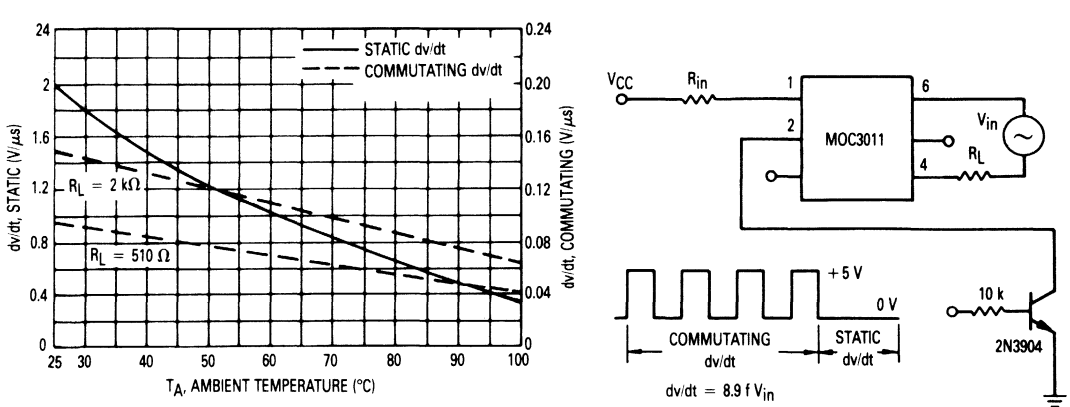
$$dv/dt = V_{to}/\tau = V_{to}/R_2C$$



NOTE: CIRCUIT SUPPLIES 25 mA DRIVE TO GATE OF TRIAC AT V_{in} = 25 V AND $T_A \leq 70°C$.

TRIAC		
I_{GT}	R2	C
15 mA	2400	0.1
30 mA	1200	0.2
50 mA	800	0.3

Figure 3.30. Logic to Inductive Load Interface



1) For a more thorough discussion of snubbers, see page 1-3-9.

Figure 3.31. dv/dt versus Temperature

Setting this equal to the worst case dv/dt (static) for the MOC3011 which we can obtain from Figure 3.33 and solving for R_2C:

$$dv/dt\ (T_J = 70°C) = 0.8\ V/\mu s = 8 \times 10^3$$

$$R_2C = V_{to}/(dv/dt) = 180/(8 \times 10^5) \approx 230 \times 10^{-6}$$

The largest value of R2 available is found, taking into consideration of triac gate requirements. If a sensitive gate triac is used, such as 2N6071B, I_{GT} = 15 mA @ −40°C. If the triac is to be triggered when $V_{in} \leq 40$ V

$$(R1 + R2) \approx V_{in}/I_{GT} \approx 40/0.015 \approx 2.3\ k$$

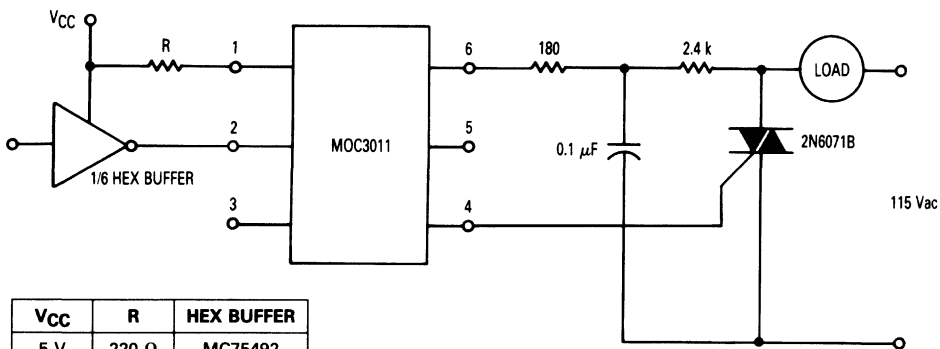
If we let R2 = 2400 ohms and C1 = 0.1 μF, the snubbing requirements are met. Triacs having less sensitive gates will require that R2 be lower and C1 be correspondingly higher as shown in Figure 3.30.

INCREASING INPUT SENSITIVITY

In some cases, the logic gate may not be able to source or sink 15 mA directly. CMOS, for example, is specified to have only 0.5 mA output, which must then be increased to drive the MOC3011. There are numerous ways to increase this current to a level compatible with the MOC3011 input requirements; an efficient way is to use athe MC14049B shown in Figure 3.32. Since there are six such buffers in a single package, the user can have a small package count when using several MOC3011's in one system.

INPUT PROTECTION CIRCUITS

In some applications, such as solid state relays, in which the input voltage varies widely, the designer may want to limit the current applied to the LED of the MOC3011. The circuit shown in Figure 3.33 allows a non-critical range of input voltages to properly drive the MOC3011 and at the same time protects the input LED from inadvertent application of reverse polarity.



V_{CC}	R	HEX BUFFER
5 V	220 Ω	MC75492
10 V	600 Ω	MC75492
15 V	910 Ω	MC14049B

Figure 3.32. MOS to ac Load Interface

INPUT CIRCUITRY

RESISTOR INPUT

When the input conditions are well controlled, as for example when driving the MOC3011 from a TTL, DTL, or HTL gate, only a single resistor is necessary to interface the gate to the input LED of the MOC3011. This resistor should be chosen to set the current into the LED to be a minimum of 10 mA but no more than 50 mA. 15 mA is a suitable value, which allows for considerable degradation of the LED over time, and assures a long operating life for the coupler. Currents higher than 15 mA do not improve performance and may hasten the aging process inherent in LED's. Assuming the forward drop to be 1.5 V at 15 mA allows a simple formula to calculate the input resistor.

$$R_i = (V_{CC} - 1.5)/0.015$$

Examples of resistive input circuits are seen in Figures 3.28 and 3.32.

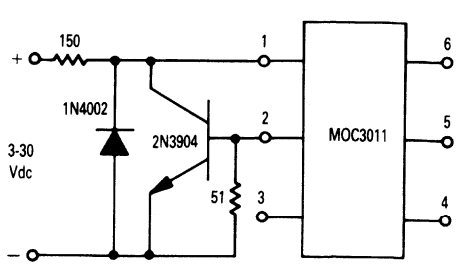


Figure 3.33. MOC3011 Input Protection Circuit

LED LIFETIME

All light emitting diodes slowly decrease in brightness during their useful life, an effect accelerated by high temperatures and high LED currents. To allow a safety margin and insure long service life, the MOC3011 is actually tested to trigger at a value lower than the specified 10 mA input threshold current. The designer can therefore design the input circuitry to supply 10 mA to the LED and still be sure of satisfactory operation over a long operating lifetime. On the other hand, care should be taken to insure that the maximum LED input current (50 mA) is not exceeded or the lifetime of the MOC3011 may be shortened.

TEST RESULTS ON THE MOC3011 AND MOC3021

Figure 3.34(a) shows the commutating dv/dt test circuit, and Figure 3.34(b) commutating dv/dt versus load resistance and ambient temperature for the non-zero crossing triac drivers.

The static dv/dt test circuit is shown in Figure 3.35(a). Static dv/dt versus ambient temperature and load resistance is graphed in Figures 3.35(a) and 3.35(b) for the MOC3011 and MOC3021, respectively. The static dv/dt is of primary importance when the triac driver is being used in conjunction with a triac, to control loads on the ac line.

Common-mode dv/dt is another significant parameter with non-zero crossing triac drivers. A common-mode spike on either the LED or detector could trigger the triac drivers. Thus, a large common-mode dv/dt rating is essential when using these devices in an electronically noisy environment. The test circuit used to measure this parameter is shown in Figure 3.36. Typical values exceed 5000 V/μs at 100°C, which is attained through the internal structure of the triac drivers.

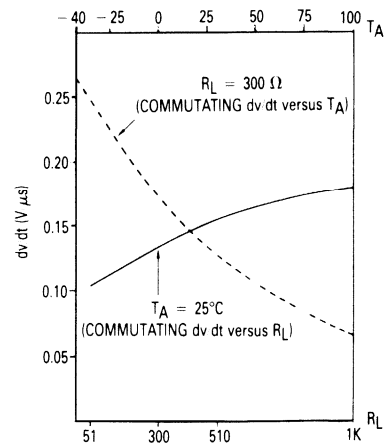
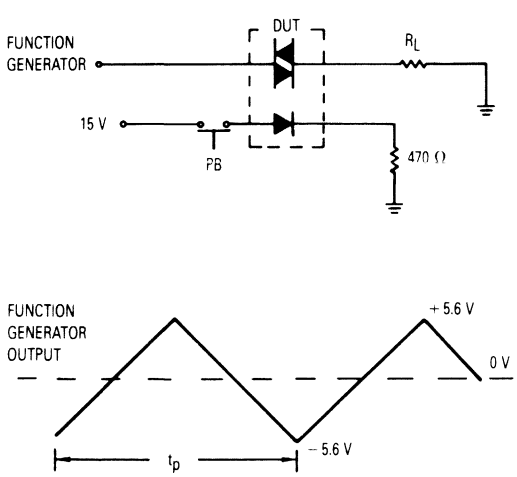


Figure 3.34(b). Commutating dv/dt versus Ambient Temperature and Load Resistance for the MOC3011 and MOC3021

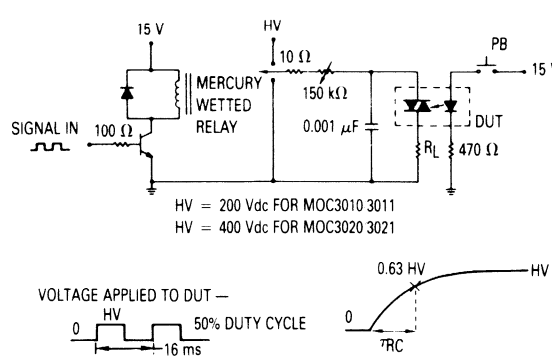


TEST PROCEDURE —

THE FREQUENCY OF THE TRAINGULAR WAVEFORM IS INCREASED UNTIL THE DUT REMAINS ON AFTER BEING TRIGGERED BY THE PUSHBUTTON. THE FREQUENCY IS THEN DECREASED UNTIL THE DUT TURNS OFF AND t_p IS MEASURED AT THIS POINT.

$$dv/dt = 22.4\ V/t_p$$

Figure 3.34(a). Commutating dv/dt Test Circuit



TEST PROCEDURE —

TURN THE DUT ONE WHILE APPLYING SUFFICIENT dv dt TO ENSURE THAT IT REMAINS ON EVEN AFTER THE TRIGGER CURRENT IS REMOVED. THEN DECREASE dv dt UNTIL THE DUT TURNS OFF. MEASURE τ_{RC}, THE TIME IT TAKES TO RISE TO 0.63 HV, AND DIVIDE 0.63 HV BE τ_{RC} TO GET dv dt.

Figure 3.35(a). Static dv/dt Test Circuit

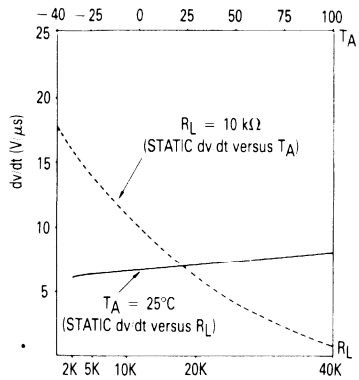


Figure 3.35(b). Static dv/dt versus Ambient Temperature and Load Resistance for the MOC3011

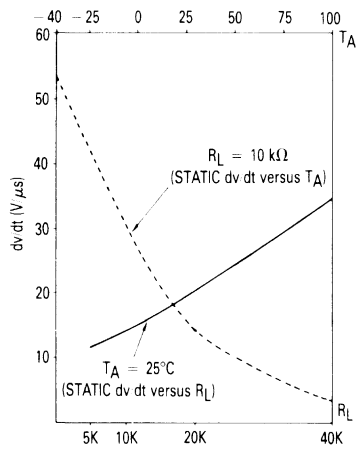


Figure 3.35(c). Static dv/dt versus Ambient Temperature and Load Resistance for the MOC3021

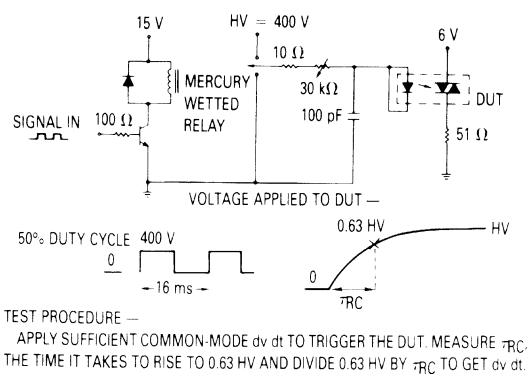


Figure 3.36. Common-Mode dv/dt Test Circuit

DRIVERS: THE MOC3061 AND MOC3081 ZERO-CROSSING TRIAC DRIVERS

Many new applications in the power control field were made possible by Motorola's introduction of the MOC3011 and MOC3021 optically isolated triac drivers. These six-pin, solid-state devices, with an input current of as little as 15 mA, can supply up to 100 mA drive current to switch triacs on either a 115 Vac or 230 Vac power line. Thus, high power ac loads can be controlled from low power circuitry, while an isolation voltage of 7.5 kV is maintained from input to output.

Increased flexibility in power control is possible with the MOC3061 and MOC3081 optically isolated, zero-crossing triac drivers. These new devices offer a unique zero-crossing feature, guaranteeing the triac driver will only 'switch on' between −25 V and +25 V. This insures lower generated noise and inrush currents and extends the life of incandescent lamp filaments. The circuitry necessary for zero-crossing is also responsible for improved device parameters, allowing the use of the MOC3061 and MOC3081 in a wide range of applications.

Zero-crossing triac drivers are currently being used in electrically noisy industrial environments, where control signals may travel several hundred yards before reaching the MOC3061 or MOC3081 triac driver. This is due to the improved common-mode noise immunity of these devices. Their large static dv/dt rating eliminates the need for snubber networks and guarantees that the zero-crossing triac drivers cannot be unintentionally triggered 'on,' by ac line noise. This is particularly important when the triac driver is used to control industrial equipment where inadvertent operation may cause damage or injury.

ELECTRICAL CHARACTERISTICS

The GaAs LED has a maximum forward voltage drop of 1.5 V at 30 mA and a reverse breakdown voltage of 3 V or more. The recommended LED current to trigger the detector (either the MOC3061 or MOC3081) is 15 mA. The minimum LED pulse width capable of triggering the detector is typically 10 microseconds at both 15 mA for the MOC3061 and MOC3081.

The MOC3061 detector has a minimum blocking voltage of 600 Vdc in either direction in the 'off' state whereas the minimum blocking voltage of the MOC3081 is 800 Vdc. Once triggered 'on,' either detector will pass 100 mA with less than 3 V drop across the device. Both will remain in this conducting state until the current drops below the holding current (typically 100 μA for the MOC3061 and the MOC3081) at which time the detector returns to the non-conducting state.

It may also be possible to inadvertently trigger the detector into the 'on' state by exceeding the forward blocking voltage or by voltage ramps across the detector exceeding the static dv/dt rating. These voltage ramps usually result from disturbances on the ac power line. However, since the typical static dv/dt rating of the zero-crossing triac driver is in excess of 1000 V microsecond

at 100°C, ac line noise poses little or no problem for these devices. As a result, the need for snubber networks on the triac drivers, to reduce the speed of voltage ramps, is eliminated. Figure 3.35 shows the static dv/dt test circuit.

Once the triac controlled by a triac driver is switched to the conducting state, very little voltage appears across MT1 and MT2, the main terminals of the triac (Figure 3.37). Since there is also a small voltage drop from the gate to T2, the total voltage across the triac driver terminals T1 and T2 is very small — typically less than 2 V. Thus, the detector of the triac driver will conduct very little current and will, for practical purposes, be 'off.' This condition has very important implications when a triac driver and triac are being used to control an inductive load.

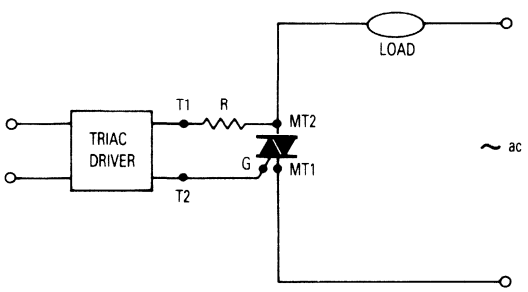


Figure 3.37. Typical ac Power Line Control Circuit

Commutating dv/dt, a phenomena associated with inductive loads, presents a problem for both triacs and zero-crossing triac drivers. In the steady state, voltage and current are 90 degrees out of phase for an inductive load. Therefore, when a triac attempts to turn 'off' at zero current, the applied voltage is high. This sudden rise in voltage will trigger the triac back 'on' if it exceeds the commutating dv/dt of the triac, since it has been on; or, the static dv/dt of the triac driver, since it has been basically off. Because the static dv/dt of the zero-crossing triac driver is so large, the commutating dv/dt of the triac will be the limiting factor. Therefore, commutating dv/dt only becomes a limiting factor when the zero-crossing triac drivers are being used in direct drive applications. Figure 3.38 shows commutating dv/dt versus ambient temperature and load resistance for the zero-crossing triac drivers.

Another important parameter associated with the zero-crossing triac drivers, is common-mode dv/dt. A large common-mode dv/dt rating is essential when using these devices in a noisy environment, due to the possibility of triggering the triac drivers 'on' with a common-mode spike on either the LED or detector. The test circuit used to measure this quantity is shown in Figure 3.36. Typical values exceed 5000 V/μs at 100°C. This value is attained through the inhibiting action of the internal circuitry of the zero-crossing triac drivers.

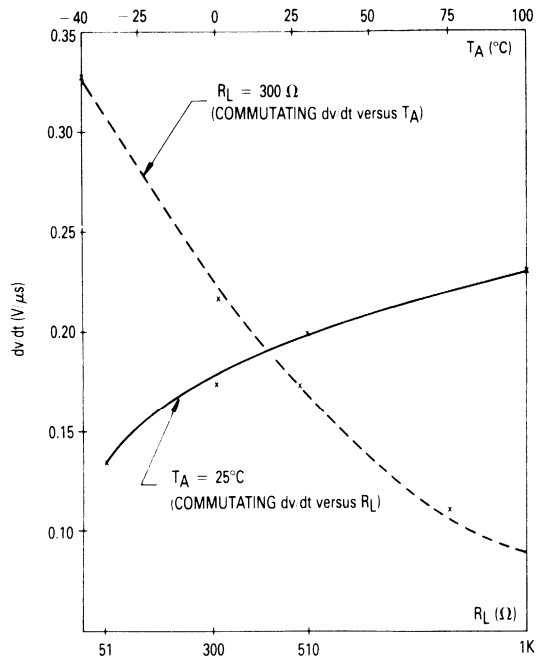


Figure 3.38. Commutating dv/dt versus Ambient Temperature and Load Resistance

ZERO CROSSING VERSUS NON-ZERO CROSSING TRIAC DRIVERS

Several of the benefits made possible by the zero-crossing circuitry have already been discussed. The large common-mode dv/dt makes these devices insensitive to common-mode EMI. In the same manner, the typical static dv/dt rating of 1000 V/microsecond at 100°C virtually eliminates the possibility of the zero-crossing triac drivers being unintentionally triggered on by ac line noise. This also eliminates the need for snubber networks on the triac drivers, along with their associated component cost and printed circuit board space.

In addition to the improvement in device parameters caused by the zero-crossing circuitry, the basic concept of switching the load 'on' only near zero voltage has many benefits.

There has been some controversy as to whether a peak-crossing triac driver might be more appropriate than a zero-crossing triac driver when controlling inductive loads. This is because the voltage and current are 90

degrees out of phase in an inductive load. At first glance it would seem logical to switch an inductive load 'on' at peak voltage to minimize the inrush current. However, voltage and current are only 90 degrees out of phase in an inductive load in the steady state. When switching an inductive load 'on,' an initial transient is also present. This transient must be added to the steady state response to fully characterize current flow in an inductive load. To illustrate this behavior, analyze the circuit of Figure 3.39, which can be used to model the response of an inductive load to the sudden application of a sinusoidal voltage.

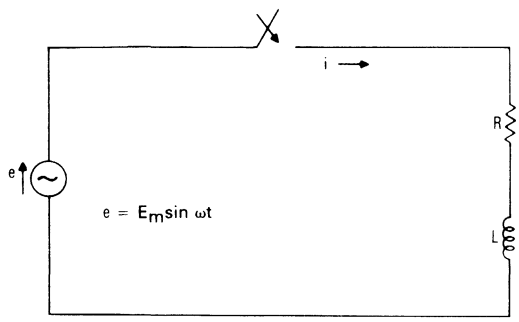


Figure 3.39. Circuit Model for Inductive Load Response

The switch is closed at t = 0. The applied voltage will be zero at this instant, analogous to the use of a zero-crossing triac driver. A small series resistance (R) has been included, since all inductors have some finite resistance.

The governing differential equation is

$$e = iR + L\frac{di}{dt} \tag{1}$$

with the initial condition $i(0-) = i(0+) = 0$, due to the inductor and no current flowing in the circuit with the switch open.

The total solution to this differential equation is the sum of a transient and steady state response

$$i_{TOT} = i_{TRAN} + i_{SS} \tag{2}$$

where

$$i_{TRAN} = A_1 e^{-Rt/L} \tag{3}$$

and

$$i_{SS} = A_2 \sin \omega t + A_3 \cos \omega t \tag{4}$$

Substituting these solutions into the governing differential equation and satisfying the initial condition gives

$$i_{TOT} = \overbrace{\frac{E_m L\omega}{R^2 + L^2\omega^2} e^{-Rt/L}}^{i_{TRAN}} + \tag{5}$$

$$\overbrace{\frac{E_m R}{R^2 + L^2\omega^2} \sin \omega t - \frac{E_m L\omega}{R^2 + L^2\omega^2} \cos \omega t}^{i_{SS}}$$

This solution also gives insight into another important parameter associated with triacs — the di/dt rating. If the maximum di/dt rating of a triac is exceeded, the triac's characteristics can be adversely affected or the triac permanently damaged. In the case of the zero-crossing triac driver, the di/dt applied to the triac is easily calculated from the previous solution.

$$\frac{di_{TOT}}{dt} = \frac{-R}{L} \frac{E_m L\omega}{R^2 + L^2\omega^2} e^{-Rt/L} + \frac{E_m R\omega}{R^2 + L^2\omega^2} \cos \omega t$$

$$+ \frac{E_m L\omega^2}{R^2 + L^2\omega^2} \sin \omega t \tag{6}$$

$$\left.\frac{di_{TOT}}{dt}\right|_{t=0} = 0$$

Thus, there is little possibility of damage to the triac when using a zero-crossing triac driver. If a peak-crossing triac driver were used, the voltage source shown in Figure 3.39 would become $e = E_m \cos \omega t$ to model the peak voltage impressed across the load at t = 0. The initial condition of $i(0-) = i(0+) = 0$ remains the same and the solution becomes

$$i_{TOT} = \overbrace{\frac{-E_m R}{R^2 + L^2\omega^2} e^{-Rt/L}}^{i_{TRAN}} +$$

$$\overbrace{\frac{E_m L\omega}{R^2 + L^2\omega^2} \sin \omega t + \frac{E_m R}{R^2 + L^2\omega^2} \cos \omega t}^{i_{SS}} \tag{7}$$

With a peak-crossing triac driver

$$\frac{di_{TOT}}{dt} = \frac{R}{L} \frac{E_m R}{R^2 + L^2\omega^2} e^{-Rt/L}$$

$$+ \frac{E_m L\omega^2}{R^2 + L^2\omega^2} \cos \omega t - \frac{E_m R\omega}{R^2 + L^2\omega^2} \sin \omega t \tag{8}$$

$$\left.\frac{di_{TOT}}{dt}\right|_{t=0} = \frac{E_m}{R^2 + L^2\omega^2}\left[\frac{R^2}{L} + L\omega^2\right] = \frac{E_m}{L} \tag{9}$$

This value can become very large depending upon the peak applied voltage and inductance of the load. If it exceeds the maximum di/dt rating of the triac, serious damage can result.

It is easy to conclude that, when controlling inductive loads using a triac driver and triac, a zero-crossing triac driver is a far more desirable device than a peak-crossing triac driver.

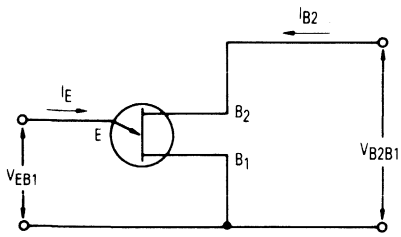


Figure 3.40(a). UJT Symbols, Nomenclature, and Emitter Characteristics

DRIVERS: THE UNIJUNCTION TRANSISTOR

The unijunction transistor (UJT) is a three terminal device, the three terminals being the emitter, base-one and base-two (Figure 3.40a).

The UJT (or double base diode as it was called in early papers) has, as the name implies, only a single P-N junction, and the characteristics of the UJT are for this reason quite different from those of the conventional transistor (Figure 3.40). Table 3.I shows the commonly used UJT symbols and their proper definitions in accordance with the Joint Electron Device Engineering Council (JEDEC) Standard.

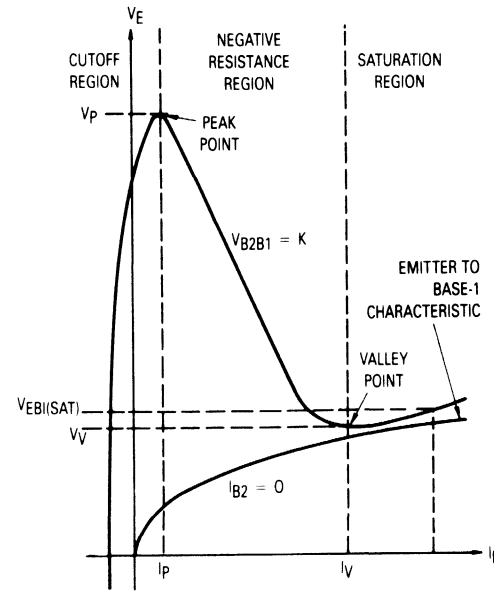


Figure 3.40(b). Static Emitter Characteristics Curves

Table 3.I. Unijunction Transistor Nomenclature

Symbol	Definition
I_E	Emitter current.
I_{EO}	Emitter reverse current. Measured between emitter and base-two at a specific voltage, and base-one open-circuited.
I_p	Peak point emitter current. The maximum emitter current that can flow without allowing the UJT to go into the negative resistance region. Peak point is the lowest current on the emitter characteristic where: $\frac{d V_{EB1}}{d I_E} = 0$
I_V	Valley point emitter current. The current flowing in the emitter when the device is biased to the valley point. Valley point is the second lowest current on the emitter characteristic where: $\frac{d V_{EB1}}{d I_E} = 0$
r_{BB}	Interbase resistance. Resistance between base-two and base-one meaured at a specified interbase voltage.
V_{B2B1}	Voltage between base-two and base-one. Positive at base-two.
V_p	Peak point emitter voltage. The maximum voltage seen at the emitter before the UJT goes into the negative resistance region.
V_D	Forward voltage drop of the emitter junction.
V_{EB1}	Emitter to base-one voltage
$V_{EB1(SAT)}$	Emitter saturation voltage. Forward voltage drop from emitter to base-one at a specific emitter current (larger than I_V) and specified interbase voltage.
V_V	Valley point emitter voltage. The voltage at which the valley point occurs with a specified V_{B2B1}.
V_{OB1}	Base-one peak pulse voltage. The peak voltage measured across a resistor in series with base-one when the unijunction transistor is operated as a relaxation oscillator in a specified circuit.
η	Intrinsic standoff ratio. Defined by the relationship: $= \frac{V_p - V_D}{V_{B2B1}}$
α_{rBB}	Interbase resistance temperature coefficient. Variation of resistance between B_2 and B_1 over the specified temperature range and measured at the specific interbase voltage and temperature with emitter open circuited.
$I_{B2(mod)}$	Interbase modulation current. B2 current modulation due to firing. Measured at a specified interbase voltage, emitter and temperature.

In order to explain the operation of the unijunction transistor it is convenient to use the so called bar structure as a model (the bar structure will be discussed in detail later). This structure is shown somewhat simplified in Figure 3.41(a) and the electrical equivalent circuit is shown in Figure 3.41(b). The equivalent circuit is valid for emitter currents equal to or less than the peak point current.

When voltage V_{B2B1} is applied, a current will flow in the silicon bar from base-two to base-one. Since the bar is essentially a resistor of magnitude r_{BB}, the current that flows into base-two is determined by $I_{B'2} = \frac{V_{B2B1}}{r_{BB}}$. A fraction of the applied voltage V_{B2B1} will appear at point A where the emitter is alloyed onto the silicon bar, and this fraction is denoted as η. The voltage at point A is therefore ηV_{B2B1}, the P-N junction formed by the emitter and the silicon bar is reverse biased and only a small reverse leakage current flows in the emitter lead.

As the voltage V_E at the emitter is increased, a point will be reached where V_E equals the voltage at point A, plus the forward voltage drop of the P-N junction, V_D. The emitter voltage at this point is called the peak point emitter voltage V_p. The peak point voltage can be written as:

$$V_p = V_D + \eta V_{B2B1} \qquad (1)$$

The P-N junction is now forward biased, and holes will be injected from the emitter into the silicon bar. The electric field inside the bar set up by V_{B2B1} is of such a direction that the injected holes will be moved toward the base-one terminal. Conductivity σ of a semiconductor material is given by the equation:

$$\sigma = q(\mu_e n + \mu_h p) \qquad (2)$$

where q = electronic charge (1.6×10^{19} coulomb)
μ_e = mobility of conduction electrons
μ_h = mobility of conduction holes
n = electron concentration
p = hole concentration

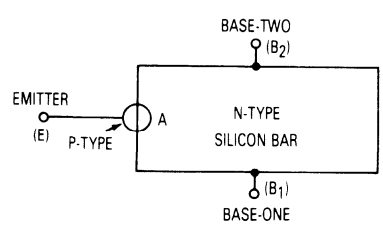
When the holes are injected into the bar from the emitter, an equal amount of electrons will be injected from base-one to maintain charge neutrality. Since both the electron and hole concentrations increase in the silicon bar between the emitter and base-one, the conductivity will also increase according to equation 2. Resistivity ρ is defined as the reciprocal of conductivity or:

$$\rho = \frac{1}{\sigma} \qquad (3)$$

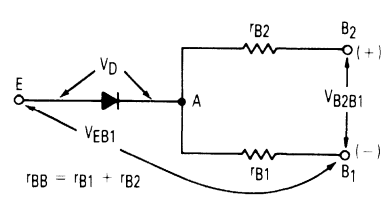
and hence the resistivity will decrease. This process is called "conductivity modulation." The decrease in resistivity will cause a decrease in the voltage drop from emitter to base-one, which in turn allows more holes to be injected from the emitter, and the conductivity will increase further. This is clearly a regenerative process, and the UJT is now in the so-called negative resistance region. An equivalent circuit for this region is shown in Figure 3.41(c). At emitter currents equal to or less than I_p the resistance r_{BB} can be divided into two parts; r_{B1} and r_{B2} according to the relations:

$$r_{B1} = \eta r_{BB} \text{ and } r_{B2} = r_{BB} - r_{B1}. \qquad (4)$$
(As shown in Figure 3.41b)

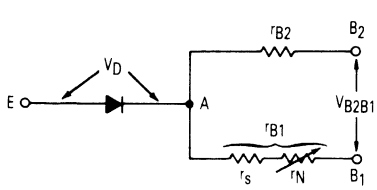
In the negative resistance region, resistor r_{B1} can be thought of to consist of a fixed portion r_s, and a variable



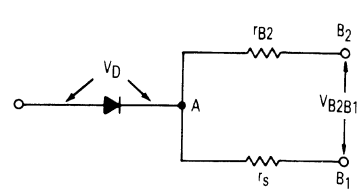
(a) A Simplified Bar Structure



(b) Equivalent Circuit Valid for $I_s \leq I_p$



(c) Equivalent Circuit for the UJT in the Negative Resistance Region



(d) Equivalent Circuit for the UJT in the Saturation Region

Figure 3.41. UJT Structure and Equivalent Circuits

portion r_N, where r_S is the saturation resistance and r_N is the negative resistance, the magnitude of which decreases with increasing emitter current. r_N will be equal to zero when the hole concentration in the silicon bar is approximately $10^{16} \frac{\text{carriers}}{\text{Cm}^3}$† and under that condition the saturation resistance r_S will be only resistance between emitter and base-one. When $r_{B1} = r_S$, the UJT is no longer in the negative resistance region. The reason for this is that the high density of carriers in the bar has decreased the lifetime τ of the carriers sufficiently to counteract the effects of the new carriers being generated. Mobility is related to lifetime by the equations:

$$\mu_e = \frac{q\tau}{m_e} \text{ and } \mu_h = \frac{q\tau}{m_h} \qquad (5)$$

where m_e and m_h are the effective mass of electrons and holes, respectively. Mobility therefore decreases when lifetime decreases, and the conductivity given by equation (2) is found to remain relatively constant for emitter currents up to 500 mA.

The point on the emitter characteristic where r_{B1} just reaches its minimum value is called the valley point. The emitter current and voltage at this point are the valley point emitter current I_V, and the valley point emitter voltage V_V.

When the emitter current is increased beyond I_V, the unijunction transistor enters the so-called saturation region where the emitter current is essentially a linear function of the emitter voltage. The equivalent circuit for the saturation region is shown in Figure 3.41(d).

The standard unijunction transistor symbol with appropriate terms for current and voltage is given in Figure 3.40(a), and a static emitter characteristic curve for a single value of V_{B2B1} is shown in Figure 3.40(b). It should be noted that the emitter curve is not drawn to scale in order to show the different operating regions in more detail. The region to the left of the peak point is called the "cutoff region," the emitter junction being reverse biased in most of this region and slightly forward biased at the peak point. The region between the peak point and the valley point, where the emitter junction is forward biased and conductivity modulation takes place, is called the "negative resistance region." The region to the right of the valley point, where the emitter current is limited by r_S, is called the "saturation region." The curve for base-two current (I_{B2}) equal to zero is essentially the forward characteristic of a silicon diode.

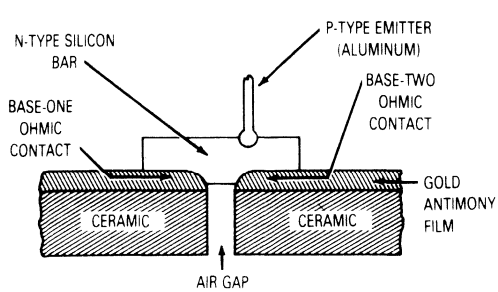
UJT STRUCTURES

Early unijunction transistors were the bar structure and the cube structure, the cross-section diagrams of which are shown in Figure 3.42.

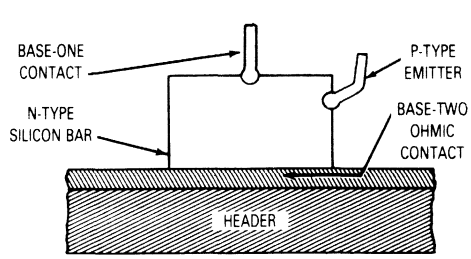
The bar structure in Figure 3.42(a) is formed by mounting a high resistivity N-type silicon bar on a ceramic platform having an air gap in the center and gold-antimony film deposited on each side of the gap. Base-one and base-two are ohmic contacts that are formed between the silicon bar and the gold. A single P-type emitter is formed by alloying an aluminum wire onto the bar opposite from the base contacts.

The cube structure, shown in Figure 3.42(b) employs a high resistivity N-type silicon cube. The cube is mounted on a header with a gold-antimony alloy contact between the bottom of the cube and the header. The base-two ohmic contact is made to the gold-antimony area. Base-one is formed by alloying a gold wire to the top of the silicon bar and the emitter is similarly formed by alloying an aluminum wire to a side of the cube.

Although the bar and cube structures have been in use for many years, they are not readily adapted to modern automatic production methods. For this reason, Motorola has evolved a new and different design in which the die is fabricated using processes similar to those used for silicon annular overlay transistors. A simplified outline of the production steps is given in Figure 3.43. Referring to Figure 3.43(a), using photo-resist techniques and starting with an oxide passivated die of high resistivity N-type silicon, the emitter is diffused in using P-type boron. In Figure 3.43(b) the whole structure is again oxide protected. Windows are then etched in the oxide, and base-one and the annular ring are formed by the diffusion of N-type phosphorus. The structure is oxide protected again in Figure 3.43(c), followed by a selective etching that removes the oxide in the emitter and base-one areas. Aluminum is then evaporated onto the structure to make contact with the emitter and base-one, while gold is evaporated onto the bottom of the die to form the base-two



(a) Bar Structure



(b) Cube Structure

Figure 3.42. Early UJT Structures

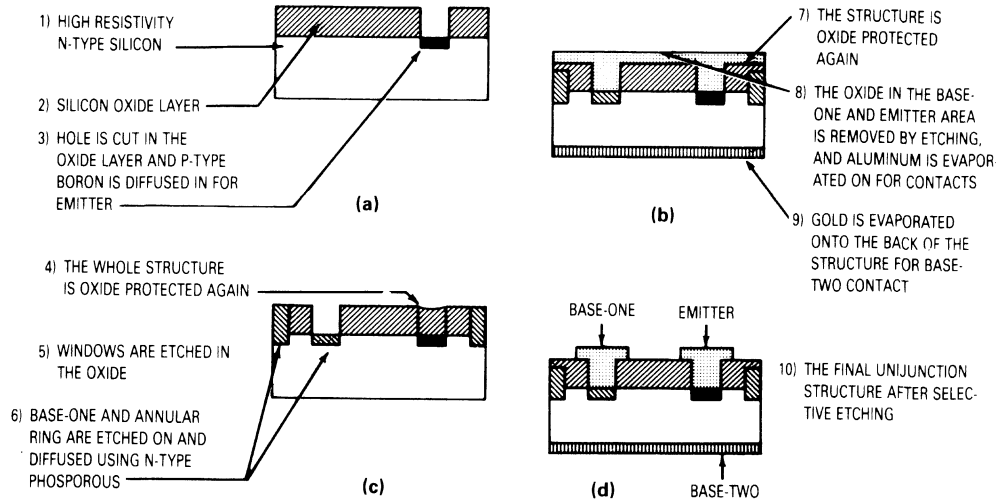


Figure 3.43. The Annular Unijunction

contact. In Figure 3.43(d) the exact contact geometries are determined by a final etch. In practice the above production steps are not performed on a single die but to a whole wafer. After the final etch the wafers are tested, scribed, and broken into several hundred dice.

Figure 3.44 shows a photomicrograph of the 2N4851 UJT geometry. In actual practice two base-one regions are formed, and before the bonding is performed, the die and the base-one region are probed, providing the optimum characteristics are selected.

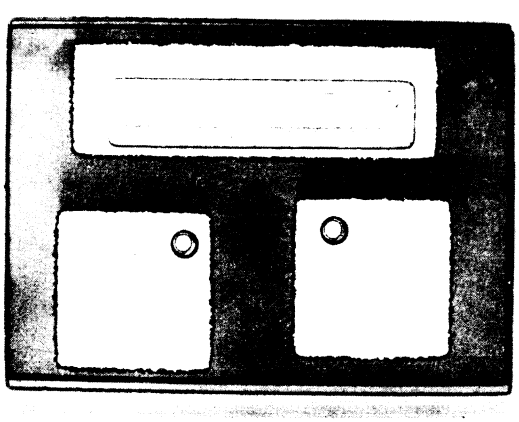


Figure 3.44. Photomicrograph of Motorola Annular UJT Structure

Table 3.II shows the key parameters of the three UJT structures.

Table 3.II. Comparison of Key Parameters for the Three Different UJT Structures. Typical Values are shown.

Parameter	Typical Values for Bar	Cube	Annular
Intrinsic Standoff Ratio η	0.6	0.65	0.7
Interbase Resistance r_{BB}	7 k	7 k	7 k
Emitter Saturation Voltage $V_{EB1(SAT)}$	3 V	1.5 V	2.5 V
Peak Point Current I_p	2 μA	1 μA	0.1 μA
Valley Point Current I_V	15 mA	10 mA	7 mA
Emitter Reverse Current I_{EO}	1 μA	0.1 μA	5 nA

STATIC EMITTER CHARACTERISTICS

The emitter characteristic shown previously was not drawn to scale for the reasons explained. Figure 3.45, however, shows typical emitter curves for V_{B2B1} = 20 volts drawn to scale. Figure 3.45(a) shows part of the cutoff region plotted on linear scale. When the emitter voltage is zero, the emitter current is negative, i.e.: out of the emitter terminal, and is approximately equal to 1

nanoampere. Peak point voltage is reached at a forward emitter current of about 10 pA and as can be seen from Figure 3.45(b) the voltage remains constant until the emitter current reaches approximately 0.1 μA, at which point the voltage starts to decrease. From the definition of peak current, I_p for this particular device is therefore 0.1 μA and V_p equals 16 volts. Valley voltage can be seen to be about 1.6 volts and the valley current approximately 8 mA. The saturation resistance r_s can be found from the slope of the emitter characteristic in the saturation region (above 8 mA) and is in this case approximately 5 ohms. The characteristic in the negative resistance region was determined by the use of a constant-current source.

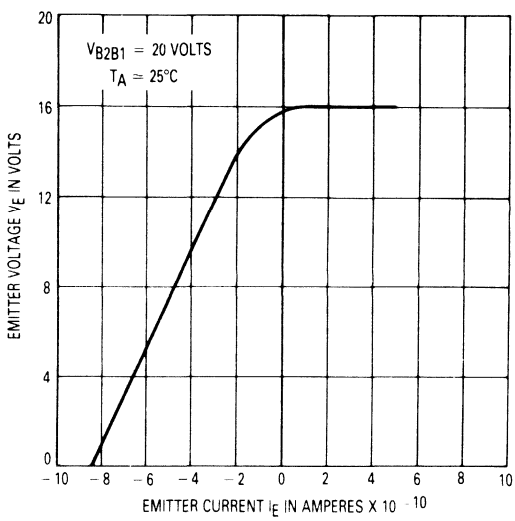


Figure 3.45(a). Static Emitter Characteristic

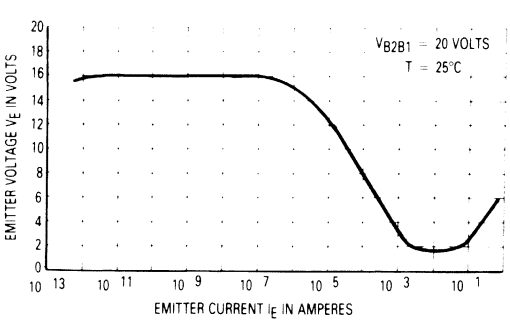


Figure 3.45(b). Static Emitter Characteristic

THE DIODE VOLTAGE DROP V_D

Some of the most important characteristics of the UJT are those that appear in the formula for peak voltage:

$$V_p = V_D + \eta V_{B1B2} \qquad (6)$$

Changes in the peak voltage would be very undesirable in applications like timers and oscillators, the accuracy of which depends on the repeatability of V_p.

V_D is defined as the forward voltage drop of the emitter junction and since it is essentially equivalent to the forward voltage drop of a silicon diode, the value of V_D is dependent both on forward current and temperature. V_D can be measured several ways, but it is important to hold the emitter current near I_p when the measurement is made since it really is V_D at I_p that is required in equation 6. One simle way of measuring V_D is shown in Figure 3.46. A constant current equal to I_p is applied between the emitter and base-one, and a potentiometric voltmeter is used to measure the voltage from emitter to base-two. This type of voltmeter has essentially infinite input impedance when the meter is "nulled" and there is no current flowing in the base-two lead. The voltage measured is therefore equal to V_D.

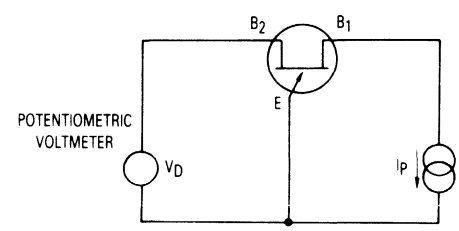


Figure 3.46. Circuit for Measuring V_D

Figure 3.47 shows V_D as a function of temperature for an emitter current of 1 μA. The variation of V_D is essentially linear over the temperature range considered and is equal to −2.7 mV/°C. The diode voltage drop therefore decreases with increasing temperature and V_D can be written as:

$$V_D = V_{DN} - (T - 25) \cdot K_D$$

where V_{DN} is the value of V_D at T_A = 25°C and K_D = −2.7 mV/°C. (Note that K_D is current dependent and the value for K_D given applies only at 1 μA.)

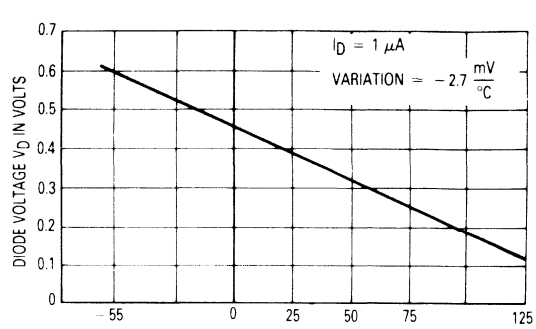


Figure 3.47. Diode Voltage V_D versus Temperature for the Annular Unijunction

THE INTRINSIC STANDOFF RATIO

The intrinsic standoff ratio, defined by:

$$\eta = \frac{V_p - V_D}{V_{B2B1}} = \frac{r_{B1}}{r_{BB}} \qquad (7)$$

is generally believed to be essentially independent of temperature variations. However, this is not true. Figure 3.48 shows typical variations of η with temperature for unijunctions from three different manufacturers. There may be several reasons why η varies with temperature; the interbase resistance r_{BB} might not have a uniform temperature coefficient throughout the base-two, base-one region, or the temperature might not be uniform over the entire interbase resistance. Surface recombination might also be a factor.

constant as the temperature is increased. The lattice mobility decreases with increasing temperature due to increased lattice scattering, and hence the resistivity will increase. As the temperature is increased beyond 125°C, the impurity concentration becomes swamped by carriers produced by thermal generation, and the resistivity decreases rapidly as the temperature is increased. The measurements were performed on a pulsed basis to avoid heating due to power dissipation. In the temperature region from 0 to +125°C, the increase in r_{BB} with temperature is essentially linear, and r_{BB} can be expressed by the formula:

$$r_{BB} = r_{BBN} + (T - 25) \cdot K_r$$

where r_{BBN} is the value of r_{BB} at 25°C, and K_r is given

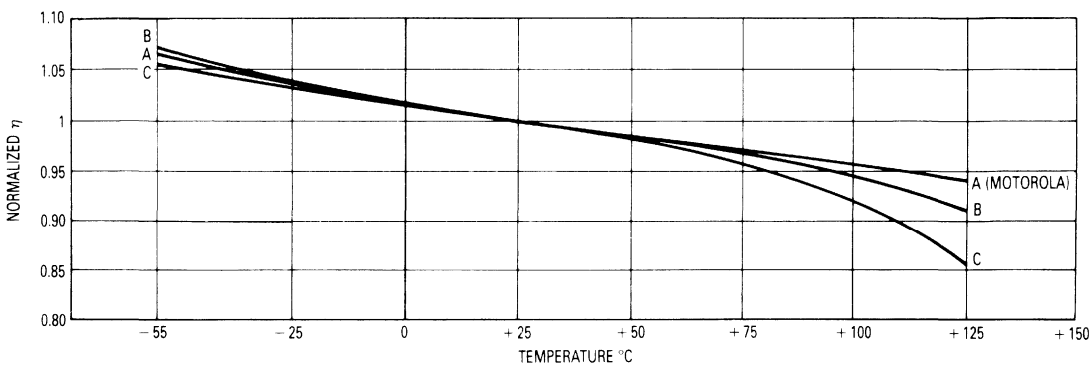


Figure 3.48. Normalized Intrinsic Standoff Ratio versus Temperature for 3 Different Manufacturers (A, B, & C)

η can be measured directly or it can be calculated from equation 7 when V_p and V_D are known.

The curve A-A in Figure 3.48 represents the Motorola annular UJT, and the variation of η is relatively linear with temperature over the temperature region considered. η can therefore be expressed by the formula:

$$\eta = \eta_N - (T - 25)\, K_\eta$$

where η_N is the value of η at 25°C, and K_η is a temperature coefficient expressed in %/°C. For the Motorola annular devices $K_\eta \cong \frac{0.06\%}{°C}\,\eta_N$

The intrinsic standoff ratio is also slightly dependent on V_{B2B1}, but the variation is so small that for all practical purposes η can be said to be independent of voltage.

THE INTERBASE RESISTANCE r_{BB}

The resistance from base-two to base-one is highly temperature dependent. A typical r_{BB} vs. temperature characteristic curve for V_{B2B1} = 3 volts is shown in Figure 3.49. At very low temperatures, near absolute zero, few of the impurity atoms in the semiconductor material are ionized and the resistivity of the doped silicon is quite high. At −55°C however, most of the impurity atoms are fully ionized, and the carrier concentration is relatively

as a %/°C variation of r_{BBN}. For the annular devices K_r is found to be:

$$K_r \simeq 0.8\%/C \cdot r_{BBN}$$

In addition, r_{BB} is also found to vary with interbase voltage V_{B2B1}. A typical curve is shown in Figure 3.50 where r_{BBN} is normalized to the value of r_{BB} for V_{B2B1}

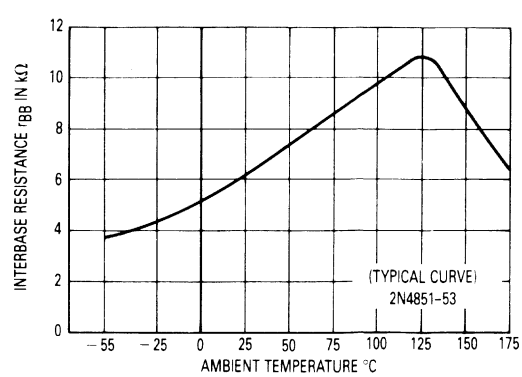


Figure 3.49. Interbase Resistance r_{BB} versus Temperature

= 3 volts, the voltage usually specified on the manufacturer's data sheet.

This increase in r_{BB} with voltage is in part due to a current limiting effect in the base one contact area. Knowing r_{BB} at V_{B2B1} = 3 V for an annular device, r_{BB} at any other value of V_{B2B1} can be found with a reasonable degree of accuracy from Figure 3.50. These readings have also been obtained by a low duty-cycle pulse method in order to avoid heating due to power dissipation. T_J is therefore approximately equal to T_A. For normal operating conditions, the temperature rise in the base-one, base-two region must be calculated and the change in r_{BB} due to temperature taken into account.

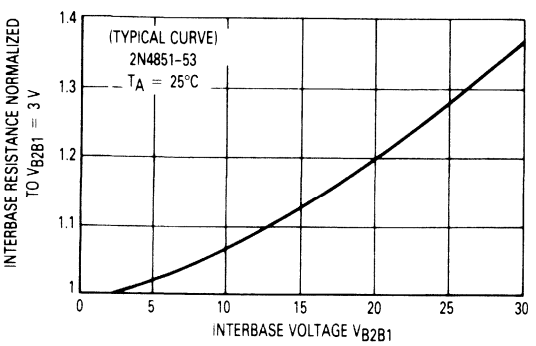


Figure 3.50. Typical Variation of r_{BB} as a Function of Interbase Voltage V_{B2B1}

THE PEAK POINT CHARACTERISTICS

Both V_p and I_p decrease as temperature is increased. That V_p will decrease is evident from the formula for V_p since both η and V_D were found to decrease. The variation of V_p with temperature can be minimized by the addition of an external resistor in the base two circuit. This procedure is discussed in detail in the appendix. V_p varies with interbase voltage in accordance with equation 6.

THE VALLEY POINT CHARACTERISTICS

Both valley point voltage V_V and current I_V decrease as ambient temperature is increased. A curve showing typical temperature behavior for the annular device is given in Figure 3.51 where the curves are normalized to the value at 25°C.

I_V and V_V are also dependent on the interbase voltage. When V_{B2B1} increases both I_V and V_V will increase also. Typical curves showing this behavior are given in Figure 3.52. I_V and V_V are normalized to the value at 10 volts V_{B2B1}.

Valley current is a relatively difficult characteristic to measure since, as can be seen in Figure 3.45(b), the voltage is relatively constant for large variations in emitter current around the valley point.

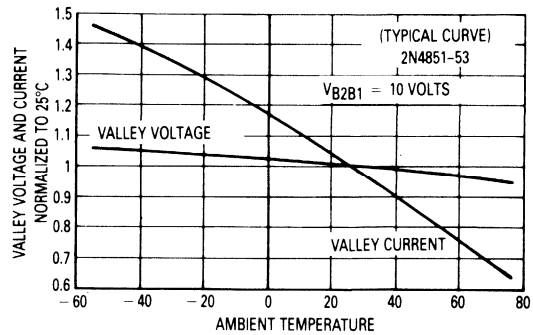


Figure 3.51. Valley Voltage and Valley Current versus Ambient Temperature

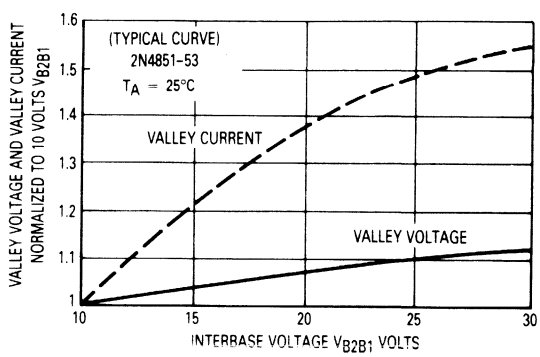


Figure 3.52. Valley Voltage and Valley Current versus Interbase Voltage V_{B2B1}

THE EMITTER REVERSE CURRENT I_{EO} (OR I_{EB2O})

The emitter reverse current is generally specified as the current flowing from base-two to the emitter with 30 volts applied between base-two and the emitter, (positive at base-two), and the base-one terminal open circuited. I_{EO} is highly temperature dependent since it actually is the leakage current of a silicon diode. This leakage current consists mainly of charge generation current, since diffusion current has little effect in silicon in the temperature range considered.

A curve showing typical variation of I_{EO} with temperature for a 2N4851 is shown in Figure 3.53 with I_{EO} being approximately 1.5 nA at 25°C.

INTERBASE CHARACTERISTICS

The measurement of base-two current I_{B2} as a function of interbase voltage and emitter current was performed on a sweep basis to avoid heating effects due to power dissipation. The test circuit for this measurement is

shown in Figure 3.54(a). A constant current was applied to the emitter from time t_0 to time t_1 and simultaneously a voltage ramp going from 0 to 30 volts was applied to base-two. Base-one was grounded. The current I_{B2} was measured with a current probe and applied to the vertical input of an oscilloscope, and the voltage ramp was applied to the horizontal input. As I_E and the ambient temperature were varied, the curves shown in Figures 3.54(b), (c) and (d) were observed.

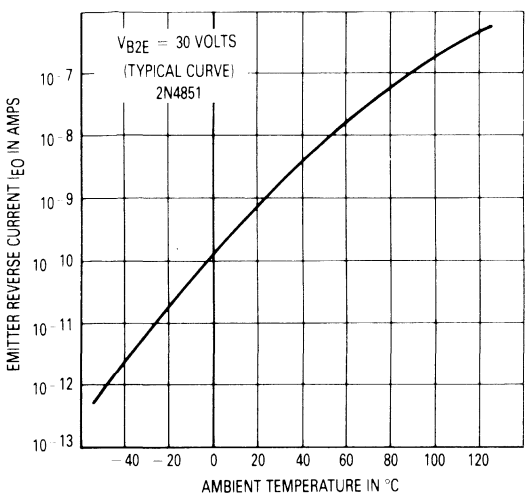


Figure 3.53. Emitter Reverse Current I_{EO} versus Ambient Temperature

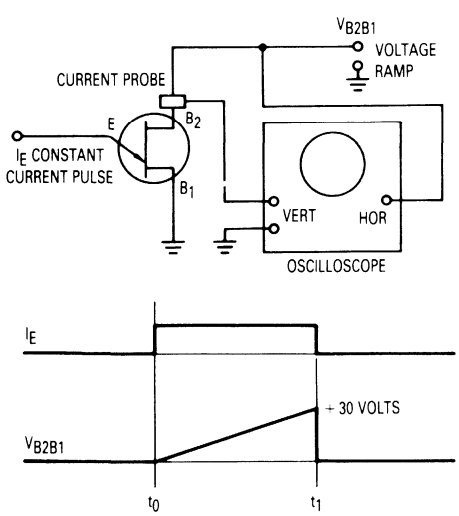


Figure 3.54(a). Test Circuit Used to Determine the Interbase Characteristic

It can be seen from the curves that the percentage increase in I_{B2} decreases with increasing emitter current and temperature. The modulated interbase current $I_{B2(mod)}$ is usually measured at I_E = 50 mA, V_{B2B1} = 10 volts, and T_A = 25°C. From Figure 3.54 this can be found to be approximately 11 mA.

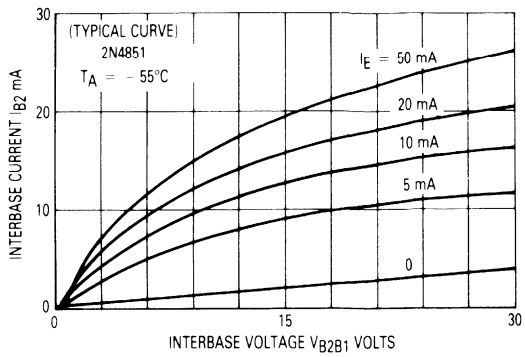


Figure 3.54(b). Interbase Characteristic

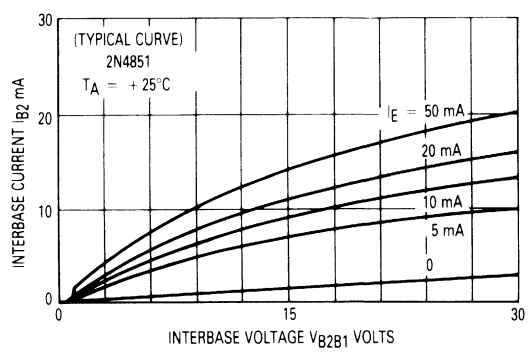


Figure 3.54(c). Interbase Characteristic

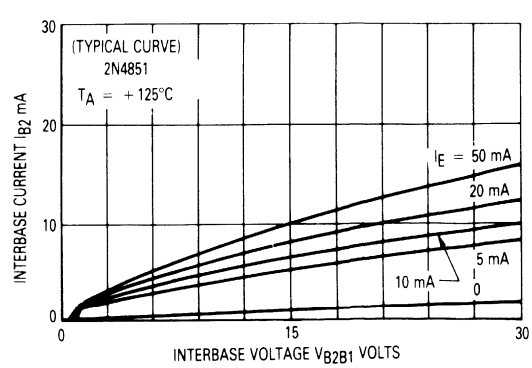


Figure 3.54(d). Interbase Characteristic

TRANSIENT CHARACTERISTICS

Switching times as specified for conventional junction transistors are generally not given on a UJT data sheet. Rather a parameter f_{max} is given which indicates the maximum frequency of oscillation that can be obtained using the UJT in a specified relaxation oscillator circuit.

In some applications such as critical timers, however, it might be of interest to determine "turn-on" and "turn-off" times associated with the UJT. Since these parameters are generally not specified, no fixed procedure has been established for their measurement, and two different methods with accompanying results will therefore be discussed here.

The circuit shown in Figure 3.55 was used to measure t_{on} and t_{off} for the case where the emitter circuit is purely resistive. Typical switching time values were found to be t_{on} = 1 μs and t_{off} = 2.5 μs. The waveform observed at the base-one terminal when the UJT turns off is shown in Figure 3.56. When the emitter is returned to ground, the stored charge in the junction will cause a current to flow out of the emitter and the output voltage across R_1 will be smaller than the steady state off value. Immediately following the removal of the excess charge, the voltage across R_1 will go higher than the steady state off value because r_{B1} has still not returned to normal following the conductivity modulation in the on state, and I_{B2} will be larger than the steady state off value. Steady state is reached after approximately 2.5 μs.

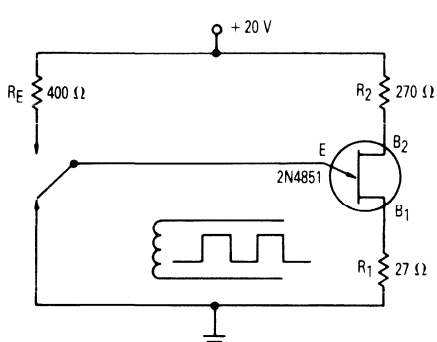


Figure 3.55. Circuit for t_{on} and t_{off} Measurements

In most practical applications, however, there will be both a resistor and a capacitor in the emitter circuit. The test circuit for this case was the relaxation oscillator circuit shown in Figure 3.57(a), and turn-on and turn-off waveforms as observed at base-one are shown in Figure 3.57(b) and (c). Turn-on time measured from the start of turn-on to the 90% point is approximately 0.5 μs and increases with increasing capacitance C_E. Turn-off time measured from the start of turn-off to the 90% point is about 12 μs, due to the long discharge time of the capacitor. t_{off} also increases with C_E.

The effect of the capacitance C_E on switching time is shown in Figure 3.58.

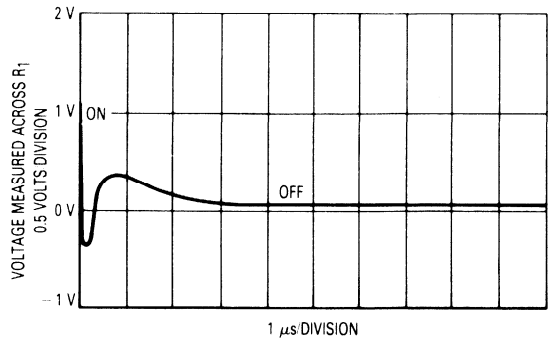


Figure 3.56. "Turn-Off" Waveform for the UJT as Measured in the Circuit in Figure 3.57

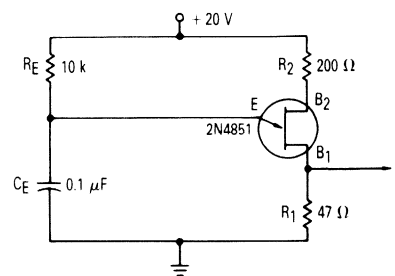


Figure 3.57(a). Relaxation Oscillator Circuit for t_{on} and t_{off} Measurements

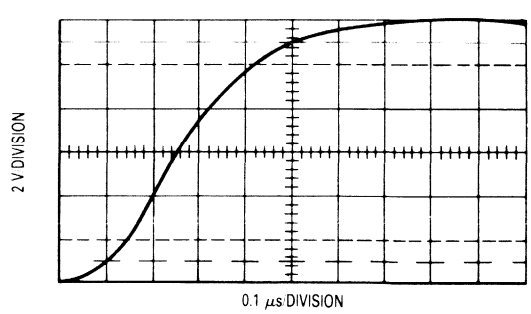


Figure 3.57(b). Turn-On Waveform

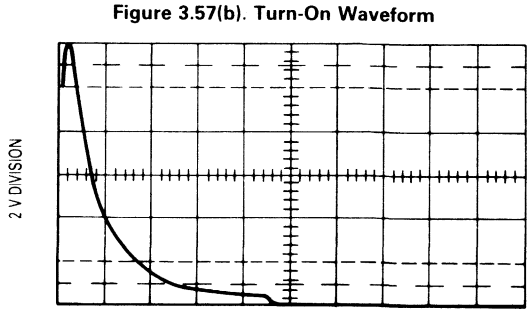


Figure 3.57(c). Turn-Off Waveform

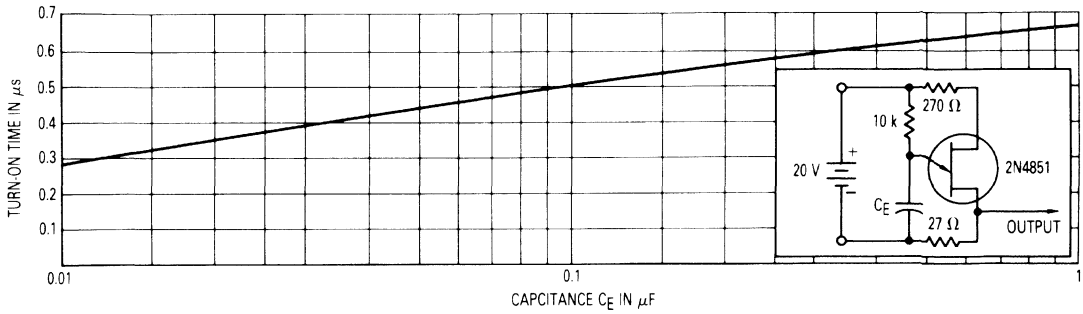


Figure 3.58(a). Turn-On Time versus Emitter Capacitance C_E

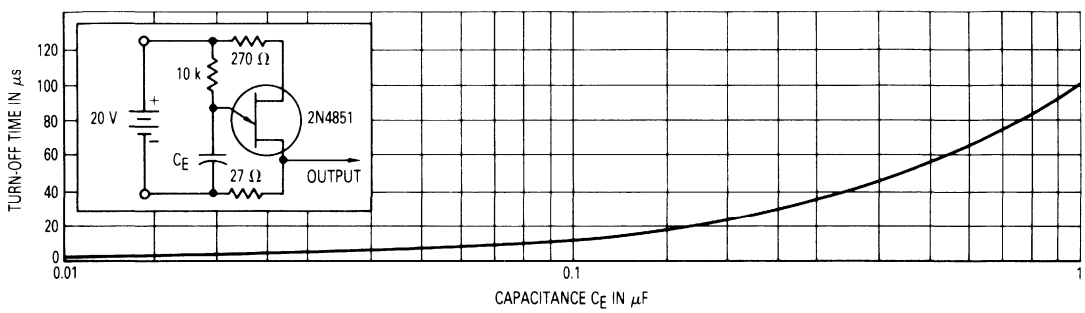


Figure 3.58(b). Turn-Off Time versus Emitter Capacitance C_E

DRIVERS: PROGRAMMABLE UNIJUNCTION TRANSISTORS

The programmable unijunction transistor (PUT) is a four layer device similar to an SCR except that the anode gate rather than the cathode gate is brought out. It is normally used in conventional unijunction transistor (UJT) circuits. The characteristics of both devices are similar, but the triggering voltage of the PUT is programmable and can be set by an external resistive voltage divider network. The PUT is faster and more sensitive than the UJT. It finds limited application as a phase control element and is most often used in long duration timer circuits. In general, the PUT is more versatile and is a more economical device than the UJT and will replace it in many applications.

OPERATION OF THE PUT

The PUT has three terminals, an anode (A), gate (G), and cathode (K). The symbol and a transistor equivalent circuit are shown in Figure 3.59. As can be seen from the equivalent circuit, the device is actually an anode-gated SCR. This means that if the gate is made negative with respect to the anode, the device will switch from a blocking state to its on state.

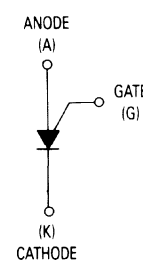


Figure 3.59(a). PUT Symbol

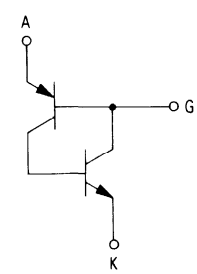


Figure 3.59(b). Transistor Equivalent

Since the PUT is normally used as a unijunction transistor (UJT), the UJT terminology is used to describe its parameters. In order to operate this device as a UJT, an external reference voltage must be maintained at the gate terminal. A typical relaxation type oscillator circuit is shown in Figure 3.60(a). The voltage divider shown is a typical way of obtaining the gate reference. In this circuit, the characteristic curve looking into the anode-cathode terminals would appear as shown in Figure 3.60(b). The peak and valley points are stable operating points at

either end of a negative resistance region. The peak point voltage (V_P) is essentially the same as the external gate reference, the only difference being the gate diode drop. Since the reference is circuit and not device dependent, it may be varied, and in this way, V_P is programmable. This feature is the most significant difference between the UJT and the PUT.

In characterizing the PUT, it is convenient to speak of the Thevenin equivalent circuit for the external gate voltage (V_S) and the equivalent gate resistance (R_G). The parameters are defined in terms of the divider resistors (R1 and R2) and supply voltage as follows:

$$V_S = R1\ V1/(R1 + R2)$$

$$R_G = R1\ R2/(R1 + R2)$$

Most device parameters are sensitive to changes in V_S and R_G. For example, decreasing R_G will cause peak and valley currents to increase. This is easy to see since R_G actually shunts the device and will cause its sensitivity to decrease.

CHARACTERISTICS OF THE PUT

Table 3.III is a list of typical characteristics of Motorola's MPU131 series of programmable unijunction transistors. The test circuits and test conditions shown are essentially the same as for the data sheet characteristics. The data presented here defines the static curve shown in Figure 3.60(b) for a 10 V gate reference (V_S) with various gate resistances (R_G). It also indicates the leakage currents of these devices and describes the output pulse. Values given are for 25°C unless otherwise noted.

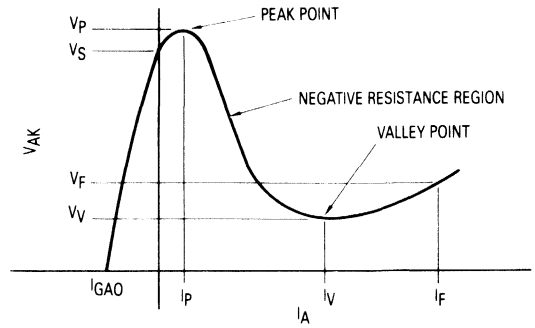


Figure 3.60(a). Static Characteristics

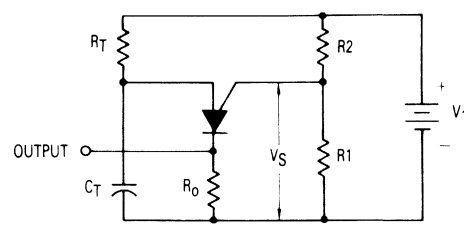


Figure 3.60(b). Typical Oscillator Circuit

Table 3.III. Typical PUT Characteristics

Symbol	Test Circuit Figure	Test Conditions	MPU131	MPU132	MPU133	Unit
I_P	3.64	R_G = 1 mΩ R_G = 10 kΩ	1.25 4	0.19 1.20	0.08 0.70	μA μA
I_V	3.64	R_G = 1 MΩ R_G = 10 kΩ	18 270	18 270	18 270	μA μA
V_{AG}		(See Figure 3.65)				
I_{GAO}		V_S = 40 V	See Figure 3.66			
I_{GKS}		V_S = 40 V	5	5	5	nA
V_F	Curve Tracer Used	I_F = 50 mA	0.8	0.8	0.8	V
V_O	3.67		16	16	16	V
t_r	3.68		40	40	40	ns

PEAK POINT CURRENT, (I_P)

The peak point is indicated graphically by the static curve. Reverse anode current flows with anode voltages less than the gate voltage (V_S) because of leakage from the bias network to the charging network. With currents less than I_P, the device is in a blocking state. With currents above I_P, the device goes through a negative resistance region to its on state.

The charging current, or the current through a timing resistor, must be greater than I_P at V_P to insure that a device will switch from a blocking to an on state in an oscillator circuit. For this reason, maximum values of I_P are given on the data sheet. These values are dependent on V_S temperature, and R_G. Typical curves on the data sheet indicate this dependence and must be consulted for most applications.

The test circuit in Figure 3.61 is a sawtooth oscillator which uses a 0.01 μF timing capacitor, a 20 V supply, an adjustable charging current, and equal biasing resistors (R). The two biasing resistors were chosen to give an equivalent R_G of 1 MΩ and 10 kΩ. The peak point current was measured with the device off just prior to oscillation as detected by the absence of an output voltage pulse. The 2N5270 held effect transistor circuit is used as a current source. A variable gate voltage supply was used to control this current.

VALLEY POINT CURRENT, (I_V)

The valley point is indicated graphically in Figure 3.60. With currents slightly less than I_V, the device is in an unstable negative resistance state. A voltage minimum occurs at I_V and with higher currents, the device is in a stable on state.

When the device is used as an oscillator, the charging current or the current through a timing resistor must be less than I_V at the valley point voltage (V_V). For this reason, minimum values for I_V are given on the data sheet for R_G = 10 kΩ. With R_G = 1 MΩ, a reasonable "low" is 2 μA for all devices.

When the device is used as an SCR in the latching mode, the anode current must be greater than I_V. Maximum values for I_V are given with R_G = 1 MΩ. All devices have a reasonable "high" of 400 μA I_V with R_G = 10 kΩ.

and is measured by increasing the current while the device is oscillating and recording the value at which oscillations stop. With the PUT, there was no measurable difference between these parameters. This is not necessarily true with a unijunction transistor.

The valley current does vary with circuit parameters and temperature as was true of I_P. Typical data sheet curves identify this dependence and are frequently used to approximate actual variations of I_V.

PEAK POINT VOLTAGE, (V_P)

The unique feature of the PUT is that the peak point voltage can be determined externally. This programmable feature gives this device the ability to function in voltage controlled oscillators or similar applications. The triggering or peak point voltage is approximated by

$$V_P \approx V_T + V_S,$$

where V_S is the unloaded divider voltage and V_T is the offset voltage. The actual offset voltage will always be higher than the anode-gate voltage V_{AG}, because I_P flows out of the gate just prior to triggering. This makes $V_T = V_{AG} + I_P R_G$. A change in R_G will affect both V_{AG} and $I_P R_G$ but in opposite ways. First, as R_G increases, I_P decreases and causes V_{AG} to decrease. Second, since I_P does not decrease as fast as R_G increases, the $I_P R_G$ product will increase and the actual V_T will increase.

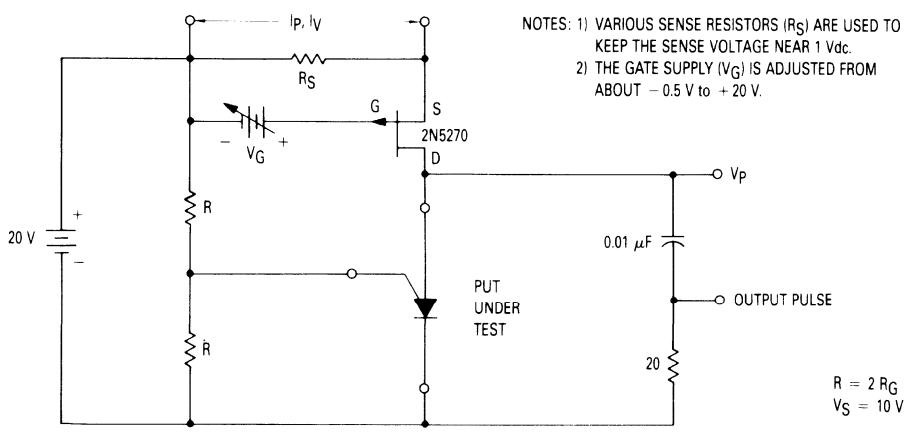


Figure 3.61. Test Circuit for I_P, V_P and I_V

LATCHING AND HOLDING CURRENT, (I_L, I_H)

Using the test circuit in Figure 3.61, an attempt was made to differentiate between latching current (I_L), holding current (I_H), and valley current. With the device latched on, reducing the current causes a voltage minimum which is the valley point. The device does remain on at lower currents until holding current (I_H) is reached. The holding current is measured as detected by the absence of an output voltage pulse just before oscillation occurs. The latching current is generally higher than I_H

These second order effects are difficult to predict and measure. Allowing V_T to be 0.5 V as a first order approximation gives sufficiently accurate results for most applications.

The peak point voltage was tested using the circuit in Figure 3.61 and a scope with 10 MΩ input impedance across the PUT. A Tektronix, Type W plug-in was used to determine this parameter.

FORWARD ANODE-GATE VOLTAGE, (V_{AG})

The forward anode-to-gate voltage drop affects the peak point voltage as was previously discussed. The drop is essentially the same as a small signal silicon diode and is plotted in Figure 3.62. The voltage decreases as current decreases, and the change in voltage with temperature is greater at low currents. At 10 nA the temperature coefficient is about −2.4 V/°C and it drops to about −1.6 mV/°C at 10 mA. This information is useful in applications where it is desirable to temperature compensate the effect of this diode.

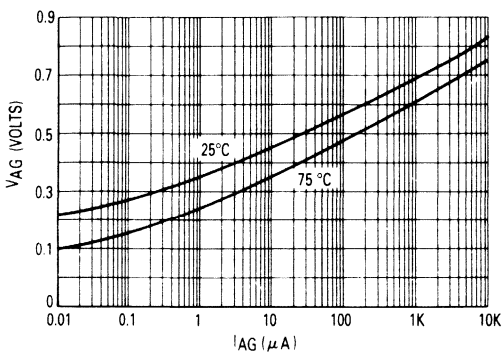


Figure 3.62. Voltage Drop of MPU131 Series

GATE-CATHODE LEAKAGE CURRENT, (I_{GKS})

The gate-to-cathode leakage current is the current that flows from the gate to the cathode with the anode shorted to the cathode. It is actually the sum of the open circuit gate-anode and gate-cathode leakage currents. The shorted leakage represents current that is shunted away from the voltage divider.

GATE-ANODE LEAKAGE CURRENT, (I_{GAO})

The gate-to-anode leakage current is the current that flows from the gate to the anode with the cathode open. It is important in long duration timers since it adds to the charging current flowing into the timing capacitor. The typical leakage currents measured at 40 V are shown in Figure 3.63. Leakage at 25°C is approximately 1 nA and the current appears to double for about every 10°C rise in temperature.

FORWARD VOLTAGE, (V_F)

The forward voltage (V_F) is the voltage drop between the anode and cathode when the device is biased on. It is the sum of an offset voltage and the drop across some internal dynamic impedance which both tend to reduce the output pulse. The typical data sheet curve shows this impedance to be less than 1 ohm for up to 2 A of forward current. This is essentially an order of magnitude better than the UJT which is closer to 20 ohms.

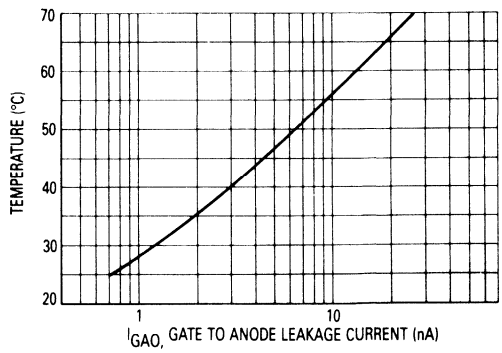


Figure 3.63. Typical Leakage Current of the MPU131, 132 and 133 Reverse Voltage Equals 40 V

PEAK OUTPUT VOLTAGE, (V_O)

The peak output voltage is not only a function of V_P, V_F and dynamic impedance, but is also affected by switching speed. This is particularly true when small capacitors (less than 0.01 μF) are used for timing since they lose part of their charge during the turn on interval. The use of a relatively large capacitor (0.2 μF) in the test circuit of Figure 3.64 tends to minimize this last effect. The output voltage is measured by placing a scope across the 20 ohm resistor which is in series with the cathode lead.

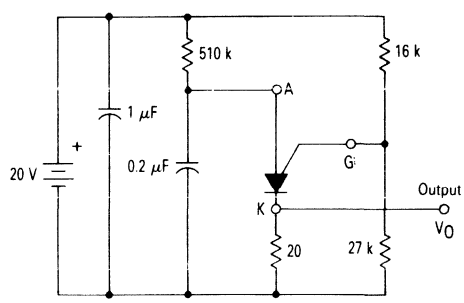


Figure 3.64. PUT Test Circuit for Peak Output Voltage (V_O)

RISE TIME, (t_r)

Rise time is a useful parameter in pulse circuits that use capacitive coupling. It can be used to predict the amount of current that will flow between these circuits. Rise time is specified using a sampling scope and measuring between 0.6 V and 6 V on the leading edge of the output pulse. Even fast scopes (100 MHz bandpass) degrade this measurement and readings must be corrected by calculations. It is preferable to use a 1000 pF capacitor and a sampling scope as shown in Figure 3.65 to read the 10% to 90% points directly. The resulting typical rise times of 40 ns are significantly better than those of the UJT which are about 100 ns.

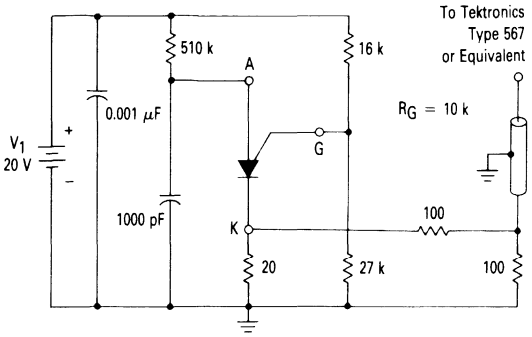


Figure 3.65. t_r Test Circuit for PUTs

MINIMUM AND MAXIMUM FREQUENCY

In actual tests with devices whose parameters are known, it is possible to establish minimum and maximum values of timing resistors that will guarantee oscillation. The circuit under discussion is a conventional RC relaxation type oscillator.

To obtain maximum frequency, it is desirable to use low values of capacitance (1000 pF) and to select devices and bias conditions to obtain high I_V. It is possible to use stray capacitance but the results are generally unpredictable. The minimum value of timing resistance is obtained using the following rule of thumb:

$$R_{(min)} = 2(V_1 - V_V)/I_V$$

where the valley voltage (V_V) is often negligible.

To obtain minimum frequency, it is desirable to use high values of capacitance (10 μF) and to select devices and bias conditions to obtain low I_P. It is important that the capacitor leakage be quite low. Glass and mylar dielectrics are often used for these applications. The maximum timing resistor is as follows:

$$R_{(max)} = (V_I - V_P)/2I_P$$

In a circuit with a fixed value of timing capacitance, our most sensitive PUT, the MPU133, offers the largest dynamic frequency range. Allowing for capacitance and bias changes, the approximate frequency range of a PUT is from 0.003 Hz to 2.5 kHz.

TEMPERATURE COMPENSATION

The PUT with its external bias network exhibits a relatively small frequency change with temperature. The uncompensated RC oscillator shown in Figure 3.66 was tested at various frequencies by changing the timing resistor R_T. At discrete frequencies of 100, 200, 1000 and 2000 Hz, the ambient temperature was increased from 25° to 60°C. At these low frequencies, the negative temperature coefficient of V_{AG} predominated and caused a consistent 2% increase in frequency. At 10 kHz, the frequency remained within 1% over the same temperature range. The storage time phenomenon which increases the length of the output pulse as temperature increases is responsible for this result. Since this parameter has not been characterized, it is obvious that temperature compensation is more practical with relatively low frequency oscillators.

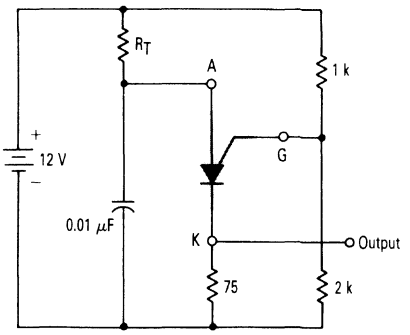
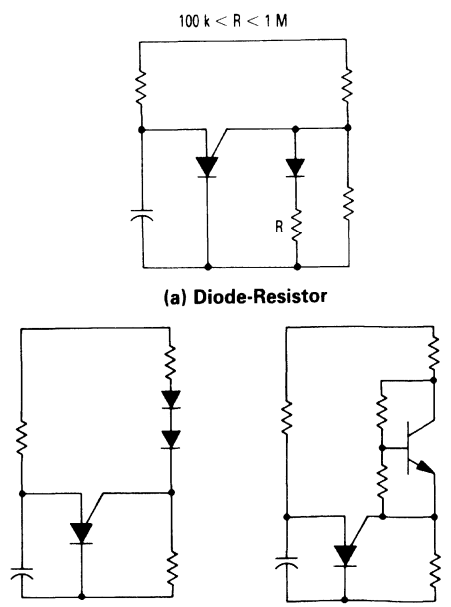


Figure 3.66. Uncompensated Oscillator

Various methods of compensation are shown in Figure 3.67. In the low cost diode-resistor combination of 3.67(a), the diode current is kept small to cause its temperature coefficient to increase. In 3.67(b), the bias current through the two diodes must be large enough so that their total coefficient compensates for V_{AG}. The transistor approach in 3.67(c) can be the most accurate since its temperature coefficient can be varied independently of bias current.



(a) Diode-Resistor

(b) Dual-Diode **(c) Transistor**

Figure 3.67. Temperature Compensation Techniques

TRIGGERS: SILICON BILATERAL SWITCH

THE SILICON BILATERAL SWITCH

The silicon bilateral switch (SBS) is an advanced semiconductor with negative resistance switching characteristics similar to the 3-layer diode, 4-layer diode and unijunction transistor (UJT). The latter devices have seen wide application, especially in triggering circuits where they can supply the fast rising, high-current gate pulse necessary for the proper operation of power thyristors. In such applications, the SBS can improve circuit performance and reduce cost at the same time.

These devices are not just an improved version of a PNPN diode. They are actually fabricated as simple integrated circuits consisting of transistors, diodes and resistors, connected as two anti-parallel, regenerative switches. Since the device is fabricated as an IC, the components are well matched resulting in an asymmetry, or difference of positive V_S and negative V_S, of less than 0.5 volts.

A third lead, designated the Gate, has been brought out for increased circuit flexibility. Since these devices are a regenerative switch, they may also be designed into many low power latching circuits.

The equivalent circuit diagram of an SBS and its symbol are shown in Figure 3.68. The device is actually a simple IC and consists of two halves of a PNP and an NPN transistor, a 6.8 volt zener diode and a 15 kΩ resistor, R_B. Unlike existing 4-layer diodes which use a stacked structure, the SBS is constructed using annular techniques. The result is a device with better stability and control of its electrical parameters.

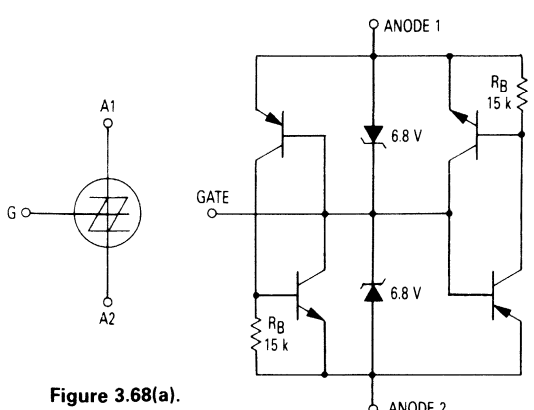


Figure 3.68(a). SBS Equivalent Circuit and Symbol

Figure 3.68(b)

Electrical characteristics are shown in Figure 3.70 and the parameters are defined as follows: V_S, the switching voltage, is the maximum forward voltage the device can sustain without switching to the conducting state; I_S, the switching current, is the current through the device when V_S is applied; V_F, the forward voltage, is the voltage drop across the device when it is in the conducting state and passing a specified current; I_H, the holding current, is the current necessary to sustain conduction; I_B is the leakage current through the device with five volts bias.

Operation of the SBS can be best understood by referring to Figures 3.69 and 3.70. Consider an adjustable source of voltage with a current limiting resistor in series supplying a voltage to a device anode 1 that is five volts positive with respect to anode 2. Since this voltage is less than the sum of V_{BE} of the PNP transistor and V_Z of the 6.8 volt zener diode, only a very small leakage current will flow and the device in the off or blocking state. As the supply voltage is increased, a point will be reached (near V_S) where a small increase in voltage results in a substantial increase in current flow. The PNP transistor purposely has high current gain and most of this increased current flows out of its collector and produces a voltage drop across R_B.

The two transistors are connected in a positive feedback loop similar to the equivalent circuit for an SCR

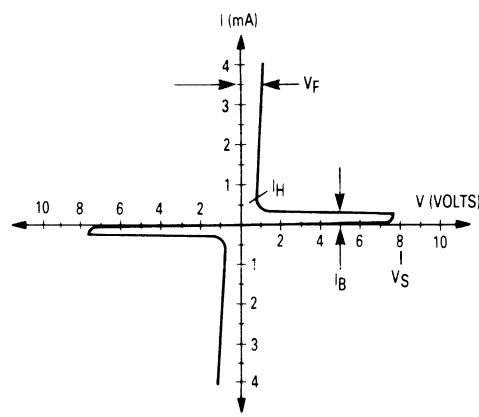


Figure 3.69. SBS Anode 1-Anode 2 V-I Characteristics

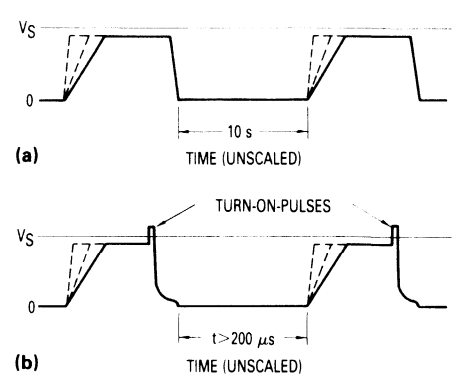


Figure 3.70. Waveforms for dv/dt Test

where the collector current of one is the base current for the other. When the voltage across R_B is sufficient to turn the NPN transistor on and the loop gain exceeds unity, both transistors are driven into saturation, the voltage across the device abruptly drops and the current through it is limited mainly by the external circuitry. The device has now switched to the on or conducting state.

The 6.8 volt zener diode has a positive temperature voltage coefficient which is opposite to that of V_{BE} of the PNP transistor. The net result is good temperature stability of V_S, typically +0.02%/°C.

V_F, the forward voltage across the device, remains relatively low even if the current through it is greatly increased, rising approximately 3 volts/ampere. The device will remain on until the current through it is reduced below the holding current value. One method of insuring turn-off is to apply a reverse voltage less than V_R, the maximum reverse voltage. After a few microseconds (turn-off time) have elapsed, the transistors will have recovered from saturation and the device will again block a forward voltage up to V_S.

A third lead, the gate, can be used to modify the characteristics of the SBS. As an example, connecting a 9.4 volt zener diode from gate to cathode would lower V_S to approximately 4.6 volts. Connecting a 20 kΩ resistor from gate to anode and a similar resistor from gate to cathode will lower V_S to approximately 4 volts at the expense of increased current around the device prior to switching. Also, if a voltage less than V_S is applied to an SBS it can be "gated" on by drawing a small current out of the gate lead.

Like other regenerative switches, the SBS has a tendency to switch on in the presence of rapidly rising anode voltage. The dv/dt rating of the SBS is difficult to define and the method of measurement may produce erroneous results. A test ramp of voltage with adjustable dv/dt as shown in Figure 3.70(a) may be applied to the device if not repeated more frequently than every 10 seconds. The device may switch to the on state when the dv/dt is in the range of 1 to 10 volts/microsecond. The repetitive waveform of (b) may be applied much more frequently (convenient for an oscilloscope display) providing only that the time interval between turn-off and the next ramp is longer than the turn-off time of the device. The turn-on pulse in (c) is necessary to discharge internal capacitance which can accumulate a charge and give false indication of very high dv/dt capability.

Sweeping an SBS in either direction will yield similar results. However, when an SBS has been conducting in one direction and the anode voltage is rapidly reversed, the dv/dt must be limited to approximately 0.1 volt/microsecond. This is necessary because if the transistors in the conducting half of the device have not recovered from saturation, they will provide a path for a current to turn the opposite side on.

CHAPTER 4
NEW THYRISTOR TECHNOLOGIES

1

THE SIDAC, A NEW HIGH VOLTAGE BILATERAL TRIGGER

The SIDAC is a high voltage bilateral trigger device that extends the trigger capabilities to significantly higher voltages and currents than have been previously obtainable, thus permitting new, cost-effective applications. Being a bilateral device, it will switch from a blocking state to a conducting state when the applied voltage of either polarity exceeds the breakover voltage. As in other trigger devices, (SBS, Four Layer Diode), the SIDAC switches through a negative resistance region to the low voltage on-state (Figure 4.1) and will remain on until the main terminal current is interrupted or drops below the holding current.

SIDAC's are available in the large MK1V series and economical, easy to insert, small MKP9V series axial lead packages. Breakdown voltages ranging from 104 to 280 V are available. The MK1V devices feature bigger chips and provide much greater surge capability along with somewhat higher RMS current ratings.

The high-voltage and current ratings of SIDACs make them ideal for high energy applications where other trigger devices are unable to function alone without the aid of additional power boosting components.

The basic SIDAC circuit and waveforms, operating off of ac are shown in Figure 4.2. Note that once the input voltage exceeds $V_{(BO)}$, the device will switch on to the forward on-voltage V_{TM} of typically 1.1 V and can conduct as much as the specified repetitive peak on-state current I_{TRM} of 20 A (10 μs pulse, 1 kHz repetition frequency).

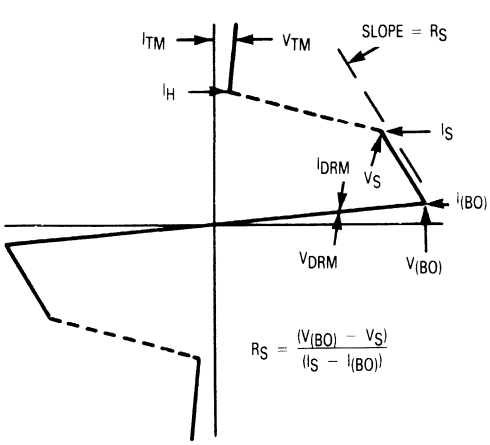


Figure 4.1(a). Idealized SIDAC V-I Characteristics

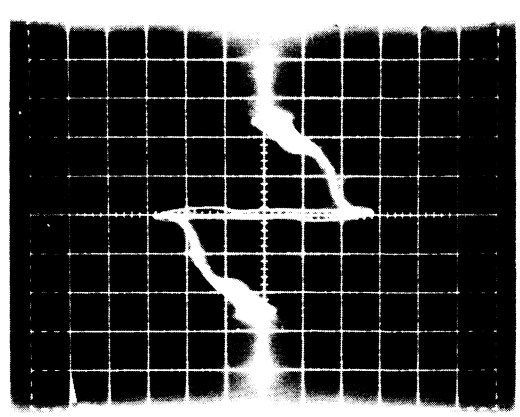


Figure 4.1(b). Actual MKP9V130 V-I Characteristic. Horizontal: 50 V/Division. Vertical: 20 mA/Division. (0,0) at Center. R_L = 14 k Ohm.

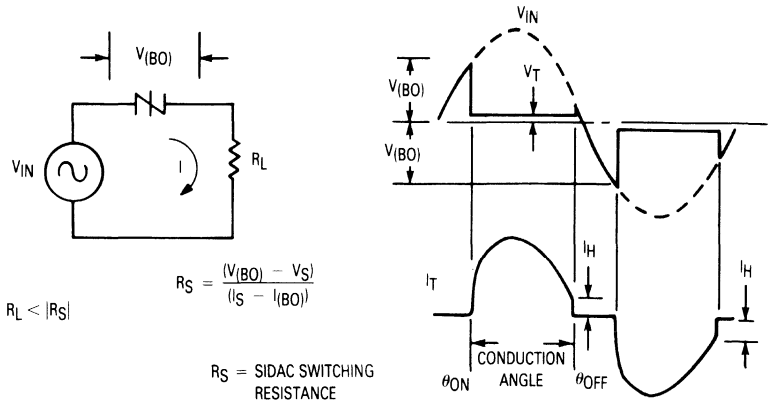


Figure 4.2. Basic SIDAC Circuit and Waveforms

Operation from an AC line with a resistive load can be analyzed by superimposing a line with slope $= -1/R_L$ on the device characteristic. When the power source is AC, the load line can be visualized as making parallel translations in step with the instantaneous line voltage and frequency. This is illustrated in Figure 4.3 where v_1 through v_5 are the instantaneous open circuit voltages of the AC generator and i_1 through i_5 are the corresponding short circuit currents that would result if the SIDAC was not in the circuit. When the SIDAC is inserted in the circuit, the current that flows is determined by the intersection of the load line with the SIDAC characteristic. Initially the SIDAC blocks, and only a small leakage current flows at times 1 through 4. The SIDAC does not turn-on until the load line supplies the breakover current ($I_{(BO)}$) at the breakover voltage ($V_{(BO)}$).

If the load resistance is less than the SIDAC switching resistance, the voltage across the device will drop quickly as shown in Figure 4.2. A stable operating point (V_T, I_T) will result if the load resistor and line voltage provide a current greater than the latching value. The SIDAC remains in an "on" condition until the generator voltage causes the current through the device to drop below the holding value (I_H). At that time, the SIDAC switches to the point (V_{off}, I_{off}) and once again only a small leakage current flows through the device.

Figure 4.4 illustrates the result of operating a SIDAC with a resistive load greater than the magnitude of its switching resistance. The behavior is similar to that described in Figures 4.2 and 4.3 except that the turn-on and turn-off of the SIDAC is neither fast nor complete. Stable operating points on the SIDAC characteristics

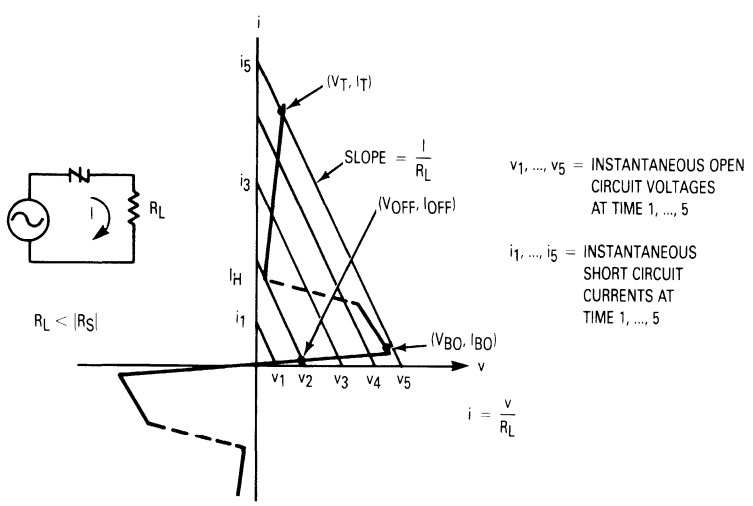


Figure 4.3. Load Line for Figure 4.2. (1/2 Cycle Shown.)

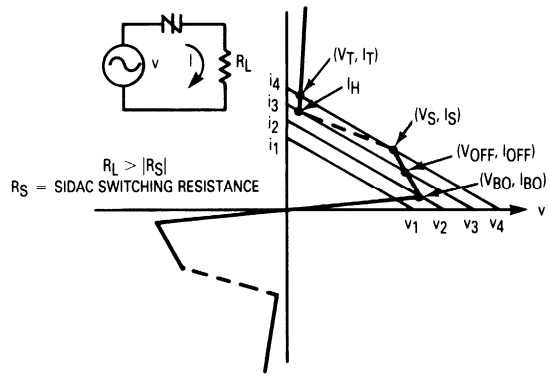


Figure 4.4. High Resistance Load Line with Incomplete Switching

between ($V_{(BO)}$, $I_{(BO)}$) and (V_S, I_S) result as the generator voltage increases from v_2 to v_4. The voltage across the SIDAC falls only partly as the loadline sweeps through this region. Complete turn-on of the SIDAC to (V_T, I_T) does not occur until the load line passes through the point (V_S, I_S). The load line illustrated in Figure 4.4 also results in incomplete turn-off. When the current drops below I_H, the operating point switches to (V_{off}, I_{off}) as shown on the device characteristic.

The switching current and voltage can be 2 to 3 orders of magnitude greater than the breakover current and on-state voltage. These parameters are not as tightly specified as V_{BO} and I_{BO}. Consequently operation of the SIDAC in the state between fully on and fully off is undesirable because of increased power dissipation, poor efficiency, slow switching, and tolerances in timing.

Figure 4.5 illustrates a technique which allows the use of the SIDAC with high impedance loads. A resistor can be placed around the load to supply the current required to latch the SIDAC. Highly inductive loads slow the current rise and the turn-on of the SIDAC because of their L/R time constant. The use of shunt resistor around the load will improve performance when the SIDAC is used with inductive loads such as small transformers and motors.

The SIDAC can be used in oscillator applications. If the load line intersects the device characteristic at a point where the total resistance (R_L + R_S) is negative, an unstable operating condition with oscillation will result. The resistive load component determines steady-state behavior. The reactive components determine transient behavior. Figure 4.10 shows a SIDAC relaxation oscillator application. The wide span between I_{BO} and I_H makes the SIDAC easy to use. Long oscillation periods can be achieved with economical capacitor sizes because of the low device $I_{(BO)}$.

Z1 is typically a low impedance. Consequently the SIDAC's switching resistance is not important in this application. The SIDAC will switch from a blocking to full on-state in less than a fraction of a microsecond.

The timing resistor must supply sufficient current to fire the SIDAC but not enough current to hold the SIDAC in an on-state. These conditions are guaranteed when the timing resistor is selected to be between R_{max} and R_{min}.

For a given time delay, capacitor size and cost is minimized by selecting the largest allowable timing resistor. R_{max} should be determined at the lowest temperature of operation because $I_{(BO)}$ increases then. The load line corresponding to R_{max} passes through the point ($V_{(BO)}$, $I_{(BO)}$) allowing the timing resistor to supply the needed breakover current at the breakover voltage. The load line for a typical circuit design should enclose this point to prevent sticking in the off state.

Requirements for higher oscillation frequencies and greater stored energy in the capacitor result in lower values for the timing resistor. R_{min} should be determined at the highest operating temperature because I_H is lower then. The load line determined by R and V_{in} should pass below I_H on the device characteristic or the SIDAC will stick in the on-state after firing once. I_H is typically more than 2 orders of magnitude greater than I_{BO}. This makes the SIDAC well suited for operation over a wide temperature span.

SIDAC turn-off can be aided when the load is an underdamped oscillatory CRL circuit. In such cases, the SIDAC current is the sum of the currents from the timing resistor and the ringing decay from the load. SIDAC turn-off behavior is similar to that of a TRIAC where turn-off will not occur if the rate of current zero crossing is high. This is a result of the stored charge within the volume of the device. Consequently, a SIDAC cannot be force commuted like an SCR. The SIDAC will pass a ring wave of sufficient amplitude and frequency. Turn-off requires the device current to approach the holding current gradually. This is a complex function of junction temperature, holding current magnitude, and the current wave parameters.

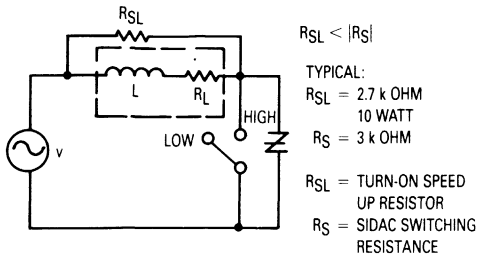


Figure 4.5. Inductive Load Phase Control

How can the SIDAC be used? One application is to replace the combination of a small-signal trigger and TRIAC with the SIDAC, as shown in Figure 4.6. In this example, the trigger — an SBS (Silicon Bidirectional Switch) that conducts at about 8 V — will fire the TRIAC by dumping the charge from the capacitor into the gate of the TRIAC. This circuit is amenable to phase controlling the TRIAC, if so required, as the RC time constant can be readily varied.

The simple SIDAC circuit can also supply switchable load current. However, the conduction angle is not readily controllable, being a function of the peak applied voltage and the breakover voltage of the SIDAC. As an example, for peak line voltage of about 170 V, at $V_{(BO)}$ of 115 V and a holding current of 100 mA, the conduction angle would be about 130°. With higher peak input voltages (or lower breakdown voltages) the conduction angle would correspondingly increase. For non-critical conduction angle, 1 A rms switching applications, the SIDAC is a very cost-effective device.

Figure 4.7 shows an example of a SIDAC used to phase control an incandescent lamp. This is done in order to lower the RMS voltage to the filament and prolong the life of the bulb. This is particularly useful when lamps are used in hard to reach locations such as outdoor lighting in signs where replacement costs are high. Bulb life span can be extended by 1.5 to 5 times depending on the type of lamp, the amount of power reduction to the filament, and the number of times the lamp is switched on from a cold filament condition.

The operating cost of the lamp is also reduced because of the lower power to the lamp; however, a higher wattage bulb is required for the same lumen output. The maximum possible energy reduction is 50% if the lamp wattage is not increased. The minimum conduction angle is 90° because the SIDAC must switch on before the peak of the line voltage. Line regulation and breakover voltage tolerances will require that a conduction angle longer than 90° be used, in order to prevent lamp turn-off under low line voltage conditions. Consequently, practical conduction angles will run between 110° and 130° with corresponding power reductions of 10% to 30%.

In Figure 4.2 and Figure 4.7, the SIDAC switching angles are given by:

$$\theta_{ON} = \sin^{-1}(V_{(BO)}/V_{pk})$$

where V_{pk} = Maximum Instantaneous Line Voltage

$$\theta_{OFF} = 180 - \sin^{-1}\left(\frac{(J_H \cdot R_L) + V_T}{V_{pk}}\right)$$

where θ_{ON}, θ_{OFF} = Switching Angles in degrees
V_T = 1 V = Main Terminal Voltage at $I_T = I_H$

Generally the load current is much greater than the SIDAC holding current. The conduction angle then becomes 180° minus $\theta_{(on)}$.

Rectifiers have also been used in this application to supply half wave power to the lamp. SIDAC's prevent the flicker associated with half-wave operation of the lamp. Also, full wave control prevents the introduction of a DC component into the power line and improves the color temperature of the light because the filament has less time to cool during the off time.

The fast turn-on time of the SIDAC will result in the generation of RFI which may be noticeable on AM radios operated in the vicinity of the lamp. This can be prevented by the use of an RFI filter. A possible filter design is shown in Figure 4.5. This filter causes a ring wave of current through the SIDAC at turn-on time. The filter inductor must be selected for resonance at a frequency above the upper frequency limit of human hearing and as low below the start of the AM broadcast band as possible for maximum harmonic attenuation. In addition, it is important that the filter inductor be non-saturating to prevent dI/dT damage to the SIDAC. For additional information on filter design see page 1-5-30 and Figure 5.34.

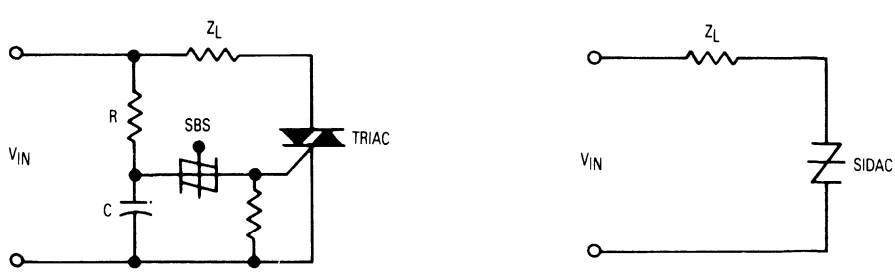


Figure 4.6. Comparison of a TRIAC and SIDAC Circuits

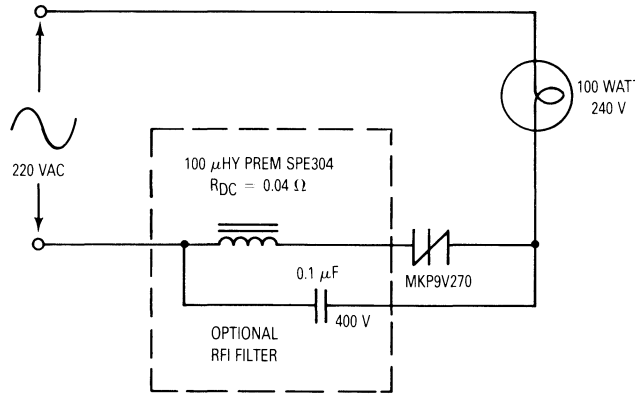


Figure 4.7. Long-Life Circuit for Incandescent Lamp

The sizing of the SIDAC must take into account the RMS current of the lamp, thermal properties of the SIDAC, and the cold start surge current of the lamp which is often 10 to 20 times the steady state load current. When lamps burn out, at the end of their operating life, very high surge currents which could damage the SIDAC are possible because of arcing within the bulb. The large MK1V device is recommended if the SIDAC is not to be replaced along with the bulb.

Since the MK1V series of SIDACs have relatively tight $V_{(BO)}$ tolerances (104 V to 115 V for the −115 device), other possible applications are over-voltage protection (OVP) and detection circuits. An example of this, as illustrated in Figure 4.8, is the SIDAC as a transient protector in the transformer-secondary of the medium voltage power supply, replacing the two more expensive back-to-back zeners or an MOV. The device can also be used across the output of the regulator (<100 V) as a simple OVP, but for this application, the regulator must have current foldback or a circuit breaker (or fuse) to minimize the dissipation of the SIDAC.

Another example of OVP is the telephony applications as illustrated in Figure 4.9. To protect the Subscriber Loop Interface Circuit (SLIC) and its associated electronics from voltage surges, two SIDACs and two rectifiers are used for secondary protection (primary protection to 1,000 V is provided by the gas discharge tube across the lines). As an example, if a high positive voltage transient appeared on the lines, rectifier D1 (with a P.I.V. of 1,000 V) would block it and SIDAC D4 would conduct the surge to ground. Conversely, rectifier D2 and SIDAC D3 would protect the SLIC for negative transients. The SIDACs will not conduct when normal signals are present.

Being a negative resistance device, the SIDAC also can be used in a simple relaxation oscillator where the frequency is determined primarily by the RC time constant (Figure 4.10). Once the capacitor voltage reaches the SIDAC breakover voltage, the device will fire, dumping the charged capacitor. By placing the load in the discharge path, power control can be obtained; a typical load could be a transformer-coupled xeon flasher, as shown in Figure 4.12.

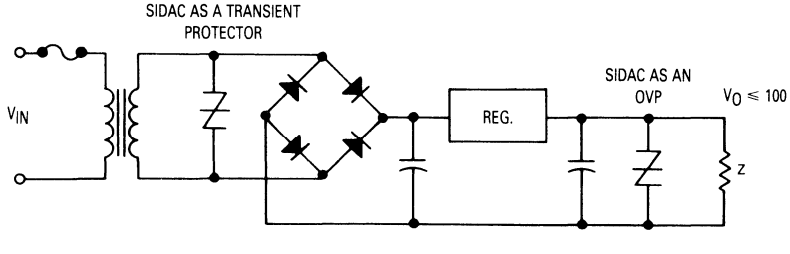


Figure 4.8. Typical Application of SIDACs as a Transient Protector and OVP in a Regulated Power Supply

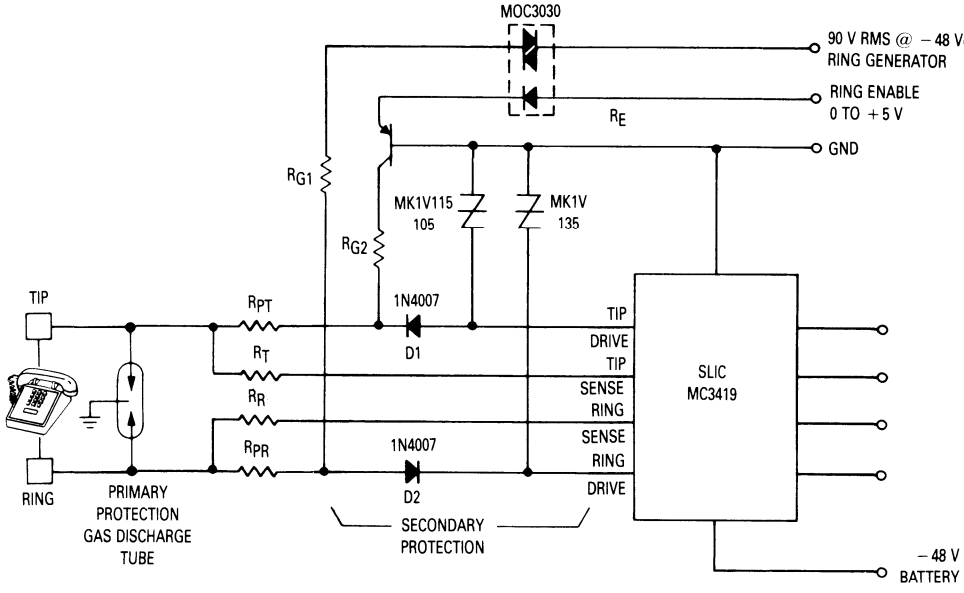


Figure 4.9. SIDACs Used for OVP in Telephony Applications

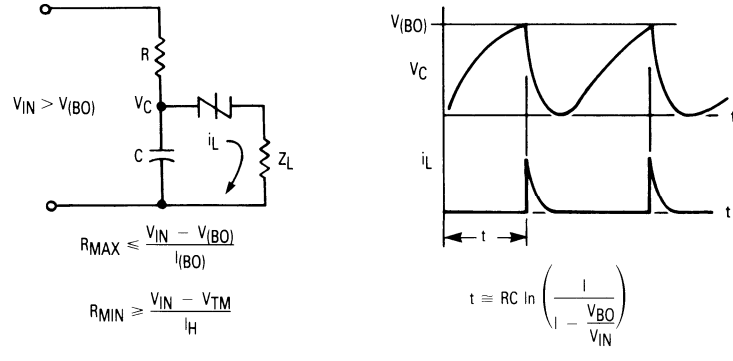


Figure 4.10. Relaxation Oscillator Using a SIDAC

SIDAC's provide an economical means for starting high intensity high pressure gas discharge lamps. These lamps are attractive because of their long operating life and high efficiency. They are widely used in outdoor lighting for these reasons.

Figure 4.13 illustrates how SIDAC's can be used in sodium vapor lamp starters. In these circuits, the SIDAC is used to generate a short duration (1 to 20 μs) high-voltage pulse of several KV or more which is timed by means of the RC network across the line to occur near the peak of the AC input line voltage. The high voltage pulse strikes the arc which lights the lamp.

In these circuits, an inductive ballast is required to provide a stable operating point for the lamp. The lamp is a negative resistance device whose impedance changes with current, temperature, and time over the first few minutes of operation. Initially, before the lamp begins to conduct, the lamp impedance is high and the full line voltage appears across it. This allows C to charge to the breakover voltage of the SIDAC, which then turns on discharging the capacitor through a step-up transformer generating the high voltage pulse. When the arc strikes, the voltage across the lamp falls reducing the available charging voltage across RC to the point where V_C no longer exceeds $V_{(BO)}$ and the SIDAC remains off. The low duty cycle lowers average junction temperature improving SIDAC reliability. Normal operation approximates non-repetitive conditions. However, if the lamp fails or is removed during replacement, operation of the SIDAC will be at the 60 Hz line frequency. The design of the circuit should take into account the resulting steady state power dissipation.

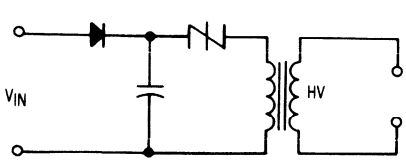


Figure 4.11. Typical Capacitor Discharge SIDAC Circuit

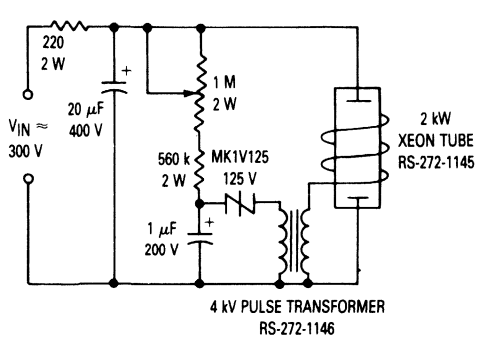
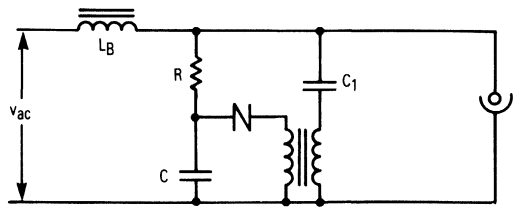
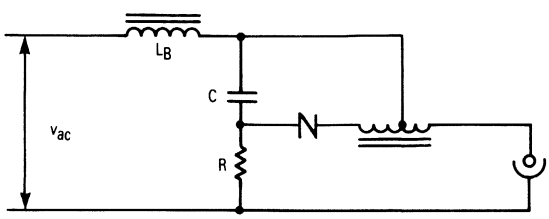


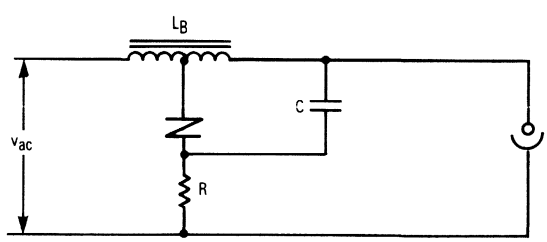
Figure 4.12. Xeon Flasher Using a SIDAC



(a). Conventional HV Transformer



(b). H.V. Auto-Transformer

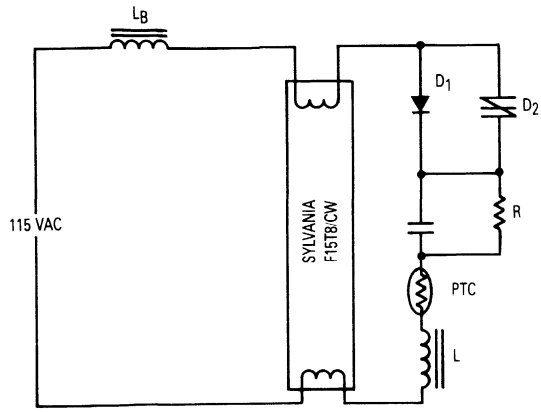


(c). Tapped Ballast Auto Transformer

Figure 4.13. Sodium Vapor Lamp Starter Circuits

Figure 4.14 illustrates a solid state fluorescent lamp starter using the SIDAC. In this circuit the ballast is identical to that used with the conventional glow-tube starter shown in Figure 4.15.

The glow tube starter consists of a bimetallic switch placed in series with the tube filaments which closes to energize the filaments and then opens to interrupt the current flowing through the ballast inductor thereby generating the high-voltage pulse necessary for starting. The mechanical glow-tube starter is the circuit component most likely to cause unreliable starting.



L_B	UNIVERSAL MFG CORP CAT200-H2 14-15-20-22 WATT BALLAST 325 mHY 28.9 Ω DCR
D1	1N4005 RECTIFIER
D2	MKP9V270 SIDAC
C	3 VFD 400 V
R	68 k OHMS 112 WATT
PTC	KEYSTONE CARBON COMPANY RL3006-50-40-25-PTO 50 OHMS/25°C
L	MICROTRAN QIL 50-F 50 mHY 11 OHMS

Figure 4.14. Fluorescent Starter Using SIDAC

The heating of the filaments causes thermonic emission of electrons from them. These electrons are accelerated along the length of the tube causing ionization of the argon gas within the tube. The heat generated by the starting current flow through the tube vaporizes the mercury droplets within the tube which then become ionized themselves causing the resistance and voltage across the tube to drop significantly. The drop in voltage across the tube is used to turn off the starting circuit and prevent filament current after the lamp is lit.

The SIDAC can be used to construct a reliable starter circuit providing fast, positive lamp ignition. The starter shown in Figure 4.14 generates high voltage by means of a series CRL charging circuit. The circuit is roughly analogous to a TRIAC snubber used with an inductive load, except for a lower damping factor and higher Q. The size of C determines the amount of filament heating current by setting the impedance in the filament circuit before ionization of the tube.

The evolution of this circuit can be understood by first considering an impractical circuit (Figure 4.16).

If L_B and C are adjusted for resonance near 60 Hz, the application of the AC line voltage will result in a charging current that heats the filaments and a voltage across the capacitor and tube that grows with each half-cycle of the AC line until the tube ionizes. Unfortunately, C is a large capacitor which can suddenly discharge through the tube causing high current pulses capable of destroying the tube filament. Also C provides a permanent path for filament current after starting. These factors cause short tube operating life and poor efficiency because of filament power losses. The impractical circuit must be modified to:

(1) Switch off the filament current after starting.

(2) Limit capacitor discharge current spikes.

In Figure 4.14 a parallel connected rectifier and SIDAC have been added in series with the capacitor C. The breakover voltage of the SIDAC is higher than the peak of the line voltage. Diode D1 is therefore necessary to provide a current path for charging C.

On the first half-cycle, C resonant charges through diode D1 to a peak voltage of about 210 V, and remains at that value because of the blocking action of the rectifier and SIDAC. During this time, the bleeder resistor R has negligible effect on the voltage across C because the RC time constant is long in comparison to the line period. When the line reverses, the capacitor voltage boosts the voltage across the SIDAC until breakover results. This results in a sudden step of voltage across the inductor L, causing resonant charging of the capacitor to a higher voltage on the 2nd half-cycle.

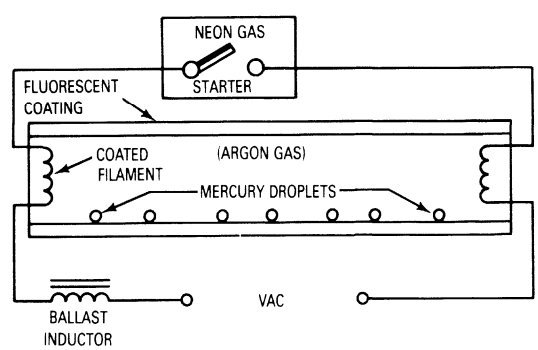


Figure 4.15. Fluorescent Lamp with Glow Tube Starter

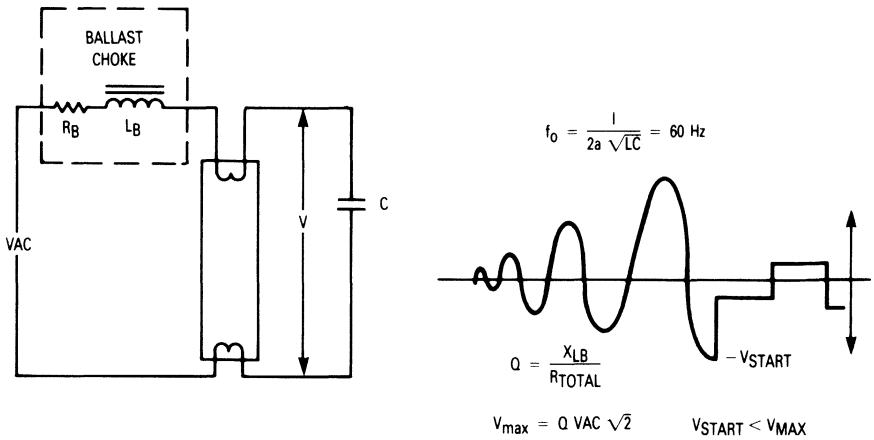
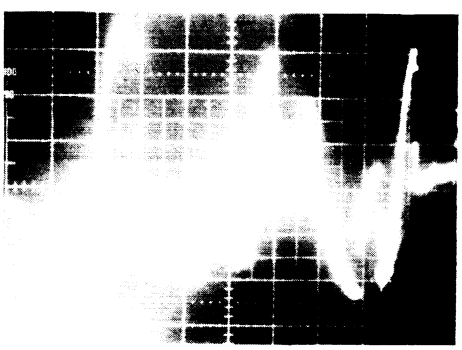
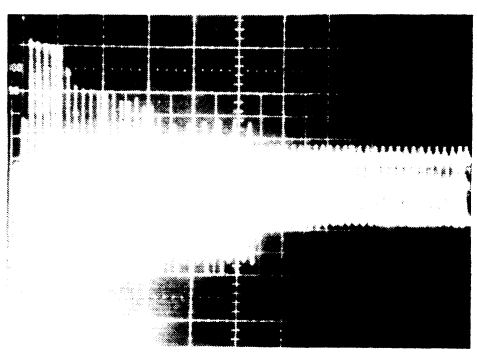


Figure 4.16. Impractical Starter Circuit



(a). 5 ms/DIVISION



(b). 100 ms/DIVISION

Figure 4.17. Starting Voltage Across Fluorescent Tube 100 V/DIV
0 V AT CENTER
V_{Line} = 110 V

Several cycles of operation are necessary to approach steady state operating conditions. Figure 4.17 shows the starting voltage waveform across the tube.

The components R, PTC, and L serve the dual role of guarantying SIDAC turn-off and preventing capacitor discharge currents through the tube.

SIDAC's can also be used with auto-transformer ballasts. The high voltage necessary for starting is generated by the leakage autotransformer. The SIDAC is used to turn-on the filament transformer initially and turn it off after ionization causes the voltage across the tube to drop.

Figure 4.18 illustrates this concept. The resistor R can be added to aid turn-off of the SIDAC by providing a small idle current resulting in a voltage drop across the impedance Z. The impedance Z could be a saturable reactor and or positive temperature coefficient thermistor. These components help to insure stability of the system comprised of the negative resistance SIDAC and negative resistance tube during starting, and promote turn off of the SIDAC.

The techniques illustrated in Figure 4.13 are also possible methods for generation of the necessary high-voltage required in fluorescent starting. The circuits

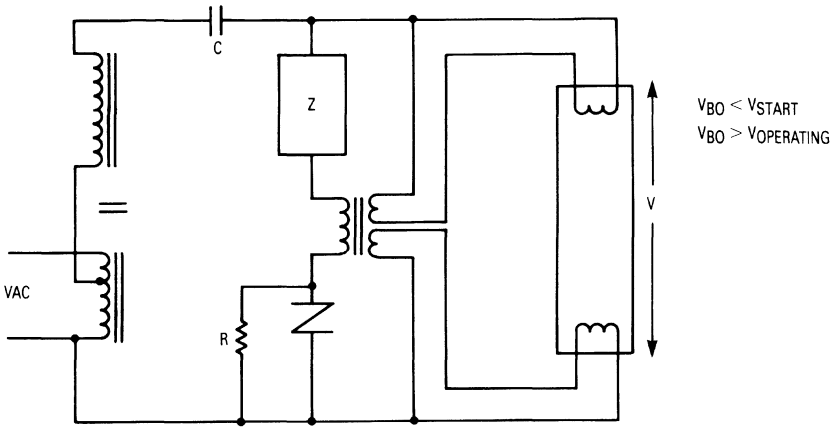


Figure 4.18. Fluorescent Starter Using SIDAC and Autotransformer Ballast

Table 4.1. Possible Sources for Thermistor Devices

Fenwal Electronics, 63 Fountain Street Framingham MA 01701
Keystone Carbon Company, Thermistor Division St. Marys, PA 15857
Thermometrics, 808 U.S. Highway 1 Edison, N.J. 08817
Therm-O-Disc, Inc. Micro Devices Product Group 1320 South Main Street, Mansfield, OH 44907
Midwest Components Inc., P.O. Box 787 1981 Port City Boulevard, Muskegon, MI 49443
Nichicon (America) Corp., Dept. G 927 E. State Pkwy, Schaumburg, IL 60195

must be modified to allow heating of the fluorescent tube cathodes if starting is to simulate the conditions existing when a glow tube is used.

Thermistors are useful in delaying the turn-on or insuring the turn-off of SIDAC devices. Table 4.1 shows possible sources of thermistor devices.

Other high voltage nominal current trigger applications are:

- Gas or oil igniters
- Electric fences
- HV electrostatic air filters
- Capacitor Discharge ignitions

Note that all these applications use similar circuits where a charged capacitor is dumped to generate a high transformer secondary voltage (Figure 4.11).

In many cases, the SIDAC current wave can be approximated by an exponential or quasi-exponential current wave (such as that resulting from a critically damped or slightly underdamped CRL discharge circuit). The question then becomes; how much "real world" surge current can the SIDAC sustain? The data sheet defines an I_{TSM} of 20 A, but this is for a 60 Hz, one cycle, peak sine wave whereas the capacitor discharge current waveform has a fast-rise time with an exponential fall time.

To generate the surge current curve of peak current versus exponential discharge pulse width, the test circuit of Figure 4.19 was implemented. It simulates the topology of many applications whereby a charged capacitor is dumped by means of a turned-on SIDAC to produce a current pulse. Timing for this circuit is derived from the nonsymmetrical CMOS astable multivibrator (M.V.) gates G1 and G2. With the component values shown, an approximate 20 second positive-going output pulse is fed to the base of the NPN small-signal high voltage transistor Q1, turning it on. The following high voltage PNP transistor is consequently turned on, allowing capacitor C1 to be charged through limiting resistor R1 in about 16 seconds. The astable M.V. then changes state for about 1.5 seconds with the positive going pulse from Gate 1 fed through integrator R2-C2 to Gate 3 and then Gate 4. The net result of about a 100 μs time delay from G4 is to ensure non-coincident timing conditions. This positive going output is then differentiated by C3-R3 to produce an approximate 1 ms, leading edge, positive going pulse which turns on NPN transistor Q3 and the following PNP transistor Q4. Thus, an approximate 15 mA, 1 ms pulse is generated for turning on SCR Q5 about 100 μs after capacitor charging transistor Q2 is turned off. The SCR now fires, discharging C1 through the current limiting resistor R4 and the SIDAC Device Under Test (D.U.T.). The peak current and its duration is set by the voltage V_C across capacitor C1 and current limiting resistor R4. The circuit has about a 240 V capability limited by C1, Q1 and Q2 (250 V, 300 V and 300 V respectively).

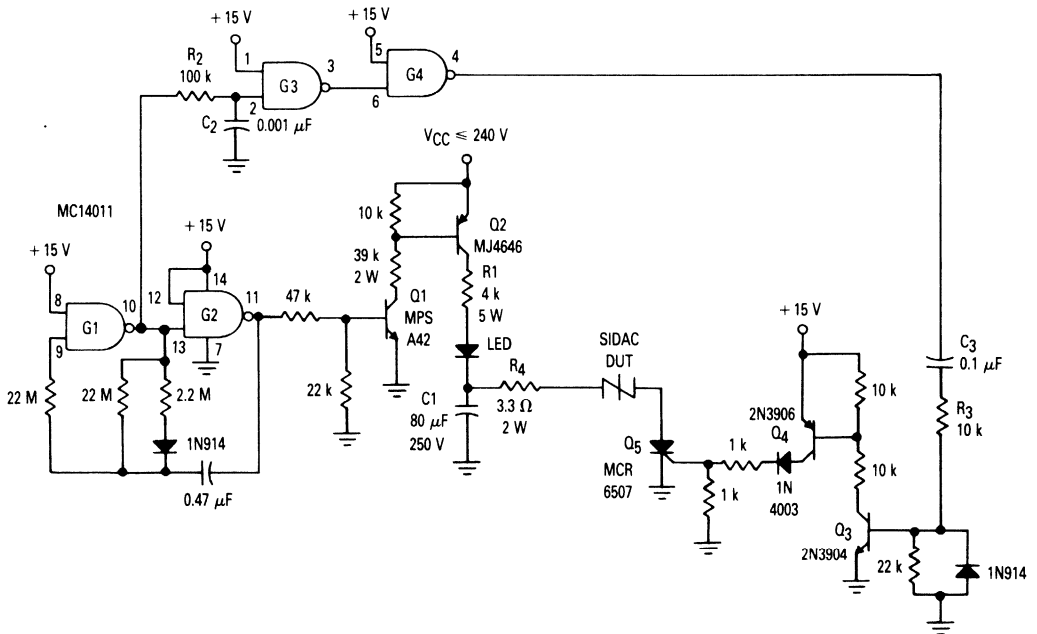


Figure 4.19. SIDAC Surge Tester

The SCR is required to fire the SIDAC, rather than the breakover voltage, so that the energy to the D.U.T. can be predictably controlled.

By varying V_C, C1 and R4, the surge current curve of Figure 15 was derived. Extensive life testing and adequate derating ensure that the SIDAC, when properly used, will reliably operate in the various applications.

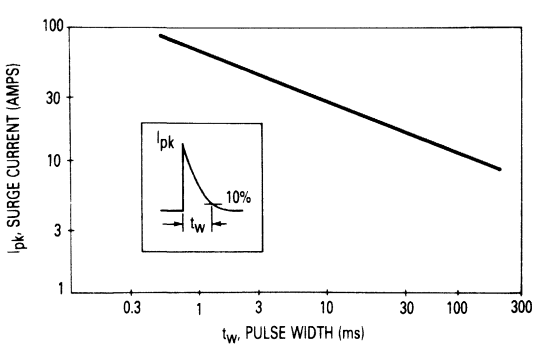


Figure 4.20. Exponential Surge Current Capability of the MK1V SIDAC. Pulse Width versus Peak Current

GTO DEVICES

Gate turn-off devices (GTOs) are thyristors which can be turned off as well as turned on by a gate signal. The symbol for a GTO is shown in Figure 4.21. Such devices were described as early as the 1960's, but they have only recently begun to see application in switching circuits.

Modern GTO devices are rugged efficient high voltage switches combining the benefits of regenerative operation with the turn-off ease of Bipolar Junction Transistors (BJTs). GTOs provide a blend of many of the most desirable characteristics of the SCR and the BJT. Since they can be turned off with a low power gate signal, they are excellent for pulse width modulation techniques in circuits that need a high-performance economical switch with the ruggedness of an SCR. The GTO should be considered wherever there is a need for a switch which can handle high pulsed power and moderate average power, with high switching SOA and excellent high-voltage switching speed.

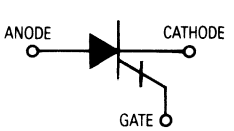


Figure 4.21. Symbol for GTO

Like the SCR, the GTO has momentary turn-on gate drive, latching, good surge handling ability, and low forward drop conduction losses at relatively high anode currents and die current densities (Figure 4.22). Like an SCR, conduction takes place by both holes and electrons injected into the respective P and N emitters of the device. The resulting high concentration of carriers and the regenerative action which holds the device in saturation allows it to operate at high current densities and that, in turn, allows a smaller chip size for a given switching capability.

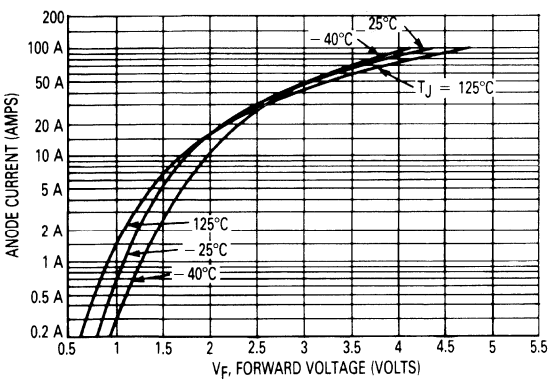


Figure 4.22. Maximum Forward Voltage versus Current
I_G = 300 mA, PW = 300 μs
Continuous Gate Drive

This results in a device with low internal capacitance and short turn-off storage delay times, high peak to average switching power and low material cost. The GTO can be an elegant solution to switching problems where other devices would require an expensive brute force approach.

Like a power transistor, the MGTO1000 Series has an interdigitated emitter geometry to aid turn-on current spreading and resist turn-on di/dt failure. Figure 4.23 shows the involute spiral pattern used.

The GTO also uses the clip and current spreading ring construction common to thyristors. This improves reliability under high surge current conditions, and results in a high device I^2t capability. The regenerative characteristic of the GTO prevents failure under surge current conditions because it cannot easily be pulled into the high dissipation active state common to transistor (BJT) devices. Consequently, GTOs can be protected by fuse techniques that are not usable with BJT devices.

Like the BJT, the GTO can be turned off by a low power drive signal. This eliminates the need for bulky, expensive, and inefficient commutation circuits that are needed in SCR forced commutation applications. The GTOs commutating dv/dt(c) and switching speed are an order of magnitude better than a conventional SCR. Unlike other thyristors, GTOs are nearly immune to turn-on by static dv/dt. This allows the use of a small snubber network and permits higher operating frequencies than with SCRs.

When a snubber is used, the GTO exhibits a dv/dt(c) sensitive turn-off switching SOA characteristic which is nearly independent of voltage. Even without a snubber it is possible to switch very high currents at moderate voltages at high temperatures. However in order to keep the dv/dt(c) stress within predictable limits, a small snubber is recommended.

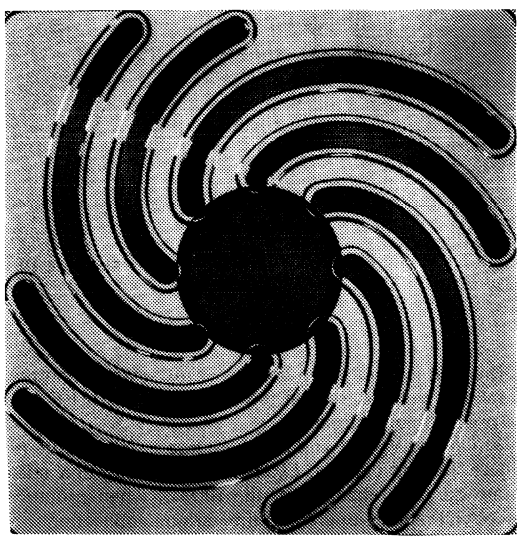


Figure 4.23. Involute Spiral Gate-Cathode Emitter Pattern Provides Constant Arm Width and Spacing

The GTO's attributes make it well suited for applications with large momentary stresses.

Such stresses sometimes arise as a consequence of the external environment not under the control of the circuit designer, or the stresses may be inherent in the design itself. *GTO ruggedness may permit simplified designs, allowing easy application of the device to less conditioned environments.

*Some sources of stress are listed in Table 4.2.

Table 4.2. Sources of Voltage or Current Stress

I. Resulting From Unexpected Circuit Fault
   1) Load short
   2) Stalled motor
   3) Transformer secondary with an open circuit

II. Characteristic of the Type of Application
   1) Non-linear loads
   2) Capacitative loads
   3) Capacitor discharge and crowbar protection circuits
   4) Fault protection by circuit breaking

III. Factors Under Control of the Designer
   1) Parasitic capacitance in the load circuit
   2) Discharge of the snubber network
   3) Diode recovery currents
   4) Parasitic inductance in wiring, snubber circuits, or load
   5) Lightning or transients due to interruption of other inductive loads on the same bus

HOW A GTO OPERATES

THE TWO-TRANSISTOR MODEL

Like most thyristors, the turn-on of a GTO can be described in terms of the two-transistor model (Figure 4.24a). This model also provides insight into the conditions necessary for turn-off. Turn-off occurs when the N-base current (Figure 4.24b) is reduced from the maximum provided by the PNP transistor (gate open) to less than the minimum required to saturate the NPN device (reverse gate current). When that happens, the gain of the device (the combined alpha of the two transistors) falls below unity and regeneration ceases.

However, the two-transistor model fails to provide an accurate estimate of the turn-off gain because the alphas are functions of the current density, spatial charge distribution, anode voltage and time.

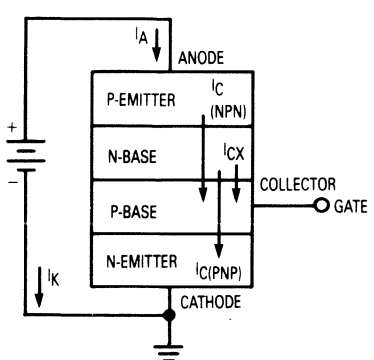


Figure 4.24(a). Turn-On

$I_A = I_K, I_G = 0$
$I_{C(PNP)} = \alpha_{PNP} I_A$
$I_{C(NPN)} = \alpha_{NPN} I_A$
$I_A = \alpha_{NPN} I_A + \alpha_{PNP} I_A + I_{CX}$

$$I_A = \frac{I_{CX}}{1 - (\alpha_{NPN} + \alpha_{PNP})}$$

WHEN $I_G > I_{GT}$ MOMENTARILY
$\alpha_{NPN} + \alpha_{PNP} > 1 \Rightarrow$ TURN ON
$\alpha_{NPN} + \alpha_{PNP} < 1 \Rightarrow$ FORWARD BLOCKING STATE

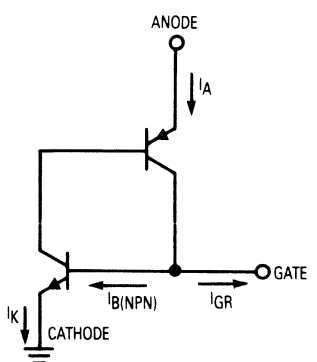


Figure 4.24(b). Turn-Off

MAX $I_{B(NPN)} = \alpha_{PNP} I_A$
MIN I_B TO SATURATE NPN $= (1 - \alpha_{NPN}) I_K$
CRITERION FOR UNSATURATION
$\alpha_{PNP} I_A - I_{GR} < (1 - \alpha_{NPN}) I_K$
BUT
$I_K = I_A - I_{GR}$
$(\alpha_{PNP} + \alpha_{NPN} - 1) I_A < \alpha_{NPN} I_{GR}$

$$\text{TURN-OFF GAIN} = G = \frac{I_A}{I_{GR}} = \frac{\alpha_{NPN}}{(\alpha_{PNP} + \alpha_{NPN} - 1)}$$

THE TWO DIMENSIONAL MODEL

Figure 4.25 gives additional insight into the switching process of a GTO. Here, the GTO is pictured as a series of smaller devices interconnected by lumped RC components that represent the spreading resistances and junction capacitances within the chip.

Early in the turn-on transient, conduction is not uniform across the entire chip area. Those portions of the emitter closest to the gate conduct first and most heavily. The turn-on of the more remote regions is delayed by the drive signal. All three junctions continue to conduct during the storage time interval until the excess carriers in the gate region have been removed and the gate-cathode junction recovers. Then the collector junction comes out of saturation and the anode current decreases rapidly during the fall time. During the tail (end region of the "fall time") time, the PNP transistor section of the GTO is biased in its active region while the remaining carriers in the N-base support conduction at low current magnitudes.

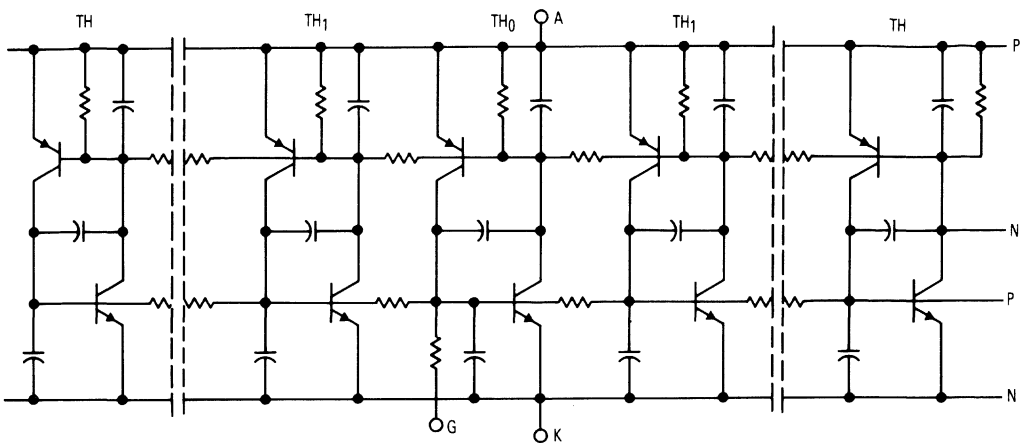


Figure 4.25. GTO Model with Junction Capacitance and Spreading Resistance Depicted as Lumped Elements

spreading resistance and distributed capacitance within the chip. The spiral geometry of the GTO minimizes the distance between the gate and emitter regions and reduces the time required for conduction to spread across the chip area. This enhances the capability of the device to conduct large, fast rise current pulses by reducing localized current densities and die temperatures.

The distributed thyristor model also applies to turn-off. Here the effect results in higher current densities under the emitter at its center rather than at the periphery.

GTO turn-off is initiated by applying reverse voltage to the gate-cathode junction to remove current and charge from the P-base. This results in an internal lateral voltage drop (Figure 4.26) which acts to turn on, or oppose, the reverse recovery of the gate-cathode junction. Because of this, recovery does not take place evenly across the entire junction area. Those regions closest to the gate recover first, resulting in a longer path and greater series resistance between the gate and the conducting area. The result is a "squeezing" effect that causes the current to be progressively concentrated in a narrow filament under the center of the cathode N-emitter stripe. Permanent damage to the device can result if the current density and power produces sufficient localized heating during this process.

The GTO does not respond instantly to the reverse gate

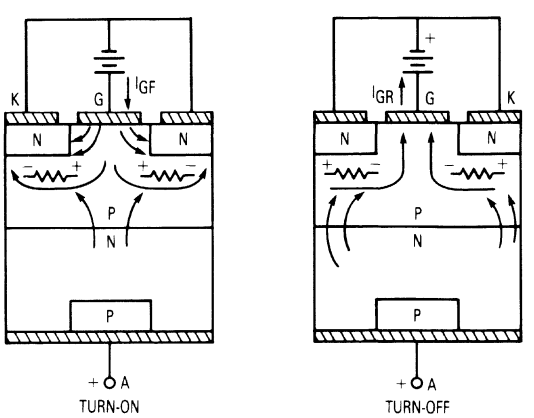


Figure 4.26. Lateral Drop at Turn-On and Turn-Off. At Turn-On, Drop Causes Heaviest Conduction at Cathode Edges. At Turn-Off, Current is Squeezed Away from the Gate-Cathode Periphery.

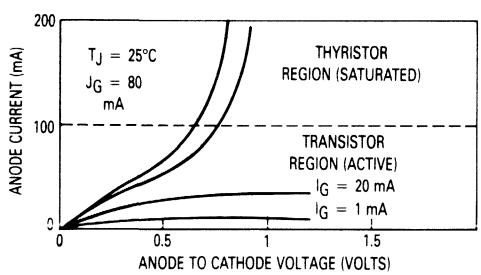
GTO FORWARD CHARACTERISTICS

TRANSISTOR REGION

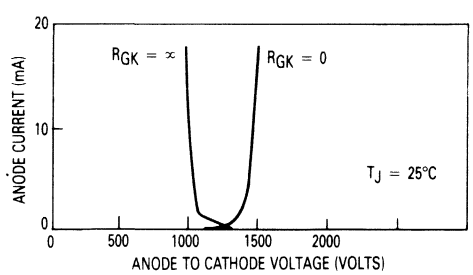
Figure 4.27 shows the anode characteristics of a MGTO1200. There are two regions of operation. At very low values of gate and anode current, the anode current is controlled by continuous gate drive. The anode characteristic is similar to a darlington BJT with base-emitter shunt resistance. The device does not latch, but its current gain increases as the anode current is made larger. Higher gate drive lowers the on-state resistance and forward voltage drop in this region and at moderately higher currents.

THYRISTOR REGION

When the anode current exceeds the latching current, the device enters the thyristor region of operation. The device saturates, allowing the anode current to be determined by the external load circuit. The gate current must momentarily exceed the minimum trigger current threshold to achieve operation in this region. Additional gate drive provides little benefit in reducing forward voltage after latching takes place and the anode current becomes large in comparison to the gate current.



(a). On-State Threshold Characteristic

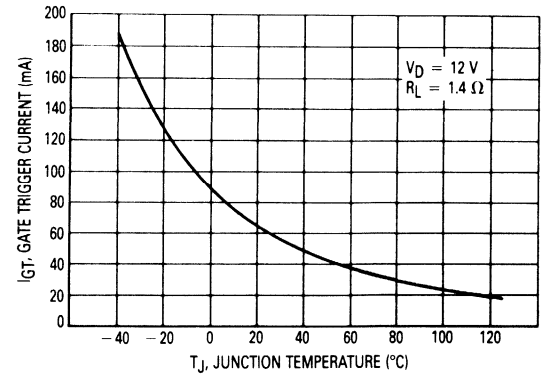


(b). Off-State Forward Blocking Characteristic

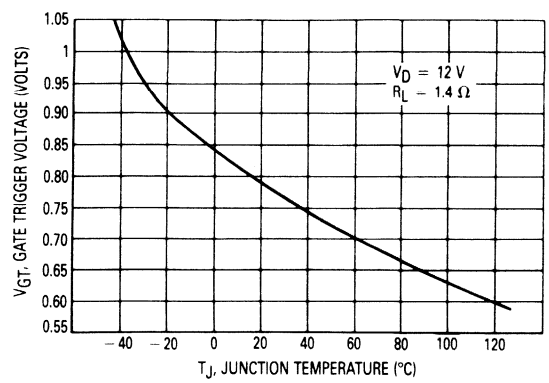
Figure 4.27. GTO Anode Characteristics

TURN-ON SWITCHING

Reliable triggering of the GTO requires that the turn-on gate current and voltage exceed the maximum specified values. Triggering requirements increase at low temperatures as shown in Figure 4.28. Consequently, the drive circuit should be designed to supply the needed



(a). Typical Gate Trigger Current

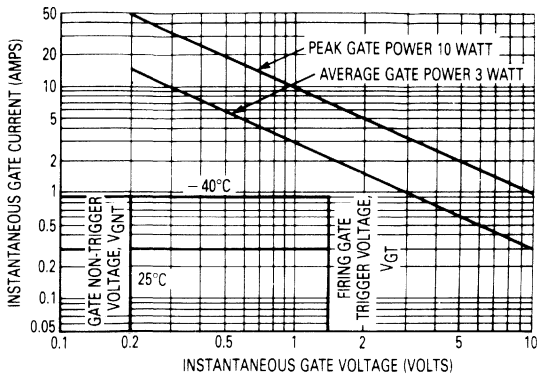


(b). Typical Gate Trigger Voltage

Figure 4.28. GTO Trigger Characteristics versus Temperature

drive at the lowest anticipated operating temperature. For example, to guarantee turn-on at −40°C, both the 900 mA and 1.5 volt conditions must be met simultaneously. The GTO's turn-on drive circuit load line should fall outside the 900 mA box in Figure 4.29. The maximum load line is set by the peak-forward gate-power rating and must lie within this safe operating area. At high operating frequencies or with continuous gate drive, average gate power will increase and needs to be kept within the three watt rating.

Standard thyristor practice has been to improve reliability and reduce di/dt failures by using a peak gate current two to ten times the minimum gate trigger current. This is a recommended practice in applications having a fast anode current rise rate and will reduce turn-on time and switching losses. The peak repetitive gate power rating sets the upper limit to the amount of gate overdrive that can be used to speed device turn-on.



FIRING CIRCUIT LOADLINE MUST FALL OUTSIDE BOX FOR CHOSEN MIN T_J AND INSIDE THE (V, I) CONSTRAINTS SET BY THE AVERAGE AND PEAK GATE POWER.

Figure 4.29. GTO Firing Characteristics

The gate current rise time should be faster than the anode current rise time to aid in spreading current conduction (Figure 4.30). During turn-on, the gate input impedance of the GTO appears inductive. Applications involving fast, high anode current spikes require measures to minimize the parasitic cathode inductance in the gate drive current loop. High values of turn-on dI_G/dT are most easily achieved by driving the gate with a high voltage compliance current source to overcome the gate circuit inductance.

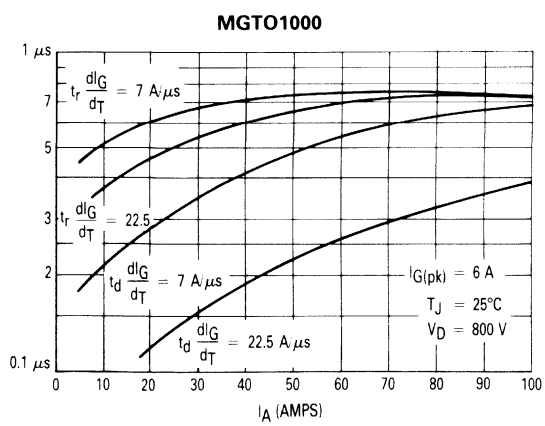


Figure 4.30. Turn-On Speed versus Gate Current Rise Time

The rate of GTO turn-on increases regeneratively with anode current. Moderate gate drive amplitudes result in comparable delay and rise times. Gate overdrive shortens the delay time (Figure 4.31) and should be used wherever the GTO is likely to face turn-on stress. Device regeneration improves the rise time versus current characteristic, causing it to be very flat with little slowdown at higher currents (Figure 4.32). GTOs switch quickly even under high overload conditions.

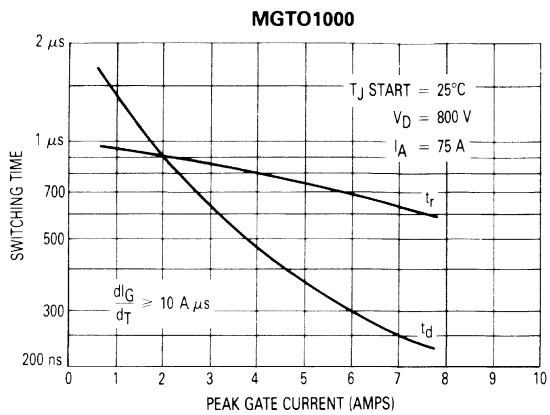


Figure 4.31. Effect of Peak Gate Current on Turn-On Time

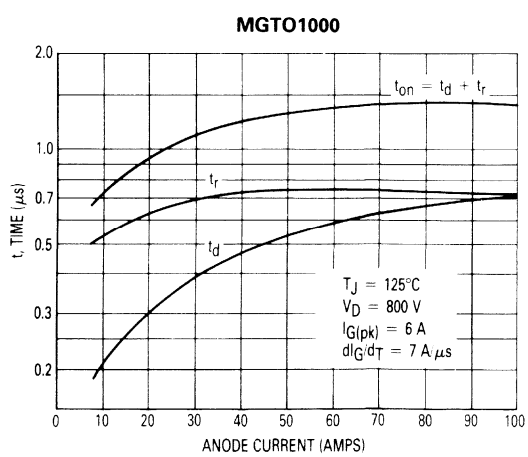
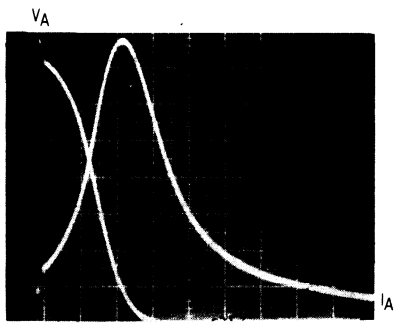


Figure 4.32. Typical Turn-On Switching Speed versus Anode Current

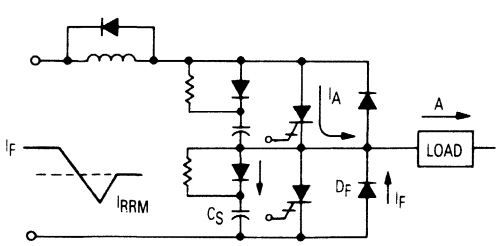
The GTO has excellent di/dt capability and may not require a series anode inductance to slow the current rise time (Figure 4.33). It is capable of switching an 800 volt, 100 ampere resistive turn-on load line (Figure 4.34). The temperature coefficient of the GTO's turn-on switching loss and on-state voltage is outstanding (Figure 4.35). The difference between room temperature and high temperature operation is nearly negligible at moderate to high currents. A dozen GTOs operated in parallel can switch a one megawatt pulse.



MGTO1000 Turn-On Snubber Discharge Transient, Inductive Load

0.2 μs/Div, 10 A/Div, f = 60 Hz, T_C = 40°C, $I_{A(pk)}$ = 70 A, C_S = 0.05 μF
R_S = 4.5 Ohm, V_C INITIAL = 770 V, $I_{GF(pk)}$ = 16 A, dI_{GF}/dT = 18 A/μs
dI_A/dT = 150 A/μs, TURN-ON ENERGY = 5.7 mJ

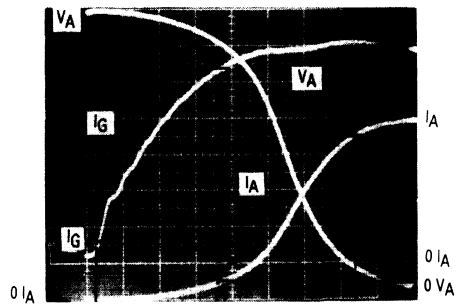
(a)



(b)

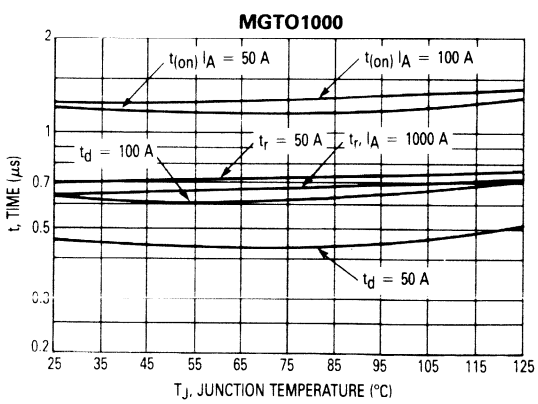
IN INVERTER APPLICATION DIODE RECOVERY, CURRENT AND SNUBBER CHARGING CONTRIBUTE TO GTO TURN-ON STRESS.

Figure 4.33. GTO Transient Handling Ability



V_D = 800 V, $I_{A(pk)}$ = 100 A, T_J START = 125°C
GATE CURRENT = 1 A/Div, ANODE CURRENT = 20 A/Div
ANODE VOLTAGE = 100 V/Div, t = 200 ns/Div
t_d = 720 ns, t_r = 720 ns, $E_{(on)}$ = 12.8 mJ, dI_G/dT = 7 A/μs

Figure 4.34. GTO Turn-On Waveform (Nonrepetitive)



V_D = 800 V, $I_{GF(pk)}$ = 6 A, $\frac{dI_{GF}}{dT}$ = 7 A/μs

Figure 4.35. Typical Turn-On Switching Time versus Temperature Junction

I_{TSM}

The non-repetitive sine wave surge characteristic (Figure 4.36) is intended to describe the capability of the GTO under unexpected fault conditions, such as those resulting from a short circuited load. Current surges of this magnitude should not be common or normal in the application. Under these conditions, the peak junction temperature will exceed the maximum rating and the part may not block voltage or regain gate control during, or immediately following, the surge. Operation at junction temperatures exceeding the maximum is permissible for short time periods, and the part will maintain its rated characteristics when the temperature returns to normal. This type of rating is traditional for thyristor devices and is included in the GTO ratings to allow comparison and to provide a measure of the extreme current conducting capability of the device. Protecting the device in these circumstances will be done by fuses rather than by its gate control capability. Interruption of the anode current is mandatory if the anode current exceeds the gate maximum non-repetitive current rating. An attempt at a gate controlled turn-off at currents above this level may cause the device to fail catastrophically.

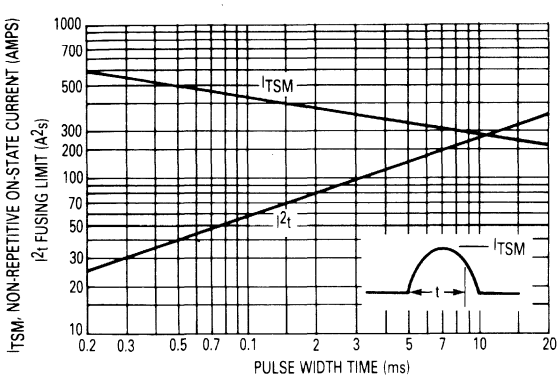
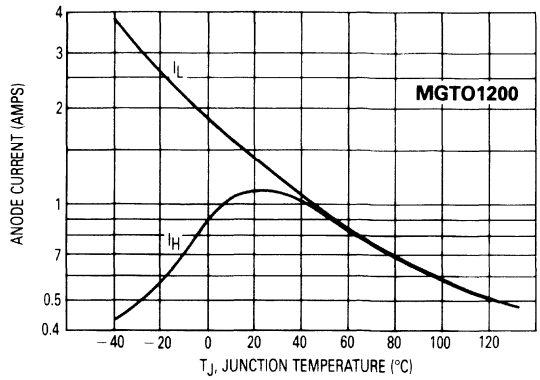


Figure 4.36. Non-Repetitive Surge Characteristic

LATCHING

Optimum GTO drive efficiency requires latching. This permits the reduction of the on-gate pulse width and duty cycle and results in lower average gate power.

GTO latching currents are higher than those of SCR devices. The gate current must be held at a value above I_{GT} until the anode current exceeds the latching value. Latching current depends on junction temperature (Figure 4.37) and is highest at low temperatures. The snubber discharge current can be used to aid in achieving latching when the load is strongly inductive and the anode current rise would otherwise be slow. In this case, the snubber discharge time constant must be selected to maintain the anode current above the latching value until the load current rises sufficiently to achieve the holding state. Alternatively, it may be feasible to shunt inductive loads with a lower impedance element to rapidly supply the latching current when the power losses are not prohibitive.



CONDITIONS:

V_D = 12 V
R_{GK} = ∞
GATE PW = 10 μs
ANODE PW = 300 μs
f = 60 Hz
$I_{G(pk)}$ = 1 A

Figure 4.37. Typical Latching Current

Continuous gate drive throughout the conduction cycle at an amplitude above the maximum specified I_{GT} value can also be used to prevent holding failure in situations where the load current could fluctuate to an unusual degree. However, this technique results in reduced drive efficiency.

Figure 4.38 illustrates an adapter that allows pulsed measurement of GTO latching and holding current on a Tektronix 576/176 curve tracer.

FORWARD BLOCKING

The blocking equation can be modified to include the effects of avalanche multiplication. The turn-on criterion becomes:

$$I_A = \frac{I_{CX}}{1 - (V_R/V_{BO})^N - \alpha NPN - \alpha PNP} \quad N \approx 1 \text{ to } 5$$

Avalanche multiplication works in conjunction with the device alphas to increase the possibility of unwanted turn-on, particularly at high voltages and high temperatures where alpha increases as a function of both leakage current and temperature.

The GTO and SCR share this blocking model. However, the GTO uses anode shorting techniques which reduce αPNP below that of an SCR. While blocking, conduction of the NPN transistor portion of the device is supported mainly through the anode shorting resistance across the P-emitter-N-base junction. This improves high temperature leakage characteristics. In addition, the high forward blocking voltage of the GTO provides a voltage margin in applications which do not require its full voltage capability.

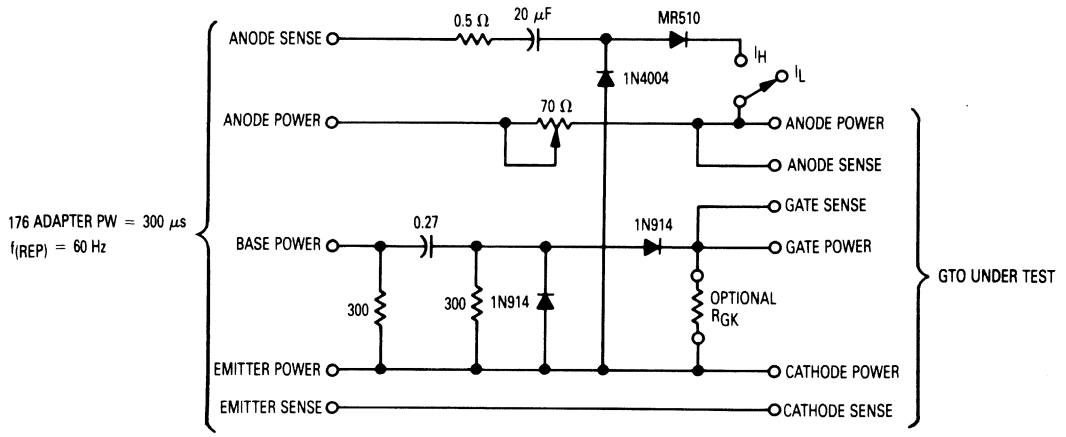


Figure 4.38. Curve Tracer Adapter for Measurement of Pulsed Latching and Holding Current with Reduced Heating Tolerances

The GTO exhibits sustaining voltage behavior (Figure 4.27) similar to that of a high voltage transistor. The anode current at high voltages depends on the effects of avalanche multiplication in the collector depletion layer and the transistor action. With the gate open-circuited, carriers freed by multiplication are acted upon by the NPN transistor gain, and result in lower blocking capability. Blocking voltage can be improved by 100 to 300 volts by providing a low gate termination resistance or, still better, a reverse bias.

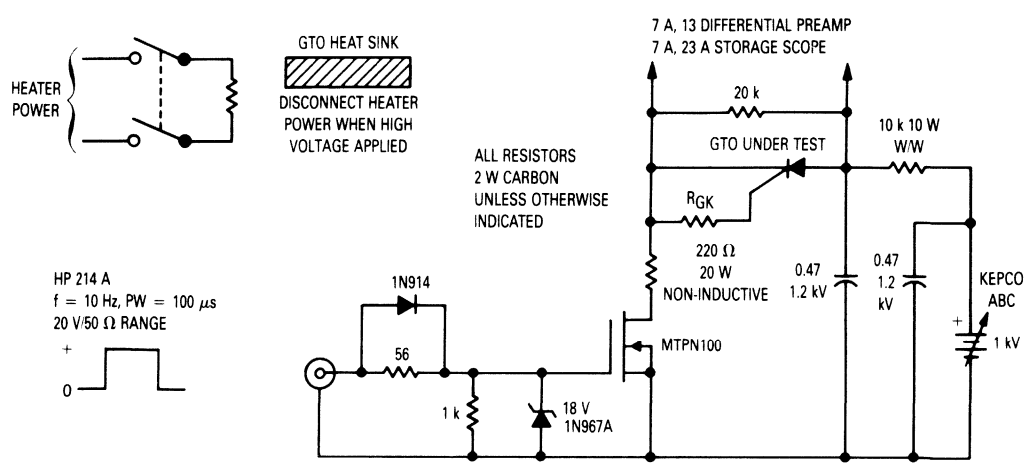
STATIC dv/dt(s)

Under extreme conditions, unwanted GTO turn-on can result from a rapid anode voltage spike even if its amplitude is below the device breakover region. This is a result of the current induced through device self-capacitance by the rapidly changing voltage. Snubber networks, which suppress rapid transients, are the common technique for preventing dv/dt(s) turn-on.

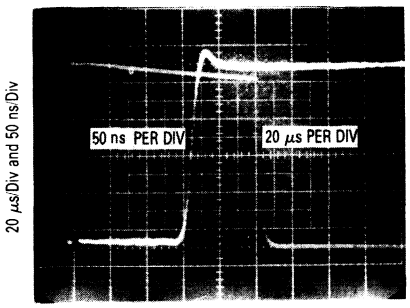
At values above 2000 V/microsecond, the GTO tends to respond to displaced internal charge and to the amplitude of the applied voltage rather than its rate. In this case, lower peak voltages reduce the possibility of unwanted turn-on more effectively than direct suppression of the rate of voltage rise.

dv/dt(s) performance depends strongly on the gate termination conditions. Low impedance values and gate reverse bias improve dv/dt(s) capability. Figure 4.39 shows the measurement circuit used.

Figure 4.39. Test Circuit and dv/dt(s) Characteristics of a GTO



(a) Linear Static dv/dt(s) GTO Test Circuit



200 V/Div, R_{GK} = 39 Ω, T_J = 128°C

Figure 4.39(b). Double Exposure Showing Static dv/dt(s) Waveforms

MGTO1000 Typical

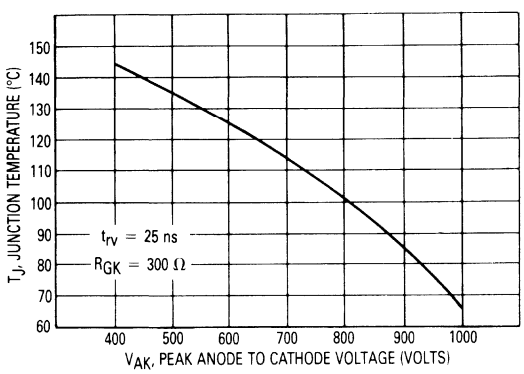


Figure 4.39(c). Linear dv/dt(s) MGTO1000 Typical

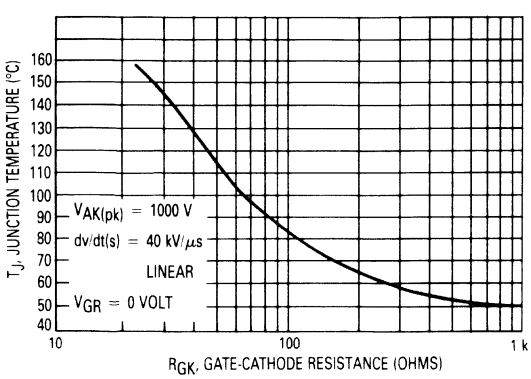


Figure 4.39(d). MGTO1000 Typical R_{GK} to Prevent dv/dt(s) Turn-On

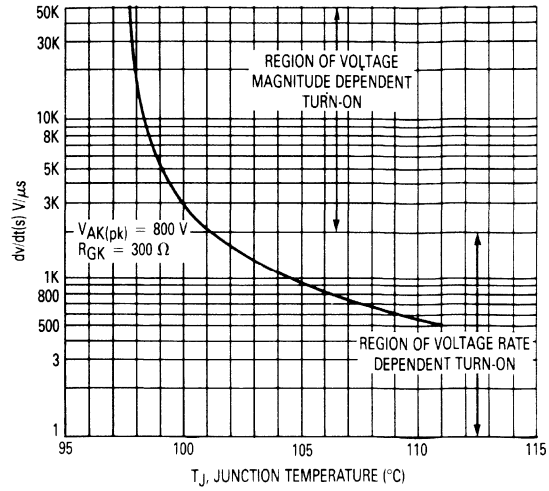


Figure 4.39(e). MGTO1000 Typical Linear dv/dt(s)

REVERSE BLOCKING AND CONDUCTING

The GTO is an asymmetrical part. Because of its shorted anode structure, the GTO's reverse blocking voltage capability is much lower than its capability in the forward direction. Its ability to block depends on the gate cathode termination conditions and approaches zero in circuits with no reverse gate voltage and zero ohms R_{GK}.

Applications requiring more than 15 volts reverse blocking capability require the addition of a series blocking diode. This increases conduction losses because of the additional diode forward drop (Figure 4.40).

Some applications will require reverse conducting capability. This is achieved by adding a "flywheel" or antiparallel diode with the necessary current handling ability and response time.

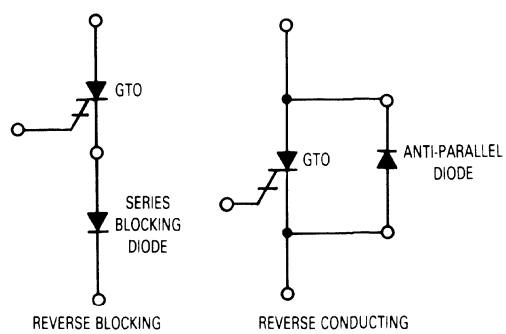
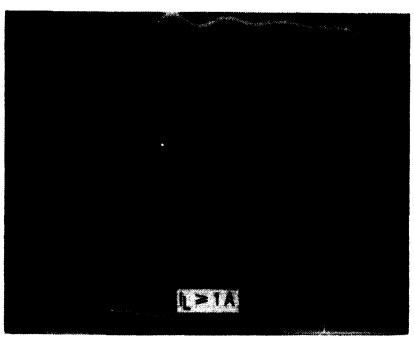


Figure 4.40. Modification of GTO Reverse Characteristic

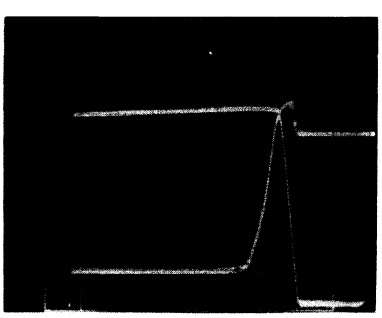
TURN-OFF SWITCHING

Inductive load switching results in a fast "kickback" voltage pulse, increasing stress on the switching device. Under these circumstances, preventing device failure is a paramount concern. Because simultaneous high voltages, currents and junction temperatures result during the turn-off transient, optimization of the drive circuit is recommended to reduce energy loss and improve efficiency. GTO performance depends on the drive and anode circuit conditions. Figure 4.41 illustrates typical switching performance.



T_C = 125°C, C_S = 0.068 μF, L_G = 2 μH, R_G = 3 Ω
V_D = 800 $V_{(pk)}$, I_A = 60 A_{pk}, PW = 100 μs, V_{GR} = 12 V
f = 50 Hz, L_A = 38 μH, 0.5 μs/Div, 10 A/Div, 100 V/Div

(a). GTO Snubbed Inductive Load Turn-Off



T_C = 125°C, $I_{A(pk)}$ = 110 A
V_D = 240 $V_{(pk)}$, PW = 100 μs, f = 10 Hz
1 μs/Div, 20 A/Div, 50 V/Div, L_A = 10 μH
L_G = 2 μH, R_G = 3 Ω, V_{GR} = 12 V

(b). GTO Unsnubbed Inductive Load Turn-Off

Figure 4.41. GTO Turn-Off Switching Under Inductive Loads

The GTO is a minority-carrier controlled device. Turn-off requires that the excess carriers stored in both base regions be removed or allowed to recombine.

An optimum turn-off drive circuit will apply a reverse bias across the gate-cathode junction for at least the entire duration of the anode transient or until a steady state blocking voltage results. Since blocking and immunity to dv/dt transients are improved by reverse bias, it is desirable to keep the gate-cathode junction reverse biased throughout the off period.

1

GTO MEASUREMENT AND DEVICE PROTECTION

SWITCHING MEASUREMENT

Figure 4.42 illustrates the drive circuit and terminal conditions used to evaluate GTO switching parameters. Figure 4.43 shows the circuit used for GTO turn-on and turn-off switching tests. However, a resistive load and a high voltage supply replaced the inductor, clamp and low voltage supply used for turn-off measurements. The snubber is used in both turn-on and turn-off measurements. It is important not to turn off the driver bias supplies while the anode circuit is still energized. Doing so will cause device failure by starving the reverse gate current.

DESCRIPTION OF THE MEASUREMENT CIRCUIT

A coil charge time of 150 microseconds was used for the turn-off measurements to insure complete GTO saturation and to provide worst case switching estimates characteristic of saturated mode switching.

Turn-off is initiated by applying reverse voltage from a low impedance source through a gate current slowdown ($dI_G/dT = V_{GR}/L_G$) inductor.

On the anode side of the circuit, a polarized snubber was used. Turn-off dv/dt is determined by the snubber and can be solved for as:

$dv/dt(c) = I_{pk}/C$.

The size of the anode inductor depends on the desired peak anode current. This inductor must be selected to maintain the flyback voltage duration beyond the tail time of the GTO. More inductance is required for lower test currents. The size of the inductor can be estimated by:

$L > (t_{off} \times V_{clamp}) / I_{pk}$

The clamp was used to insure accurate definition of the GTO peak anode voltage rise. This improves measurement repeatability, prevents avalanche of the GTO and provides freedom in the selection of the load inductor size. Without a clamp, the peak voltage will approach

$$V_{pk} = I_{pk} \left(\frac{L}{C_s} \right)^{1/2}$$

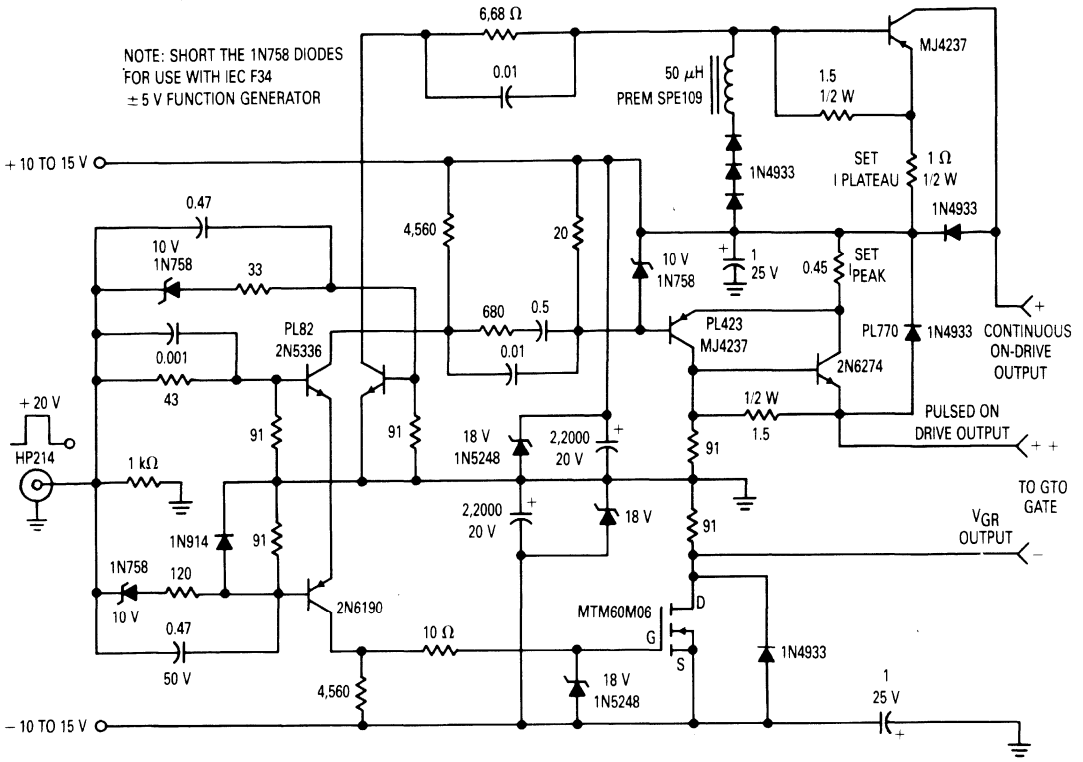
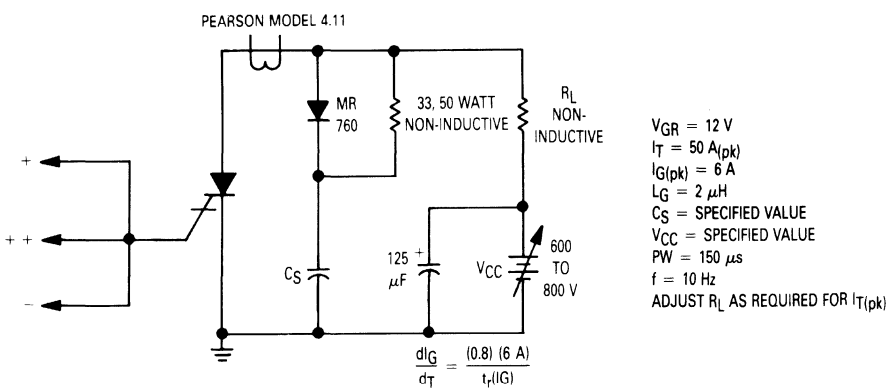
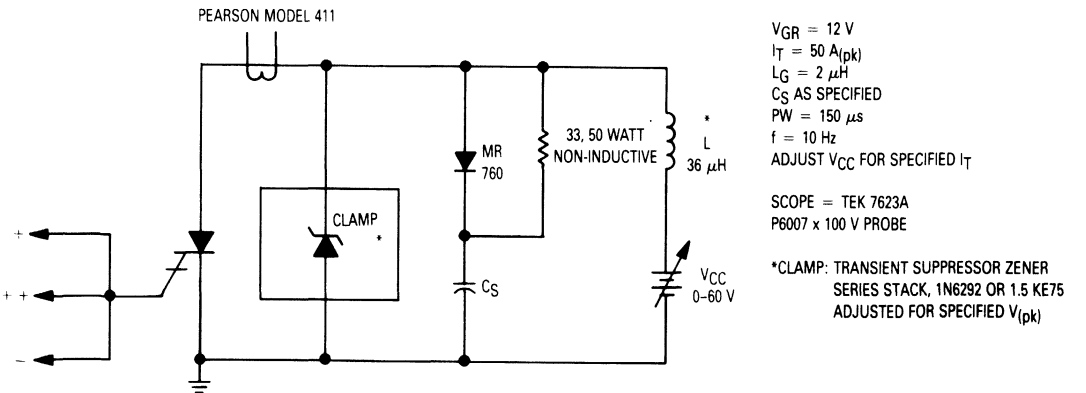


Figure 4.42. GTO Laboratory Driver. All R's 2 W Non-Inductive. (4,560) Indicates Parallel Resistor Combination. All Capacitors μF unless otherwise noted.



(a). Resistive Switching Test Circuit (Turn-On)



(b). Inductive Switching Test Circuit (Turn-Off)

Figure 4.43. GTO Test Circuit

TURN-OFF PARAMETERS AND CHARACTERISTICS

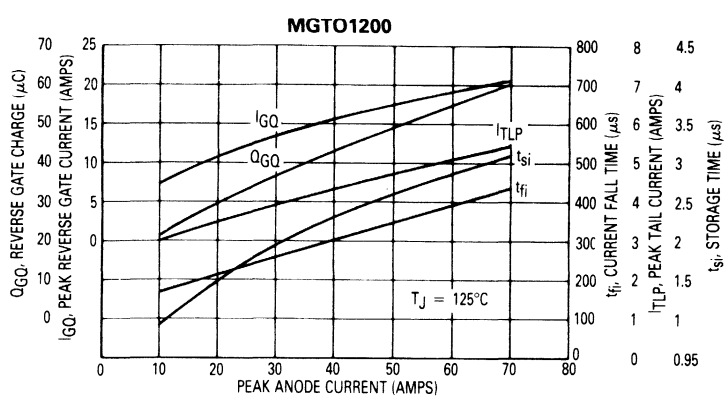
Q_{GQ} is the amount of charge per turn-off cycle removed from the gate of the GTO through the storage and fall time intervals (Figure 4.44). A small amount of additional charge will be removed because of current tailing.

For constant L_G and V_{GR}, Q_{GQ} is directly proportional to the peak anode current prior to turn-off.

Higher values of V_{GR} will increase the peak gate reverse current (I_{GQ}) and lower the turn-off gain (BR) but will not rapidly increase the total recovered charge.

This is due to a shortening of the storage and fall time, which reduces the number of charge carriers injected from the P-emitter and the proportion recovered through the gate.

The maximum value of steady-state gate reverse bias is limited by the avalanche of the gate-cathode junction and by the gate maximum ratings. Typical GTO gate-cathode voltage breakdowns are large to facilitate turn-off. Driving the gate-cathode junction beyond avalanche does not benefit switching and only serves to increase the gate power dissipation, reduce drive efficiency and raise junction temperature.



C_S = 0.1 μF, $V_{(pk)}$ = 800 V, T_J = 125°C, L_G = 2 μH

R_G = 3 Ω, V_{GR} = 12 V, PW = 150 μs

Figure 4.44. Typical Turn-Off Dynamics (Inductive Load)

The gate current slowdown inductor, L_G, influences most of the turn-off parameters. This inductor, along with the reverse turn-off voltage supply, determines the rate of change of gate current during the initial part of the turn-off transient, until the rising gate-cathode impedance dominates the current response and stops the linear ramp.

L_G provides an additional momentary inductive voltage kick that aids the turn-off voltage supply by avalanching the gate cathode junction at the moment the reverse gate current reaches maximum and begins its rapid decline. This aids in preventing the attenuation of the reverse gate current by the rising cathode impedance. The duration of this pulse can be adjusted by adding a clamping resistor across the gate inductor. This technique maximizes the instantaneous turn-off voltage without the drawbacks associated with the use of a high V_{GR} supply.

L_G is also a gate-cathode recovery slow-down inductor. When it slows the rise of the reverse gate current, it also delays the recovery of the gate-cathode junction, which leads to longer storage and fall times. Those effects can be undesirable. Still, there are benefits from the use of L_G. They include preventing early recovery of the cathode emitter at only those regions near the gate periphery.

L_G reduces localized heating and helps hold the die temperature even. When the GTO begins the turn-off process, reverse gate current and the internal lateral voltage drop focus the current into the area under the center of the cathode emitter stripes. If the current density and applied voltage go high enough, localized heating will permanently damage the device. The gate recovery slowdown inductor helps prevent this by reducing and delaying the instantaneous amplitude of the reverse gate current to insure a more homogenous turn-off of the cathode.

When L_G and V_{GR} are constant, the peak gate reverse current in the GTO will increase slowly with anode current as shown in Figure 4.44. The turn-off gain can be raised by using a larger L_G, which also results in a longer storage time. Q_{GQ} increases slightly for larger L_G values because of the increase in t_S.

Consequently, it is not necessary to greatly increase the drive to the GTO to achieve operation in overload situations. The peak reverse gate current that must be conducted by the turn-off drive transistor can be reduced by the selection of larger values of L_G. However, this will not reduce the average current required from the turn-off supply.

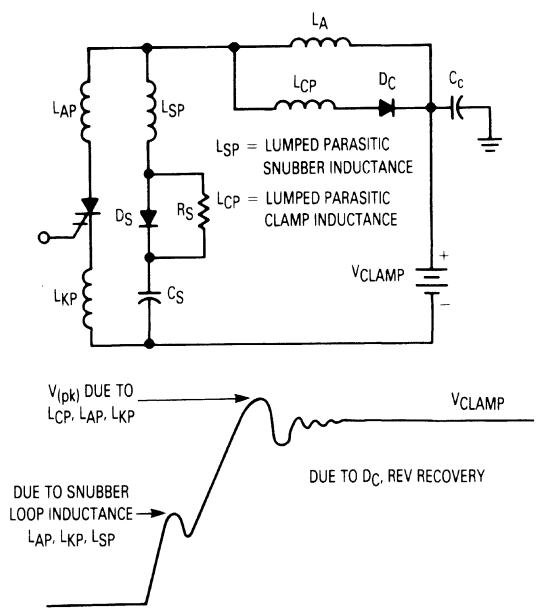
In other words, there are counter balancing considerations in selecting the gate recovery inductor. It should be small to reduce storage time and dissipation during fall time, but it should be large to improve switching energy handling ability, gate drive efficiency and turn-off gain. The reverse gate current will usually be higher than the reverse base current in similar darlington drive configurations. However the peak current flows for only a few microseconds and does not require the drive circuit to handle high average current or power. The reverse gate charge recovered from a GTO compares favorably with that observed in darlingtons with turn-off speed-up diodes.

Control of I_{TLP} and the tail time duration is of particular importance in inductive switching applications because the anode voltage is often very high and the "tail" can result in heating and device failures.

Larger values of L_G result in reductions in tail current magnitude. The increase in dissipated energy during the resulting longer fall time counterbalances the benefits of reduced tail time dissipation and also suggests an upper limit on the size of L_G. L_G must be small enough to permit enough reverse gate current to exceed the threshold necessary to unsaturate the device and start turn-off. The peak reverse gate power rating may set the lower limit to the size of the gate inductor in some applications. Reverse gate current can approach the magnitude of the anode current and lead to gate failure if no limiting is used.

In some situations, it may be better to have a slower current fall time. High turn-off di/dt can lead to increased GTO voltage stress due to increased parasitic inductance in the snubber and clamp circuits, which can cause overshoot when these elements are switched on (Figure 4.45). These spikes can be largely eliminated by circuit layout techniques which are not difficult at the 50 ampere level.

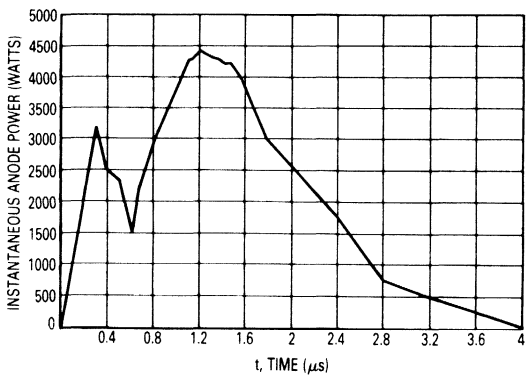
The tail current is a function of the peak anode current prior to turn off, junction temperature and the rate-of-rise of the anode voltage. It increases with any of these.



ABERRATIONS IN THE FLYBACK VOLTAGE WAVEFORM CAUSE INCREASED POWER DISSIPATION AND GTO STRESS. THIS PROBLEM CAN BE REDUCED BY LAYOUT TECHNIQUES AND COMPONENT SELECTION TO MINIMIZE THE PARASITICS SHOWN.

Figure 4.45. Effects of Undesirable Parasitic Circuit and Component Inductance at Turn-Off Time

Figure 4.46 is a plot of power versus time for an operating GTO. The first peak in the curve corresponds to the fall time and the second, larger peak to the tail time. In the example, the tail time is the major contributor to turn-off energy dissipation. Similar waveforms were integrated to generate the switching loss curves (Figure 4.49).



PEAK ANODE CURRENT = 50 A, AVERAGE ANODE CURRENT = 17.1 A
T_C = 81°C, f = 1 kHz, C_S = 0.05 μF
V_{CLAMP} = 800 V, L_A = 25 μH, L_G = 2 μH
V_{GR} = −15 V, TURN-OFF ENERGY = 7.8 mJ

Figure 4.46. Turn-Off Power versus Time

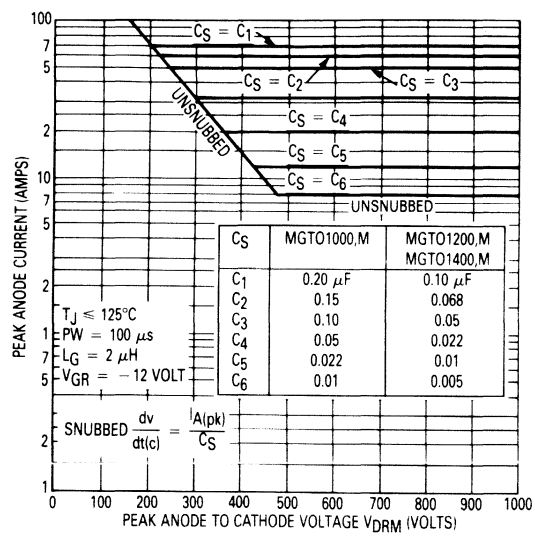
SWITCHING SAFE OPERATING AREA

Figure 4.47 describes the switching SOA capability of the GTO. The turn-off capability of the device is shown to be determined by the snubber size and dv/dt.

The unsnubbed operating limit has a voltage sensitive roll-off characteristic similar to the second breakdown derating shown on power transistor safe operating area (SOA) curves. Since the clamped unsnubbed inductive switching loadline is nearly square, it represents the instantaneous (V, I) handling capability of the device. The initial roll-off shown on the graph has a steeper slope than a constant power line. This is thought to be the result of the SOA capability of the GTO.

At higher voltages, unsnubbed operation allows much less peak anode current. However, the continuing drop in permitted maximum current takes place at a much slower rate.

The snubber limits the rate of anode voltage rise and changes the shape of the turn-off load line, causing the locus of instantaneous (Va, Ia) coordinates traversed by the GTO to pass through lower power values. Lower dv/dt(c) speeds turn off due to reduced Miller effect and provides additional time for the GTO to reduce its current before having to withstand high voltage. This brings the turn-off load line (V, I) locus of points below the instantaneous capability of the device.



C_S	MGTO1000,M	MGTO1200,M MGTO1400,M
C_1	0.20 μF	0.10 μF
C_2	0.15	0.068
C_3	0.10	0.05
C_4	0.05	0.022
C_5	0.022	0.01
C_6	0.01	0.005

NOTE: IN BRIDGE INVERTER CONFIGURATIONS THE UPPER AND LOWER SNUBBER CAPACITORS ARE IN PARALLEL PERMITTING A SNUBBER $\geq \frac{C_S}{2}$ WHEN STRAY INDUCTANCE IS KEPT LOW. UNSNUBBED OPERATION IS NOT RECOMMENDED ALTHOUGH HIGH CURRENTS AT LOW VOLTAGES CAN BE SWITCHED GIVEN WELL DEFINED LOAD CONDITIONS. THE USE OF A SMALL SNUBBER INSURES THAT THE WORST CASE dv/dt STRESS IS KNOWN.

Figure 4.47. Maximum Gate Controlled Interruptable Current (Rating is Non-Repetitive at I > 50 A)

Power and energy dissipation in the GTO tends to be greatest during the tail time because the anode voltage is highest then and because the decay of the tail current is relatively slow in comparison to the fall time.

The primary influences on the magnitude of tail current for a given set of gate drive parameters are temperature and dv/dt(c). Figure 4.48 shows how the anode current ramp is influenced by dv/dt(c). This current can be roughly modeled as the result of dv/dt across an equivalent capacitance. An abrupt failure will result if this current exceeds the SOA (V, I) capability of the GTO.

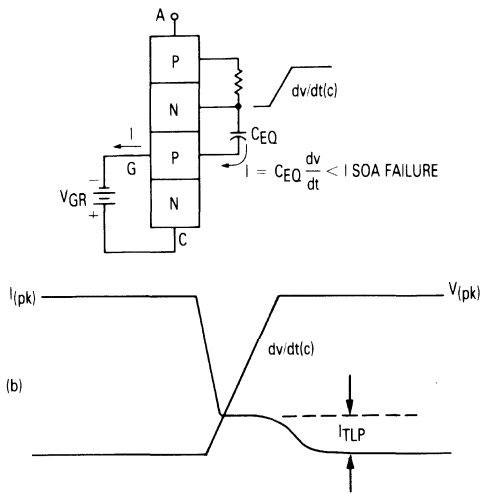


Figure 4.48. dv/dt(c), SOA Model Of GTO Failure

Like SCR devices, dv/dt effects in GTOs increase rapidly at junction temperatures at or above 125°C. The use of larger heat sinks to control the worst case T_J will provide significant increases in the switching safety margin.

It is desirable to minimize the snubber capacitance to improve circuit efficiency and allow higher switching speeds. The stored energy in the snubber capacitor is dissipated in the snubber resistor each cycle when RCD snubbers are used. This makes the snubber loss directly proportional to frequency. However, the snubber capacitor must be large enough to prevent turn-off failure under the worst case conditions.

A polarized snubber provides effective dv/dt limiting by providing an alternative path for the load current which is diverted into the snubber. Most of the stored energy in the load inductance is transferred to the snubber capacitor where its charging aids in limiting the kickback voltage. The snubber diode must be capable of conducting the peak anode current and blocking the peak voltage. The snubber resistor is used to limit the component of anode current supplied from the charged snubber capacitor at GTO turn-on during the next conduction cycle, and to prevent turn-on di/dt failure.

The snubber RC time constant must be selected to insure that the snubber capacitor fully discharges during the minimum GTO conduction time. Failure to achieve a low voltage initial condition will result in higher than anticipated anode voltages and dv/dt stress when the anode voltage abruptly flies up to the remaining capacitor voltage at turn-off time.

Measurement and application circuits using polarized snubbers and/or clamps should minimize the wiring inductance to these components to prevent overshoot in the anode voltage. These elements will be small enough to permit installation in close proximity to the GTO. The effects of parasitic inductance become more prominent at high current levels, requiring increased attention to management of current parasitics.

FAULT PROTECTION

The $I_{T(CSM)}$ rating is a measure of a GTO's ability to interrupt the current in a load under fault conditions. This allows overload protection of the GTO by means of its own gate turn-off capability.

Switched voltage source applications require the addition of a current slow down inductor to prevent excessive anode current rise before turn-off time. The ability of the GTO to self protect depends on its storage time and $I_{T(CSM)}$ capability as well as the speed of the fault detection and shut-down circuit. Storage time increases with the anode current and is roughly proportional to the square root of the peak current prior to turn-off.

Snubber design must consider fault conditions as well as normal repetitive operation. Turn-off cannot be attempted until the snubber circuit has been nearly discharged at least several time constants after the beginning of device turn-on. Failure to initialize the snubber capacitor will lead to high dv/dt stress and probable device failure if a fault-initiated shutdown takes place early in the conduction cycle.

Options for the protection of the GTO depend on the abruptness and severity of overload. Higher fault currents are allowable when device protection is accomplished by fusing techniques that rely on the device I^2t capability. Gate turn-off must not be attempted at currents above the $I_{T(CSM)}$ value if device destruction is to be avoided.

POWER DISSIPATION AND HEAT SINK DESIGN

The GTO is designed to operate at peak junction temperatures of 125°C or less. The management of maximum peak instantaneous junction temperature is particularly important at turn-off time because the stress on the device and the possibility of failure is greatest then. Conventional SCR phase control curves do not require forward blocking capability until the beginning of the next ac cycle and allow operation at instantaneous junction temperatures exceeding 125°C. The GTO may be required to turn off, withstand high dv/dt stress and forward block at any time in its conduction wave form. In addition, it may be operated at high frequencies where the power dissipation due to switching losses is a major component of the total average power. Actual GTO devices exhibit superior extreme high temperature blocking capability

and are capable of operation at higher temperatures than SCR units. However, the conditions of use will often place more stringent requirements on GTO devices. Consequently, a conservative approach to heat sink design and thermal control is advisable.

GTO phase control rating curves showing average current, power dissipation and allowable case temperature versus conduction angle, are similar to SCR curves. These curves describe operation from an ac line or chopping a dc source at variable duty cycle under low frequency conditions where switching power is negligible and the assumption of a current pulse with zero rise and fall time is valid. These curves do not adequately describe peak pulse device capability when inductive, capacitive or high-frequency switching is involved.

Figure 4.49 allows estimation of the heat sink requirement under pulsed and higher frequency conditions. The total power that must be dissipated in the heat sink is given by:

$$P_{total} = P_{t(on)} + P_{tf} + P_{tail} + P_{conduction} + P_{gate} + P_{leakage}$$

$$P_{off} = P_{tf} + P_{tail}$$

$$P_{(AV)} = \text{Energy per cycle/Time per cycle}$$

Wave shapes departing from those described may require multiplication and integration of the operating voltage and current waveforms in the actual application. Peak T_J can be estimated using the transient thermal response graph (Figure 4.49g) and the method for finding the temperature at the end of the N + 1 pulse in a rectangular pulse train. Non-rectangular pulses can be modeled as an equal energy rectangular pulse at the same peak power. This provides a worst case high junction temperature estimate. Refer to Motorola Application Note AN569 "Transient Thermal Resistance — General Data and Its Use" for more information.

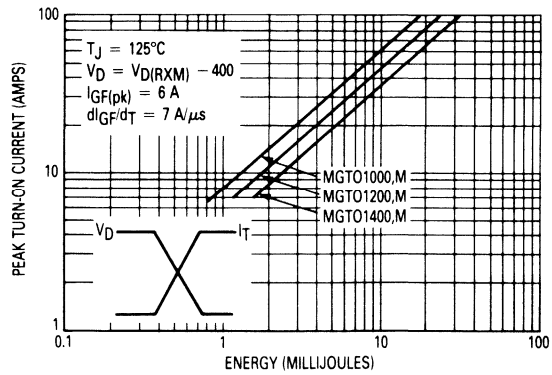


Figure 4.49(b). Maximum Energy Per Pulse at Turn-On

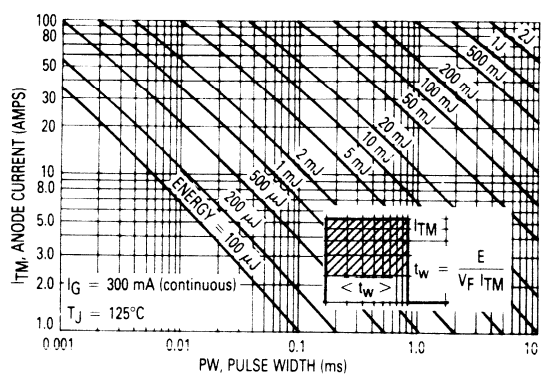


Figure 4.49(c). Conduction Energy Per Pulse

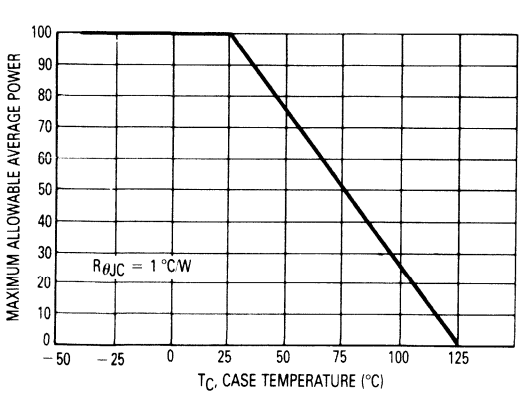


Figure 4.49(a). Average Power Derating

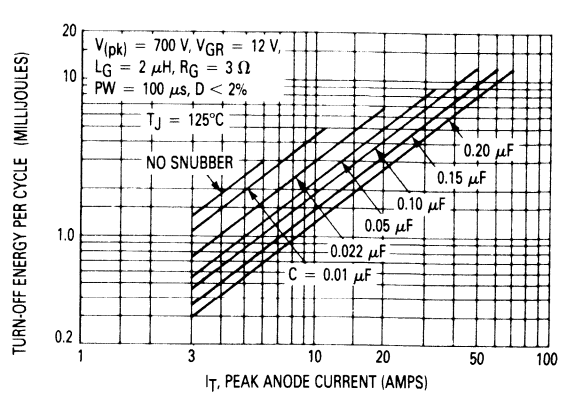


Figure 4.49(d). MGTO1000,M Turn-Off Energy (Inductive Load)

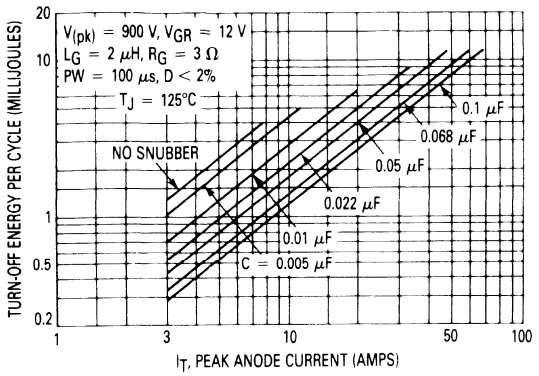


Figure 4.49(e). MGTO1200,M Turn-Off Energy (Inductive Load)

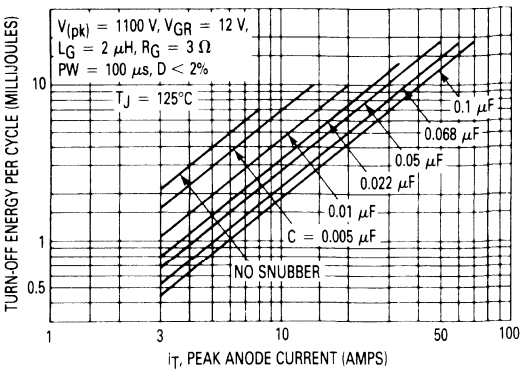


Figure 4.49(f). MGTO1400,M Turn-Off Energy (Inductive Load)

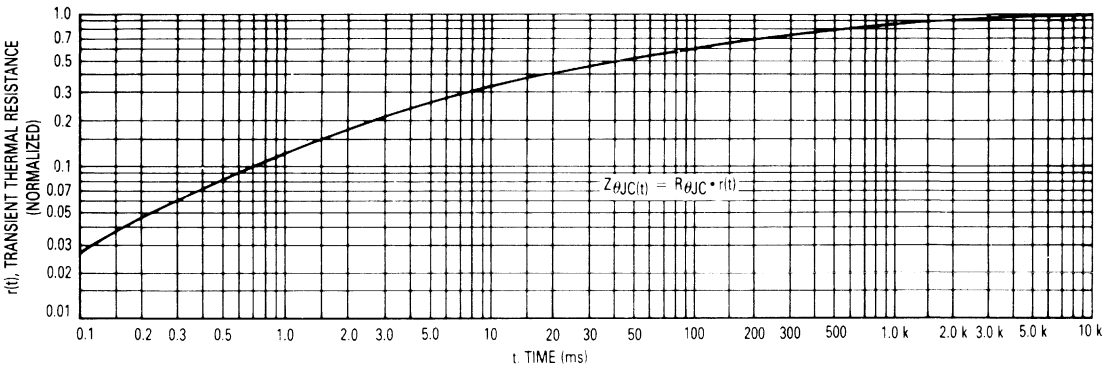


Figure 4.49(g). Thermal Response

POTENTIAL CIRCUIT APPLICATIONS FOR GTO DEVICES

Optimum GTO characteristics vary with the generic application and specific circumstances of usage. Consult the factory regarding your specific needs.

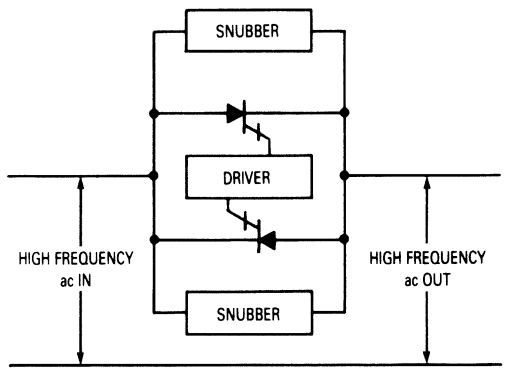


Figure 4.50. GTO dv/dt(c) Permits Solid State Switching At High Frequencies

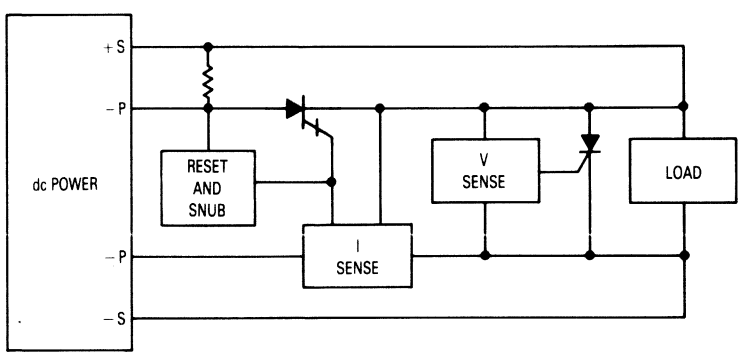


Figure 4.51. dc Circuit Breaker with OVP Crowbar

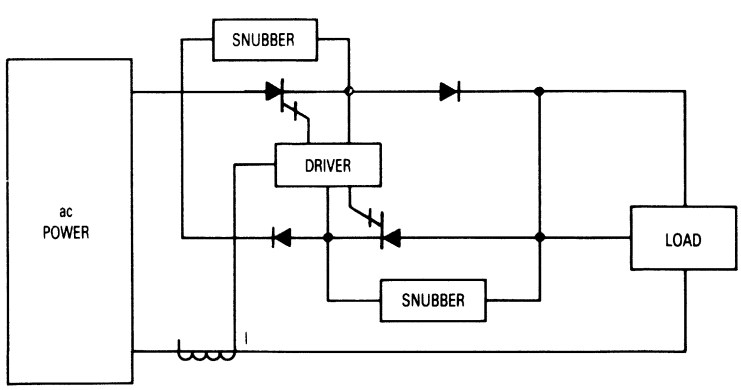


Figure 4.52. GTO ac Circuit Breaker

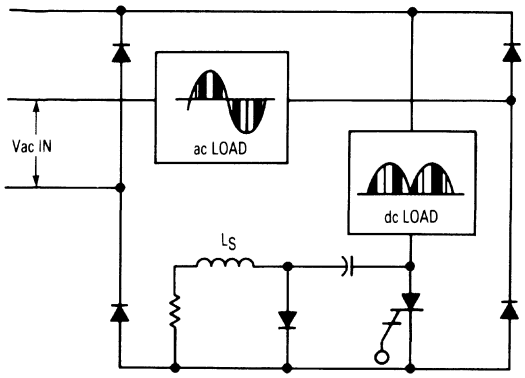


Figure 4.53. PWM Chopper for ac or dc Load, Snubber with di/dt Limiting Inductor

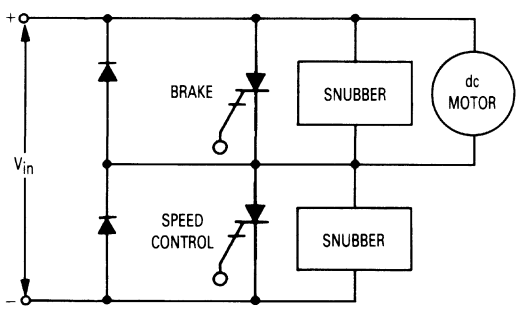


Figure 4.54. dc Motor Control

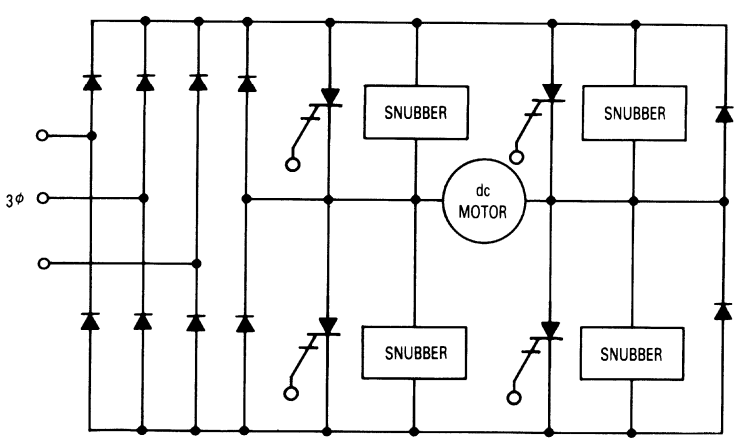


Figure 4.55. Variable Speed Reversible dc Motor Control

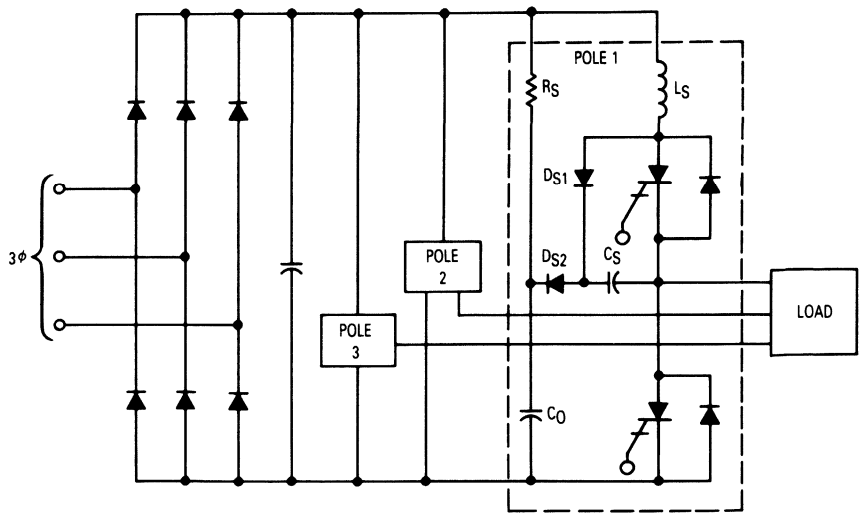


Figure 4.56. GTO Inverter for VVVF Induction Motor Control or CVCF Service with Turn-On/Off Snubber and Voltage Clamping

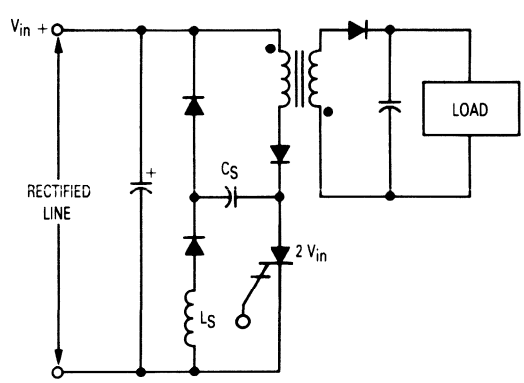


Figure 4.57. GTO Flyback Converter with Non-Dissipative L_C Snubber

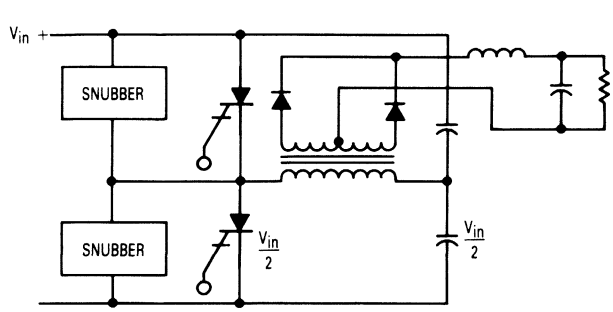


Figure 4.58. Half Bridge Converter

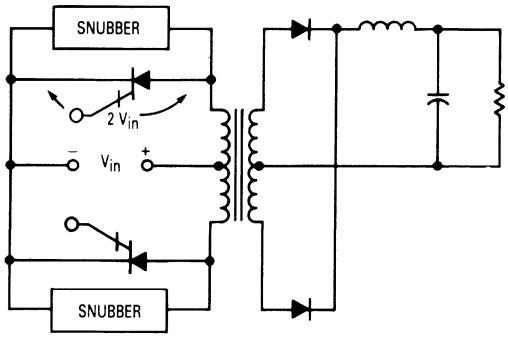


Figure 4.59. Push-Pull Converter

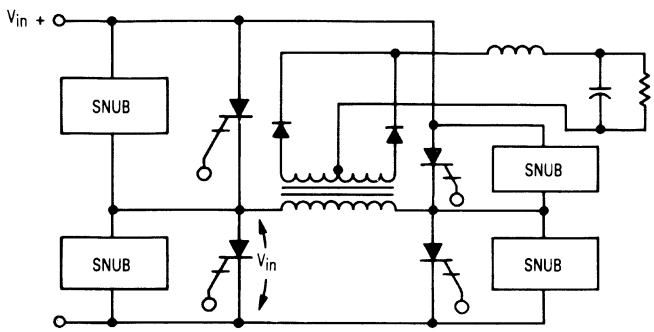


Figure 4.60. Full Bridge Converter

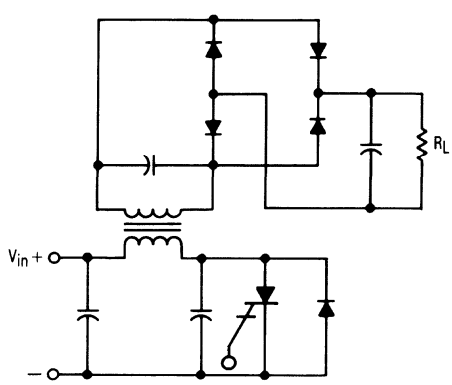


Figure 4.61. Series Resonant Power Supply Provides High Efficiency and Reduced RFI

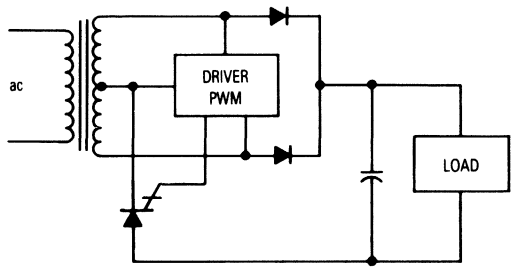


Figure 4.62. PWM Softstart for Capacitor Input Filter Reduces Rectifier Start-Up Stress and Line Surge

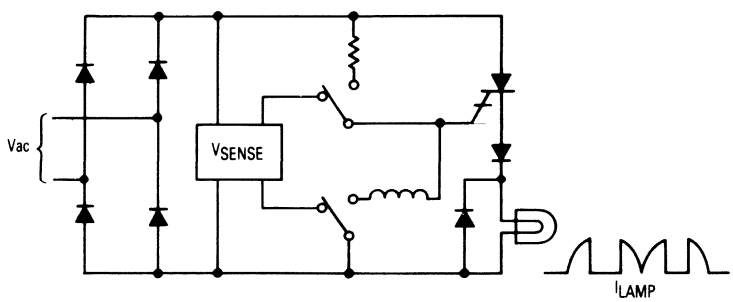


Figure 4.63. Double Edged Chopper Incandescent Lamp Dimmer Features Improved Line Regulation

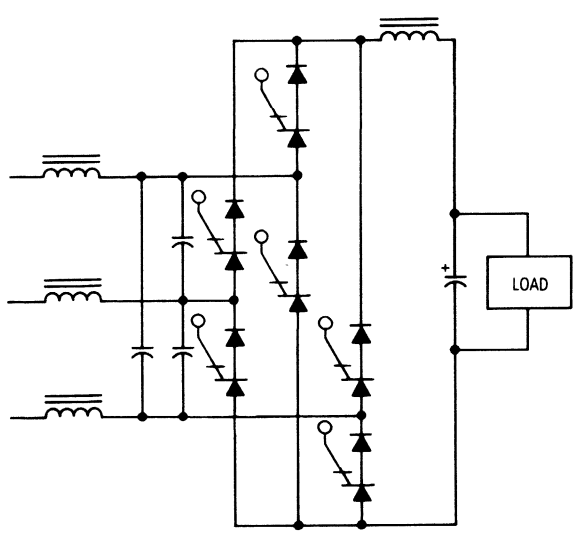


Figure 4.64. Three Phase PWM Rectifier Reduces Filter Size and Improves Input Power Factor

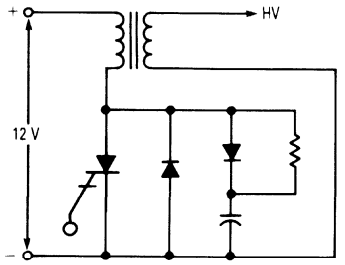


Figure 4.65. GTO Ignition System with Inductive Energy Storage

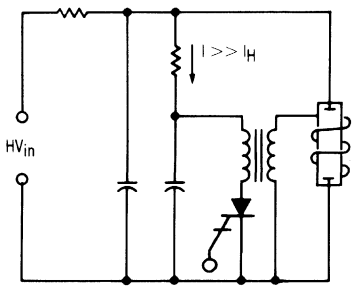


Figure 4.66. High Power, High Frequency Strobe Light

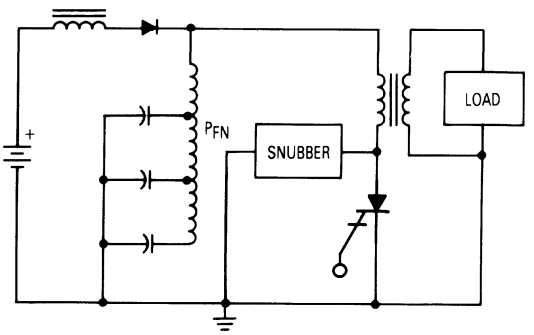


Figure 4.67. GTO Radar Modulator Provides High Operating Voltage, Repetition Frequency, and Turn-Off Confidence.

CHAPTER 5
SCR CHARACTERISTICS

1

SCR TURN-OFF CHARACTERISTICS

In addition to their traditional role of power control devices, SCRs are being used in a wide variety of other applications in which the SCR's turn-off characteristics are important. As an example — reliable high frequency inverters and converter designs (<20 kHz) require a known and controlled circuit-commutated turn-off time (t_q). Unfortunately, it is usually difficult to find the turn-off time of a particular SCR for a given set of circuit conditions.

This section discusses t_q in general and describes a circuit capable of measuring t_q. Moreover, it provides data and curves that illustrate the effect on t_q when other parameters are varied, to optimize circuit performance.

SCR TURN-OFF MECHANISM

The SCR, being a four layer device (P-N-P-N), is represented by the two interconnected transistors, as shown in Figure 5.1. This regenerative configuration allows the device to turn on and remain on when the gate trigger is removed, as long as the loop gain criteria is satisfied; i.e., when the sum of the common base current gains (α) of both the equivalent NPN transistor and PNP transistor, exceed one. To turn off the SCR, the loop gain must be brought below unity, whereby the on-state principal current (anode current i_T) limited by the external circuit impedance, is reduced below the holding current (I_H). For ac line applications, this occurs automatically during the negative going portion of the waveform. However, for dc applications (inverters, as an example), the anode current must be interrupted or diverted; (diversion of the anode current is the technique used in the t_q test fixture described later in this application note).

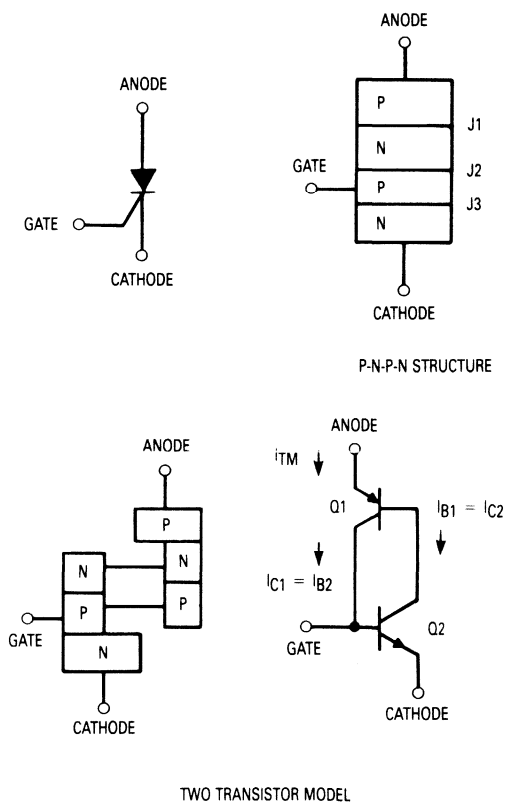


Figure 5.1. Two Transistor Analogy of an SCR

SCR TURN-OFF TIME t_q

Once the anode current in the SCR ceases, a period of time must elapse before the SCR can again block a forward voltage. This period is the SCR's turn-off time, t_q, and is dependent on temperature, forward current, and other parameters. The turn-off time phenomenon can be understood by considering the three junctions that make up the SCR. When the SCR is in the conducting state, each of the three junctions is forward biased and the N and P regions (base regions) on either side of J2 are heavily saturated with holes and electrons (stored charge). In order to turn off the SCR in a minimum amount of time, it is necessary to apply a negative (reverse) voltage to the device anode, causing the holes and electrons near the two end junctions, J1 and J3, to diffuse to these junctions. This causes a reverse current to flow through the SCR. When the holes and electrons near junc-

tions J1 and J3 have been removed, the reverse current will cease and junctions J1 and J3 will assume a blocking state. However, this does not complete the recovery of the SCR since a high concentration of holes and electrons still exist near the center junction, J2. This concentration decreases by the recombination process and is largely independent of the external circuit. When the hole and electron concentration near junction J2 has reached some low value, junction J2 will assume its blocking condition and a forward voltage can, after this time, be applied without the SCR switching back to the conduction state.

1

t_q MEASUREMENT

When measuring SCR turn-off time, t_q, it is first necessary to establish a forward current for a period of time long enough to ensure carrier equilibrium. This must be specified, since I_{TM} has a strong effect on the turn-off time of the device. Then, the SCR current is reversed at a specified di/dt rate, usually by shunting the SCR anode to some negative voltage through an inductor. The SCR will then display a "reverse recovery current," which is the charge clearing away from the junctions. A further waiting time must then elapse while charges recombine, before a forward voltage can be applied. This forward voltage is ramped up a specified dv/dt rate. The dv/dt delay time is reduced until a critical point is reached where the SCR can no longer block the forward applied voltage ramp. In effect, the SCR turns on and consequently, the ramp voltage collapses. The elapsed time between this critical point and the point at which the forward SCR current passes through zero and starts to go negative (reverse recovery phase), is the t_q of the SCR. This is illustrated by the waveforms shown in Figure 5.2.

t_q GENERAL TEST FIXTURE

The simplified circuit for generating these waveforms is schematically illustrated in Figure 5.3. This circuit is implemented with as many as eight transformers including variacs, and in addition to being very bulky, has been known to be troublesome to operate. However, the configuration is relevent and, in fact, is the basis for the design, as described in the following paragraphs.

t_q TEST FIXTURE BLOCK DIAGRAMS AND WAVEFORMS

The block diagram of the t_q Test Fixture, illustrated in Figure 5.4, consists of four basic blocks: A Line Synchronized Pulse Generator establishes system timing; a Constant Current Generator (variable in amplitude) powers the Device Under Test (DUT); a di/dt Circuit controls the rate of change of the SCR turn-off current; and the dv/dt Circuit reapplies a controlled forward blocking voltage. Note from the waveforms illustrated that the di/dt circuit, in parallel with the DUT, diverts the constant current from the DUT to produce the described anode current I_{TM}.

t_q TEST FIXTURE CHARACTERISTICS

The complete schematic of the t_q Test Fixture and the important waveforms are shown in Figures 5.5 and 5.6, respectively.

One CMOS Hex Gate U1, Motorola type MC14572, is used as the Line Synchronized Pulse Generator, configured as a wave shaping Schmitt trigger, clocking two cascaded monostable multivibrators for delay and pulse width settings (Gates 1C to 1F). The result is a pulse generated every half cycle whose width and position

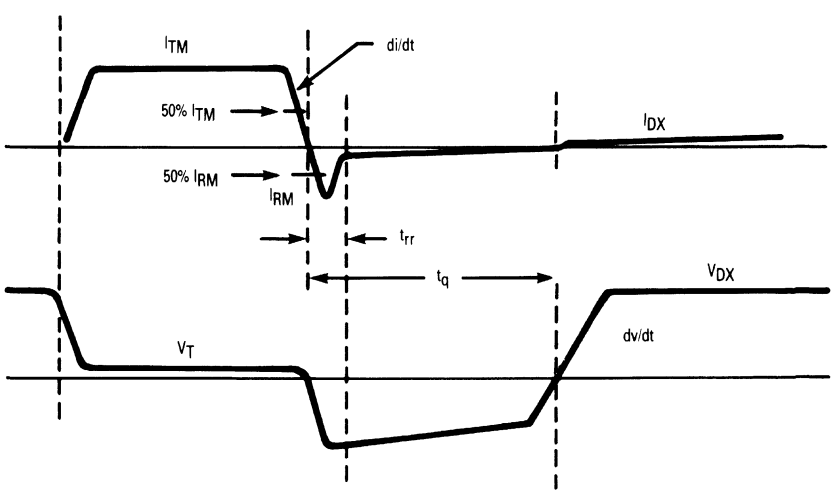


Figure 5.2. SCR Current and Voltage Waveforms During Circuit-Commutated Turn-Off

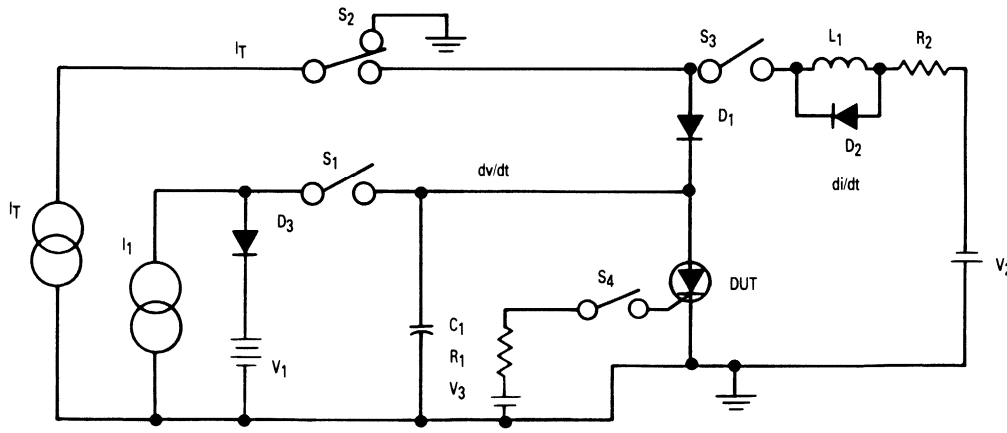


Figure 5.3. Simplified t_q Test Circuit

(where on the cycle it triggers) are adjustable by means of potentiometers R2 and R3, respectively. The output pulse is normally set to straddle the peak of the ac line, which not only makes the power supplies more efficient, but also allows a more consistent oscilloscope display. This pulse shown in waveform A of Figure 5.6 initiates the t_q test, which requires approximately 0.5 ms to assure the device a complete turn on. A fairly low duty cycle results, (approximately 5%) which is important in minimizing temperature effects. The repetitive nature of this test permits easy oscilloscope viewing and allows one to readily "walk in" the dv/dt ramp. This is accomplished by adjusting the appropriate potentiometer (R7) which, every 8.33 ms (every half cycle) will apply the dv/dt ramp at a controlled time delay.

To generate the appropriate system timing delays, four RC integrating network/comparators are used, consisting of op-amps U2, U5 and U6.

Op-amp U2A, along with transistor Q2, opto-coupler U4 and the following transistors Q6 and Q7, provide the gate drive pulse to the DUT (see waveforms B, C and D of Figure 5.6). The resulting gate current pulse is about 50 μs wide and can be selected, by means of switch S2, for an I_{GT} of from about 1 mA to 90 mA. Opto-coupler U4, as well as U1 in the Constant Current Circuit, provide electrical isolation between the power circuitry and the low level circuitry.

The Constant Current Circuit consists of an NPN Darlington Q3, connected as a constant current source driving a PNP tri-Darlington (Darlington Q4, Bipolar Q5). By varying the base voltage of Q3 (with Current Control potentiometer R4), the collector current of Q3 and thus the base voltage of Q4 will also vary. The PNP output transistor Q5 (MJ14003) (rated at 70 A), is also configured as a constant current source with four, parallel connected emitter resistors (approximately 0.04 ohms, 200 W), thus providing as much as 60 A test current. Very briefly, the circuit operates as follows: — CMOS Gate 1E is clocked high, turning on, in order, a) NPN transistor Q16, b) PNP transistor Q1, c) optocoupler U3, and d) transistors Q3, Q4 and Q5. The board mounted Current Set potentiometer R5, sets the maximum output current and R4, the Current Control, is a front panel, multiturn potentiometer.

Time delay for the di/dt Circuit is derived from cascaded op-amps U2B and U5 (waveforms F and G of Figure 5.6). The output gate, in turn, drives NPN transistor Q8, fol-

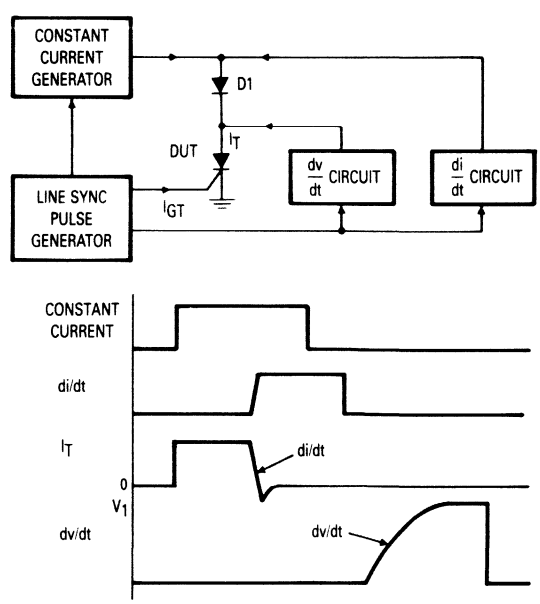
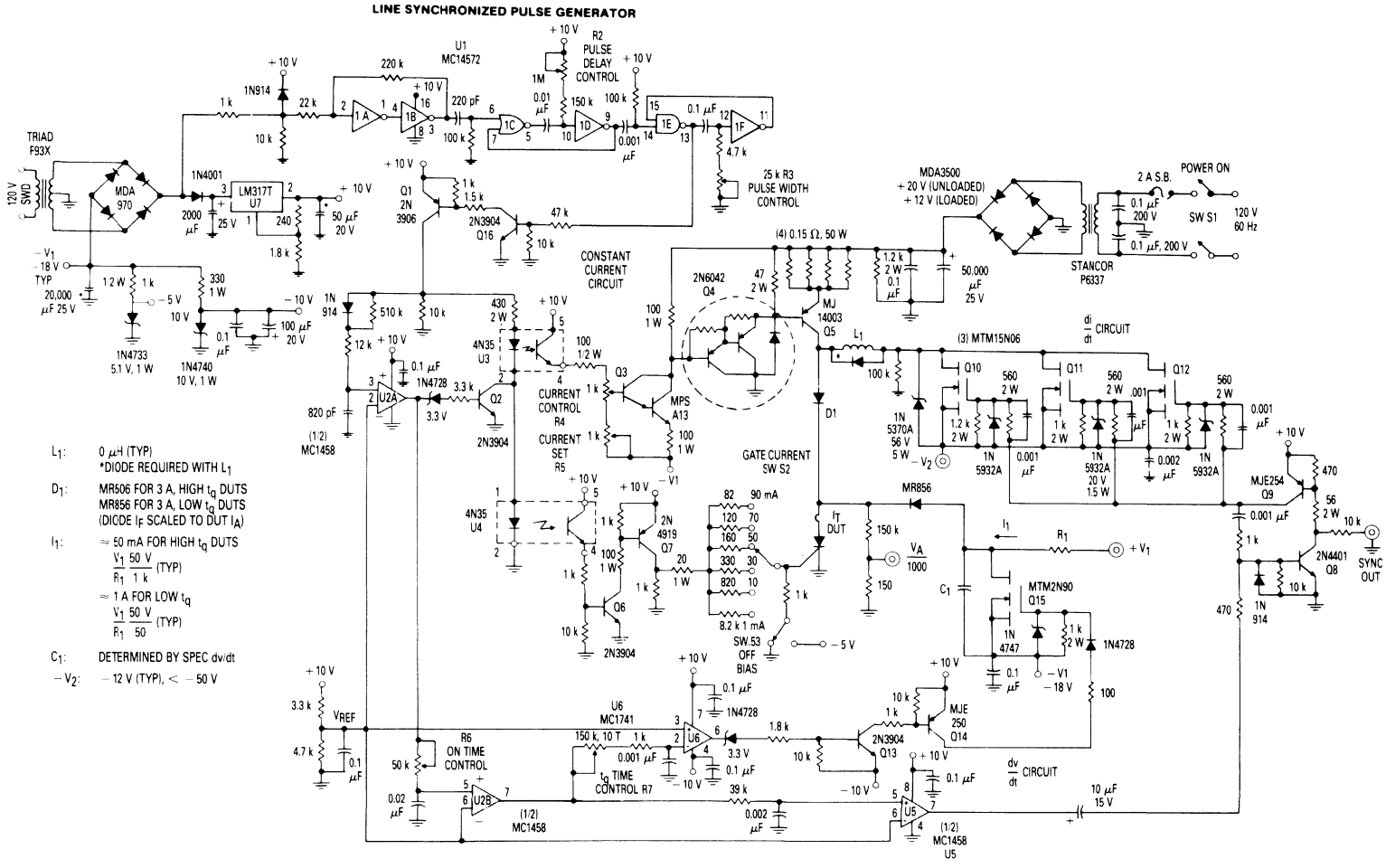


Figure 5.4. Block Diagram of the t_q Test Fixture and Waveforms



L_1: 0 μH (TYP)
*DIODE REQUIRED WITH L_1

D_1: MR506 FOR 3 A, HIGH t_q DUTS
MR856 FOR 3 A, LOW t_q DUTS
(DIODE I_F SCALED TO DUT I_A)

I_1: ≈ 50 mA FOR HIGH t_q DUTS
$\frac{V_1}{R_1} \frac{50\ V}{1\ k}$ (TYP)
≈ 1 A FOR LOW t_q
$\frac{V_1}{R_1} \frac{50\ V}{50}$ (TYP)

C_1: DETERMINED BY SPEC dv/dt

$-V_2$: − 12 V (TYP), < − 50 V

Figure 5.5. t_q Test Fixture

lowed by PNP transistor Q9, whose output provides the gate drive for the three parallel connected N-channel power MOSFET transistors Q10–Q12 (waveform H of Figure 5.6). These three FETs (MTM15N06), are rated at 15 A continuous drain current and 40 A pulsed current and thus can readily divert the maximum 60 A constant current that the Fixture can generate. The results of this diversion from the DUT is described by waveforms E, H and I of Figure 5.6, with the di/dt of I_{TM} dictated by the series inductance L1. For all subsequent testing, the inductor was a shorting bar, resulting in very little inductance and consequently, the highest di/dt (limited primarily by wiring inductance). When a physical inductor L1 is used, a clamp diode, scaled to the diverted current, should be placed across L1 to limit "inductive kicks."

dv/dt CIRCUIT

The last major portion of the Fixture, the dv/dt Circuit, is variable time delayed by the multi-turn, front panel t_q Time Control potentiometer R7, operating as part of an integrator on the input of comparator U6. Its output (waveform J of Figure 5.6) is used to turn-off, in order, a) normally on NPN transistor Q13, b) PNP transistor Q14 and c) N-channel power MOSFET Q15 (waveform L of Figure 5.6). This FET is placed across ramp generating capacitor C1, and when unclamped (turned off), the capacitor is allowed to charge through resistor R1 to the supply voltage $+V_1$. Thus, the voltage appearing on the drain will be an exponentially rising voltage with a dv/dt dictated by R1, C1, whose position in time can be advanced or delayed. This waveform is then applied through a blocking diode to the anode of the DUT for the forward blocking voltage test.

Another blocking diode, D1, also plays an important role in t_q measurements and must be properly selected. Its purpose is to prevent the dv/dt ramp from feeding back into the Current Source and di/dt Circuit and also to momentarily apply a reverse blocking voltage (a function of $-V_2$ of the di/dt circuit) to the DUT. Consequently, D1 must have a reverse recovery time t_{rr} greater than the DUT, but less than the t_q time. When measuring standard recovery SCRs, its selection — fast recovery rectifiers or standard recovery — is not that critical, however, for fast recovery, low t_q SCRs, the diode must be tailored to the DUT to produce accurate results. Also, the current rating of the diode must be compatible with the DUT test current. These effects are illustrated in the waveforms shown in Figure 5.7 where both a fast recovery rectifier and standard recovery rectifier were used in measuring t_q of a standard 2N6058 SCR. Although the di/dt's were the same, the reverse recovery current I_{RM} and t_{rr} were greater with the standard recovery rectifier, resulting in a somewhat shorter t_q (59 μs versus 63 μs). In fact, t_q is affected by the initial conditions (I_{TM}, di/dt, I_{RM}, dv/dt, etc.) and these conditions should be specified to maintain measurement repeatability. This is later described in the published curves and tables.

Finally, the resistor R1 and the resultant current I_1 in the dv/dt circuit must meet certain criteria: I_1 should be greater than the SCR holding current so that when the DUT does indicate t_q limitation, it latches up, thus suppressing the dv/dt ramp voltage; and, for fast SCRs (low t_q), I_1 should be large enough to ensure measurement repeatability. Typical values of I_1 for standard and fast SCRs may be 50 mA and 500 mA, respectively. Obviously, for high forward blocking voltage $+V_1$ tests, the power requirements must be met.

EFFECTS OF GATE BIAS ON t_q

Examples of the effects of I_1 on t_q are listed in Table 5.III whereby standard and fast SCRs were tested with about 50 mA and 1 A, respectively. Note that the low t_q SCR's required fast recovery diodes and high I_1 current.

TEST FIXTURE POWER SUPPLIES

Most of the power supplies for the system are self-contained, including the +12 V supply for the Constant Current Circuit. This simple, unregulated supply furnishes up to 60 A peak pulsed current, primarily due to the line synchronized operation of the system. Power supplies $+V_1$ and $-V_2$, for this exercise, were external supplies, since they are variable, but they can be incorporated in the system. The reverse blocking voltage to the DUT is supplied by $-V_2$ and is typically set for about

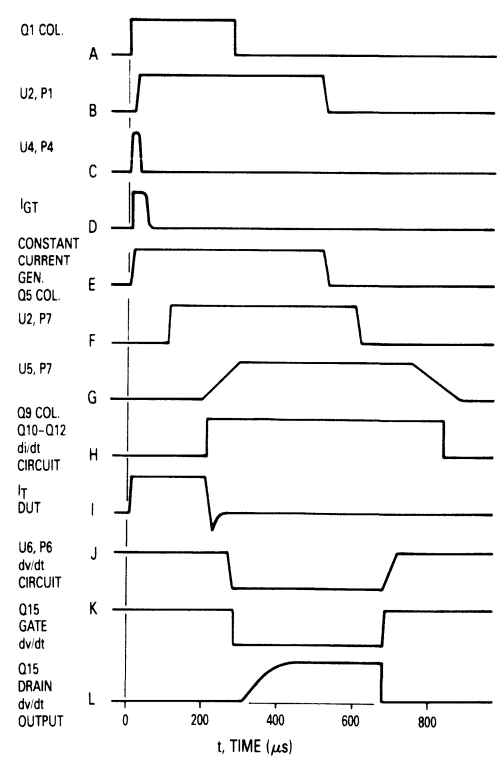
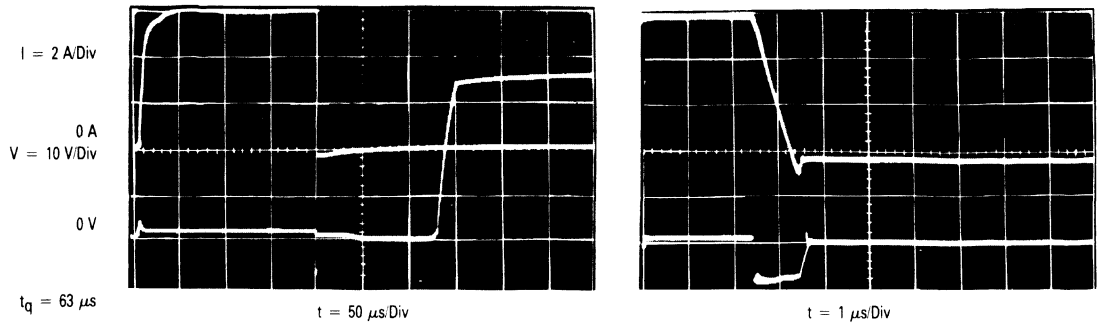
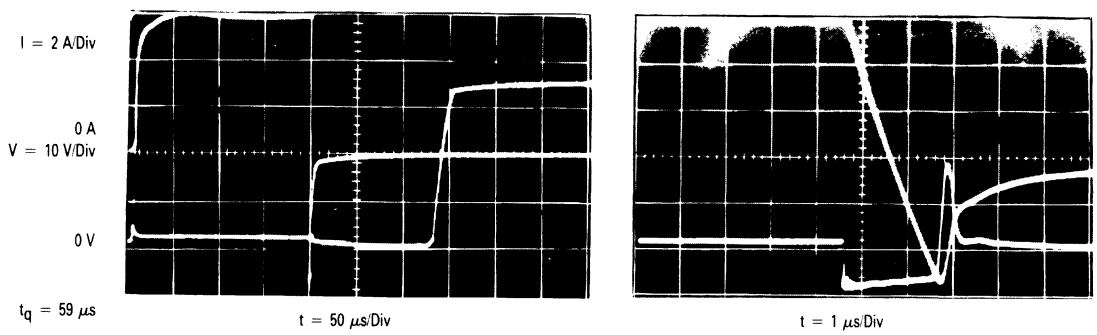


Figure 5.6. t_q Test Fixture System Waveforms



D1 = MR856, FAST RECOVERY RECTIFIER



D1 = MR502, STANDARD RECOVERY RECTIFIER

Figure 5.7. The Effects of Blocking Diode D1 on t_q of a 2N6058 SCR

−10 V to −20 V, being limited to the breakdown voltage of the diverting power MOSFETS (V_{DSS} = 60 V). The +12 V unregulated supply can be as high as +20 V when unloaded; therefore, $-V_2$ (MAX), in theory, would be −40 V but should be limited to less than −36 V due to the 56 V protective Zener across the drain-source of the FETs. Also, $-V_2$ must be capable of handling the peak 60 A, diverting current, if so required.

The reapplied forward blocking voltage power supply $+V_1$, may be as high as the DUT V_{DRM} which conceivably can be 600 V, 1,000 V or greater and, since this supply is on most of the time, must be able to supply the required I_1. Due to the sometimes high power requirements, $+V_1$ test conditions may have to be reduced for extremely fast SCRs.

PARAMETERS AFFECTING t_q

To see how the various circuit parameters can affect t_q, one condition at a time is varied while the others are held constant. The parameters to be investigated are a) forward current magnitude (I_{TM}), b) forward current duration, c) rate of change of turn-off current (di/dt), d) reverse-current magnitude (I_{RM}), e) reverse voltage (V_{RM}), f) rate of reapplied forward voltage (dv/dt), g) magnitude limit of reapplied voltage, h) gate-cathode resistance and i) gate drive magnitude (I_{GT}).

Typical data of this kind, taken for a variety of SCRs, including standard SCRs, high speed SCRs, and the new TMOS SCRs (Motorola MCR1000 series), is condensed and shown in Table 5.I. The data consists of the different conditions which the particular SCR types were subjected to; ten SCRs of each type were serailized and tested to each condition and the ten t_q's were averaged to yield a "typical t_q."

The conditions listed in Column A in Table 5.I, are typical conditions that might be found in circuit operation. Columns B through J in Table 5.I, are in order of increasing t_q; the conditions listed in these columns are only the conditions that were modified from those in Column A and if a parameter is not listed, it is the same as in Column A.

Table 5.II is a condensed summary of Table 5.I and

Table 5.I. Parameters Affecting t_q

Device	A	B	C	D	E	F	G	H	I
2N6508 25 A 600 V	R_{GK} = 1 k dv/dt = 15 V/µs I_{TM} = 25 A I_{RM} = 14 A di/dt = −100 A/µs I_{TM} duration = 275 µs I_{GT} = 30 mA	R_{GK} = 100 dv/dt = 2.4 V/µs I_{TM} = 1 A I_{RM} = 1.8 A di/dt = 32 A/µs	R_{GK} = 100 dv/dt = 2.4 V/µs I_{TM} = 2 A I_{RM} = 50 mA di/dt = 0.5 µs	R_{GK} = 100 dv/dt = 2.4 V/µs I_{RM} = 50 mA di/dt = 0.45 A/µs	R_{GK} = 100 dv/dt = 2.4 V/µs	R_{GK} = ∞ dv/dt = 2.4 V/µs	R_{GK} = 100 dv/dt = 2.4 V/µs I_{TM} = 37 A	R_{GK} = 100	I_{GT} = 90 mA
	typ t_q = 68 µs	typ t_q = 42 µs	typ t_q = 45 µs	typ t_q = 49 µs	typ t_q = 60 µs	typ t_q = 64 µs	typ t_q = 64 µs	typ t_q = 65 µs	typ t_q = 68 µs
MCR2150 15 A	R_{GK} = 1 k dv/dt = 125 V/µs I_{TM} = 15 A I_{RM} = 5.5 A di/dt = 36 A/µs I_{TM} duration = 275 µs I_{GT} = 50 mA	R_{GK} = 100 I_{RM} = 0.2 A di/dt = 0.64 A/µs I_{GT} = 90 mA	R_{GK} = 100 I_{TM} = 2 A I_{RM} = 2.4 A di/dt = −40 A/µs I_{GT} = 90 mA	R_{GK} = 100 I_{GT} = 90 mA	R_{GK} = ∞ I_{GT} = 90 mA	I_{GT} = 90 mA	R_{GK} = 100 dv/dt = 7 V/µs I_{GT} = 90 mA	R_{GK} = 100 I_{TM} = 23 A I_{RM} = 8 A di/dt = 32 A/µs I_{GT} = 90 mA	
	typ t_q = 3.15 µs	typ t_q = 0.975 µs	typ t_q = 2.3 µs	typ t_q = 3.1 µs	typ t_q = 3.13 µs	typ t_q = 3.13 µs	typ t_q = 3.3 µs	typ t_q = 3.8 µs	
2N6398 12 A	R_{GK} = 1 k dv/dt = 90 V/µs I_{TM} = 12 A I_{RM} = 11 A di/dt = −100 A/µs I_{TM} duration = 275 µs I_{GT} = 30 mA	R_{GK} = 100 dv/dt = 2.5 V/µs I_{TM} = 1 A I_{RM} = 50 mA di/dt = −0.5 A/µs	R_{GK} = 100 dv/dt = 2.5 V/µs I_{TM} = 1 A I_{RM} = 2.7 A di/dt = 56 A/µs	R_{GK} = 100 dv/dt = 2.5 V/µs I_{RM} = 50 mA di/dt = 32 A/µs	R_{GK} = 100 dv/dt = 2.5 V/µs I_{TM} = 18 A I_{RM} = 50 mA di/dt = 0.3 A/µs	R_{GK} = ∞ dv/dt = 2.5 V/µs I_{RM} = 50 mA di/dt = 0.35 A/µs	R_{GK} = 100	I_{GT} = 90 mA	
	typ t_q = 48 µs	typ t_q = 30 µs	typ t_q = 31 µs	typ t_q = 32 µs	typ t_q = 33 µs	typ t_q = 35.5 µs	typ t_q = 45 µs	typ t_q = 48 µs	
MCR2080 8 A	R_{GK} = 1 k dv/dt = 110 V/µs I_{TM} = 8 A I_{RM} = 5 A di/dt = −50 A/µs I_{TM} duration = 275 µs I_{GT} = 50 mA	R_{GK} = 100 I_{TM} = 1 A I_{RM} = 50 mA di/dt = −0.7 A/µs	R_{GK} = 100 I_{TM} = 12 A I_{RM} = 0.1 A di/dt = −0.7 A/µs	R_{GK} = ∞ I_{RM} = 0.1 A di/dt = −0.7 A/µs	R_{GK} = 100 I_{TM} = 1 A I_{RM} = 2.8 A di/dt = −60 A/µs	R_{GK} = 100 I_{RM} = 1 A di/dt = −0.7 A/µs	I_{GT} = 90 mA	R_{GK} = 100	R_{GK} = 100 dv/dt = 3.6 V/µs
	typ t_q = 4.7 µs	typ t_q = 2.3 µs	typ t_q = 2.4 µs	typ t_q = 3.2 µs	typ t_q = 3.2 µs	typ t_q = 3.3 µs	typ t_q = 4.7 µs	typ t_q = 4.8 µs	typ t_q = 4.9 µs

Table 5.I. Continued

Device	A	B	C	D	E	F	G	H	I	J
C1060 4 A	I_{GT} = 1 mA R_{GK} = 1 k dv/dt = 5 V/μs I_{TM} = 4 A I_{RM} = 4 A di/dt = 50 A/μs I_{TM} duration = 275 μs V_{DX} = 50 V	I_{TM} = 2 A I_{RM} = 2.5 A di/dt = −30 A/μs V_{DX} = 50 V	I_{TM} = 6 A I_{RM} = −1 A/μs di/dt = −1 A/μs V_{DX} = 150 V	I_{TM} = 6 A I_{RM} = 0.1 A di/dt = −1 A/μs V_{DX} = 50 V	dv/dt = 1.4 V/μs I_{TM} = 2 A I_{RM} = 0.2 A di/dt = −1.4 A/μs	$-V_2$ = 35 V I_{RM} = 0.2 A di/dt = −1.4 A/μs	I_{RM} = 0.15 A $-V_2$ = 4 V di/dt = −1.4 A/μs	dv/dt = 1.4 V/μs I_{RM} = 0.15 A di/dt = 1.4 A/μs	I_{GT} = 90 mA dv/dt = 1.4 V/μs I_{RM} = 2 A di/dt = −1.4 A/μs	dv/dt = 28 V/μs I_{RM} = 0.15 A di/dt = −1.4 A
	typ t_q = 28 μs	typ t_q = 25 μs	typ t_q = 26 μs	typ t_q = 26 μs	typ t_q = 26 μs	typ t_q = 27 μs	typ t_q = 27 μs	typ t_q = 27 μs	typ t_q = 27 μs	typ t_q = 29 μs
2N6240 4 A	R_{GK} = 1 k dv/dt = 40 V/μs I_{TM} = 4 A I_{RM} = 4 A di/dt = 50 A/μs I_{TM} duration = 275 μs I_{GT} = 1 mA V_{DX} = 50 V	R_{GK} = 100 dv/dt = 1.3 V/μs I_{TM} = 1 A I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA V_{DX} = 150 V	R_{GK} = 100 dv/dt = 1.75 V/μs I_{TM} = 1 A I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA	R_{GK} = 100 dv/dt = 1.75 V/μs I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA	dv/dt = 1.75 V/μs R_{GK} = 100 I_{TM} = 6 A I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA	R_{GK} = 100 I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA	R_{GK} = 100 I_{GT} = 900 mA	R_{GK} = ∞ dv/dt = 1.75 V μs I_{TM} = 1 A I_{RM} = 50 mA di/dt = −0.5 A/μs I_{GT} = 90 mA	I_{GT} = 90 mA	
	typ t_q = 44.8 μs	typ t_q = 26 μs	typ t_q = 26.2 μs	typ t_q = 27.7 μs	typ t_q = 28.6 μs	typ t_q = 30 μs	typ t_q = 32.7 μs	typ t_q = 37.2 μs	typ t_q = 41.4 μs	
MCR100-6 8 A	R_{GK} = 1 k dv/dt = 160 V/μs I_{TM} = 0.8 A I_{RM} = 0.8 A di/dt = 12 A/μs V_{DX} = 50 V I_{TM} duration = 275 μs	dv/dt = 30 V/μs I_{TM} = 0.25 A I_{RM} = 40 mA di/dt = −0.6 A/μs	dv/dt = 30 V/μs Ir = 40 mA di/dt = −0.8 A/μs	$-V_2$ = 9 V I_{RM} = 20 mA di/dt = −0.4 A/μs	$-V_2$ = 1 V Ir = 40 mA di/dt = −0.8 A/μs	dv/dt = 30 V/μs I_{TM} = 1.12 A I_{RM} = 40 mA di/dt = −0.8 A/μs	dv/dt = 30 V/μs I_{TM} = 1.12 A I_{RM} = 40 mA di/dt = −0.8 A/μs V_{DX} = 100 V			
	typ t_q = 14.4 μs	typ t_q = 12.7 μs	typ t_q = 13.5 μs	typ t_q = 13.7 μs	typ t_q = 13.9 μs	typ t_q = 14.4 μs	typ t_q = 14.4 μs			
2N5063 8 A	R_{GK} = 1 k dv/dt = 30 V/μs I_{TM} = 0.8 A I_{RM} = 0.8 A di/dt = 12 A/μs I_{TM} duration = 275 μs V_{DX} = 50 V	dv/dt = 5 V/μs I_{TM} = 0.2 A I_{RM} = 50 mA di/dt = −0.6 A/μs	dv/dt = 5 V/μs I_{RM} = 50 mA di/dt = −0.8 A/μs	dv/dt = 5 V/μs I_{TM} = 1.12 A I_{RM} = 50 mA di/dt = −0.8 A/μs	I_{RM} = 40 mA $-V_2$ = 9 V di/dt = −0.45 A/μs	I_{RM} = 40 mA $-V_2$ = 1 V di/dt = −0.8 A/μs	V_{DX} = 100 V dv/dt = 5 V/μs I_{TM} = 1.12 A I_{RM} = 50 mA di/dt = −0.8 A			
	typ t_q = 28.9 μs	typ t_q = 27/μs	typ t_q = 30/μs	typ t_q = 31 μs	typ t_q = 31.2 μs	typ t_q = 31.4 μs	typ t_q = 31.7 μs			
2N5061 8 A	dv/dt = 10 V/μs I_{TM} = 0.8 A I_{RM} = 0.8 A di/dt = 18 A/μs I_{TM} duration = 275 μs R_{GK} = 1 k V_{DX} = 30 V	dv/dt = 3.5 V/μs I_{TM} = 0.25 A I_{RM} = 40 mA di/dt = −0.7 A/μs	dv/dt = −3.5 V/μs I_{RM} = 40 mA di/dt = −0.8 A/μs	dv/dt = 3.5 V/μs I_{TM} = 1.12 A I_{RM} = 40 mA di/dt = −0.8 A/μs V_{DX} = 60 V	dv/dt = 3.58/μs I_{TM} = 1.12 A I_{RM} = 40 mA di/dt = −0.7 A/μs	$-V_2$ = 4 V I_{RM} = 20 mA di/dt = −0.2 A/μs	$-V_2$ = 1 V I_{RM} = 40 mA di/dt = −0.8 A/μs			
	typ t_q = 31.7 μs	typ t_q = 19.1 μs	typ t_q = 19/μs	typ t_q = 19.8 μs	typ t_q = 20.2 μs	typ t_q = 30 μs	typ t_q = 30.2 μs			

shows what happens to the t_q of the different devices when a parameter is varied in one direction or the other. There are also several curves (Figures 5.8, 5.9 and 5.10) which indicate what happens to t_q when other influential parameters are varied.

THE EFFECTS OF CHANGING PARAMETERS ON t_q

From Tables 5.I and 5.II, it is clear that some parameters affect t_q more than others. The following discussion describes the effect on t_q of the various parameters.

FORWARD CURRENT MAGNITUDE (I_{TM})

Of the parameters that were investigated, forward-current magnitude and the di/dt rate have the strongest effect on t_q. Varying the I_{TM} magnitude over a realistic range of I_{TM} conditions can change the measured t_q by about 30%. The change in t_q is attributed to varying current densities (stored charge) present in the SCR's junctions as the I_{TM} magnitude is changed. Thus, if a large SCR must have a short t_q when a low I_{TM} is present, a large gate trigger pulse (I_{GT} magnitude) would be advantageous. This turns on a large portion of the SCR to minimize the high current densities that exists if only a small portion of the SCR were turned on (by a weak gate pulse) and the low I_{TM} did not fully extend the turned on region.

In general, the SCR will exhibit longer t_q times with increasing I_{TM}, as shown in the curves of Figures 5.8 and 5.9. Increasing temperature also increases the t_q time (Figure 5.9).

di/dt RATE

Varying the turn-off rate of change of anode current di/dt does have some effect on the t_q of SCRs, as shown in Figure 5.10. Although the increase in t_q versus increasing di/dt was nominal for the SCRs illustrated, the percentage change for the fast SCRs was fairly high (about 30–40%).

Parameter Changed	Device	Columns	1st (μs)	2nd (μs)
I_{GT} Increase	2N6508	AI	68	68
	MCR2150	AF	3.15	3.13
	2N6398	AG	48	48
	MCR2080	AG	4.7	4.7
	2N6240	AI	44.8	41.4
	C106D	HI	27	27
Decrease R_{GK} 1 k to 100 ohms	2N6508	AH	68	65
	MCR2150	DF	3.13	3.1
	2N6398	AG	48	45
	MCR2080	AH	4.7	4.8
	2N6240	GI	41.4	32.7
Increase R_{GK} 1 k to ∞	2N6508	EF	60	64
	MCR2150	DE	3.1	3.13
	2N6398	DF	32	35.5
	MCR2080	DF	3.3	2.5
	2N6240	CH	26.2	37.2
V_{DX}	C106D	DC	26	26
	2N6240	BC	26.2	26
	MCR100-6	FG	14.4	14.4
	2N5063	DG	31	31.7
	2N5061	DE	20.2	19.8
Decrease dv/dt Rate	2N6508	EH	65	60
	MCR2150	DG	3.1	3.3
	MCR2080	HI	4.8	4.9
	C106D	HJ	29	27
	2N6240	DF	30	27.7
Increase I_{TM}	2N6508	EG	60	64
	MCR2150	AH	3.15	3.8
	2N6398	DE	32	33
	MCR2080	BC	2.3	2.4
	C106D	EH	26	27
	2N6240	DC	26.2	27.7
		DE	27.7	28.6
		CE	26.2	28.6
	MCR100-6	CF	13.5	14.4
	2N5063	CD	30.7	31
	2N5061	BE	19.1	20.7

Table 5.II. The Effects of Changing Parameters on t_q

Device	Gate Bias		Conditions		$+V_1$	RI	dv/dt (v/μs)
	0V	−5 V	$-V_2 = -10$ V, $I_F = 3$ A		50 V	1 k/50	2.5/50
	t_q[1]	t_q[2]	Diode DI	dv/dt (V/μs)	Remarks		
2N6508	40 μs	30 μs	Slow MR502	2.5	Slow diode faster than fast diode, (lower t_q)		
2N6240	16 μs	9 μs	Slow	2.5	Slow diode faster. 2.5 V/μs faster than 50 V/μs		
2N6398	30 μs	25 μs	Slow	2.5	Tested slow diode only		
C106D	13 μs	8 μs	Slow	2.5	Tested slow diode only		
MCR2150	4 μs	3.7 μs	Fast MR856	50	2.5 V/μs does not t_q. Both diodes work.		
MCR2080	2.5 μs	2.3 μs	Fast	50	50 V/μs & fast diode only work. $-V_2 \leq -8$ V.		

Table 5.III. The Effects of Gate Bias on t_q

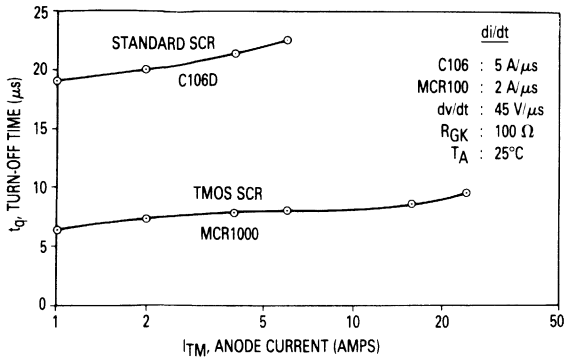


Figure 5.8. Standard SCR & TMOS SCR Turn-Off Time t_q as a Function of Anode Current I_{TM}

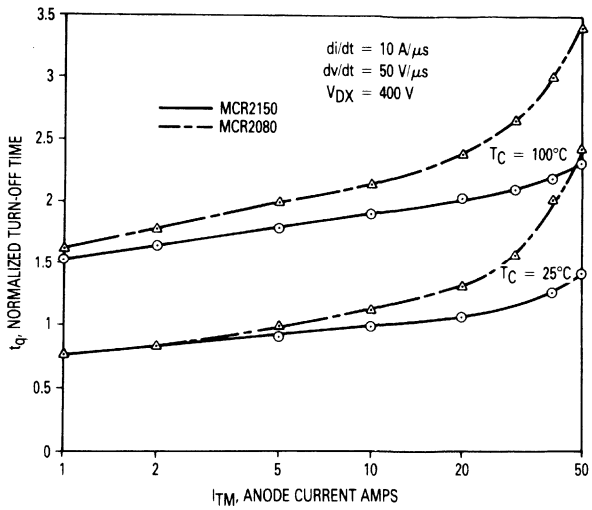


Figure 5.9. Normalized Turn-Off Time t_q as a Function of Anode Current I_{TM} for Fast SCRs. Case Temperature T_C at 25°C & 100°C

REVERSE CURRENT MAGNITUDE (I_{RM})

The reverse current is actually due to the stored charge clearing out of the SCR's junctions when a negative voltage is applied to the SCR anode. I_{RM} is very closely related to the di/dt rate; an increasing di/dt rate causing an increase of I_{RM} and a decreasing di/dt rate causing a lower I_{RM}.

By using different series inductors and changing the negative anode turn-off voltage, it is possible to keep the di/dt rate constant while changing I_{RM}. It was found that I_{RM} has little or no effect on t_q when it is the only variable changed (see Table 5.I C106D, Columns F and G, for example).

REVERSE ANODE VOLTAGE (V_{RM})

Reverse anode voltage has a strong effect on the I_{RM} magnitude and the di/dt rate, but when V_{RM} alone is varied, with I_{RM} and di/dt held constant, little or no change in t_q time was noticed. V_{RM} must always be within the reverse voltage of the device.

REAPPLIED dv/dt RATE

Varying the reapplied dv/dt rate across the range of dv/dt's commonly encountered can vary the t_q of a given SCR by more than 10.0%. The effect of the dv/dt rate on t_q is due to the Anode-Gate capacitance. The dv/dt ap-

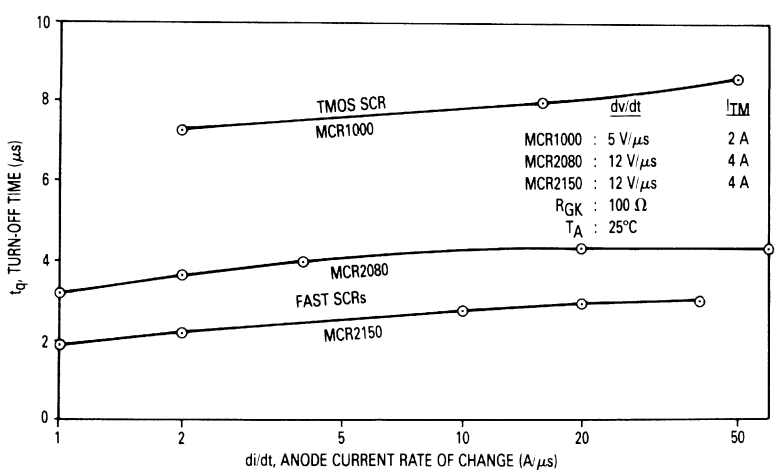


Figure 5.10. Turn-Off Time t_q as a Function of Anode Current Rate of Change di/dt

plied at the SCR anode injects current into the gate through this capacitance (i_{GT} = C dv/dt). As the dv/dt rate increased, the gate current also increases and can trigger the SCR on. To complicate matters, this injected current also adds to the current due to leakage or stored charge left in the junctions just after turn-off.

The stored charge remaining in the center junction is the main reason for long t_q times and, for the most part, the charge is removed by the recombination process. If the reapplied dv/dt rate is high, more charge is injected into this junction and prevents it from returning to the blocking state, as soon as if it were a slow dv/dt rate. The higher the dv/dt rate, the longer the t_q times will be.

MAGNITUDE LIMIT OF REAPPLIED dv/dt (V_{DX})

Changing the magnitude limit of the reapplied dv/dt voltage has little or no effect on a given SCR's t_q time when the maximum applied voltage is well below the voltage breakdown of the SCR. The t_q times will lengthen if the SCR is being used near its voltage breakdown, since the leakage present near breakdown is higher than at lower voltage levels. The leakage will lengthen the time it takes for the charge to be swept out of the SCR's center junction, thus lengthening the time it takes for this junction to return to the blocking state.

GATE CATHODE RESISTANCE (R_{GK})

In general, the lower the R_{GK} is, the shorter the t_q time will be for a given SCR. This is because low R_{GK} aids in the removal of stored charge in the SCR's junctions. An approximate 15% change in the t_q time is seen by changing R_{GK} from 100 ohms to 1000 ohms for the DUTs.

GATE DRIVE MAGNITUDE (I_{GT})

Changing the gate drive magnitude has little effect on a SCR's t_q time unless it is grossly overdriven or underdriven. When it is overdriven, there is an unnecessary large amount of charge in the SCR's junction. When underdriven, it is possible that only a small portion of the chip at the gate region turns on. If the anode current is not large enough to spread the small turned on region, there is a high current and charge density in this region that consequently lengthens the t_q time.

FORWARD CURRENT DURATION

Forward current duration had no measurable effect on t_q time when varied from 100 μs to 300 μs, which were the limits of the Motorola t_q Tester. Longer I_{TM} durations heat up the SCR which causes temperature effects; very short I_{TM} durations affect the t_q time due to the lack of time for the charges in the SCR's junctions to reach equilibrium, but these effects were not seen in the range tested.

REVERSE GATE BIAS VOLTAGE

As in transistor operation, reverse biasing the gate of the SCR decreases the turn-off time, due to the rapid "sweeping out" of the stored charge. The reduction in t_q for standard SCRs is quite pronounced, approaching perhaps 50% in some cases; for fast SCRs, only nominal improvement might result. Table 5.III shows this effect on six SCRs where the gate bias was set for 0 V and −5 V, respectively (the 1 k gate resistor of the DUT was either grounded or returned to −5 V). Due to the internal, monolithic resistor of most SCRs, the actual reverse bias voltage between the gate-cathode is less than the reverse bias supply.

1

CHARACTERIZING SCRs FOR CROWBAR APPLICATIONS

The use of a crowbar to protect sensitive loads from power supply overvoltage is quite common and, at the first glance, the design of these crowbars seems like a straightfoward, relatively simple task. The crowbar SCR is selected so as to handle the overvoltage condition and a fuse is chosen at 125 to 250% of the supply's rated full-load line current. However, upon further investigation, other questions and problems are encountered.

How much overvoltage and for how long (energy) can the load take this overvoltage? Will the crowbar respond too slowly and thus not protect the load or too fast resulting in false, nuisance triggering? How much energy can the crowbar thyristor (SCR) take and will it survive until the fuse opens or the circuit breaker opens? How fast will the fuse open, and at what energy level? Can the fuse adequately differentiate between normal current levels — including surge currents — and crowbar short circuit conditions?

It is the attempt of this section to answer these questions — to characterize the load, crowbar, and fuse and thus to match their characteristics to each other.

The type of regulator of most concern is the low voltage, series pass regulator where the filter capacitors to be crowbarred, due to 60 Hz operation, are relatively large and the charge and energy stored correspondingly large. On the other hand, switching regulators operating at about 20 kHz require smaller capacitors and thus have lower crowbar constraints.

These regulators are quite often line-operated using a high voltage, two-transistor inverter, half bridge or full bridge, driving an output step-down transformer. If a transistor were to fail, the regulator-transformed power would be less and the output voltage would drop, not rise, as is the case for the linear series regulator with a

shorted pass transistor. Thus, the need for overvoltage protection of these types of switching regulators is minimized.

This premise, however, does not consider the case of the lower power series switching regulator where a shorted transistor would cause the output voltage to rise. Nor does it take into account overvoltage due to transients on the output bus or accidental power supply hookup. For these types of operations, the crowbar SCR should be considered.

1

HOW MUCH OVERVOLTAGE CAN THE LOAD TAKE?

Crowbar protection is most often needed when ICs are used, particularly those requiring a critical supply voltage such as TTL or expensive LSI memories and MPUs.

If the load is 5 V TTL, the maximum specified continuous voltage is 7 V. (CMOS, with its wide power supply range of 3 to 18 V, is quite immune to most overvoltage conditions.) But, can the TTL sustain 8 V or 10 V or 15 V and, if so, for how long and for how many power cycles? Safe Operating Area (SOA) of the TTL must be known. Unfortunately, this information is not readily available and has to be generated.

Using the test circuit illustrated in Appendix III, a quasi-SOA curve for a typical TTL gate was generated (Figure 5.11). Knowing this overvoltage-time limit, the crowbar and fuse energy ratings can be determined.

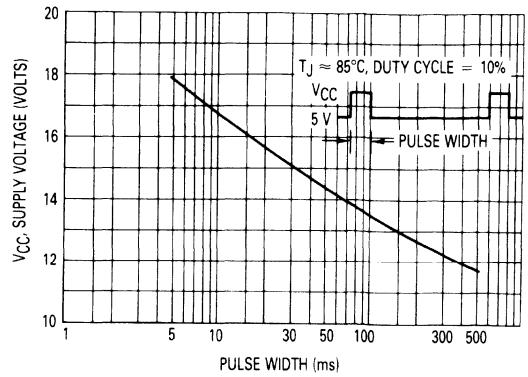
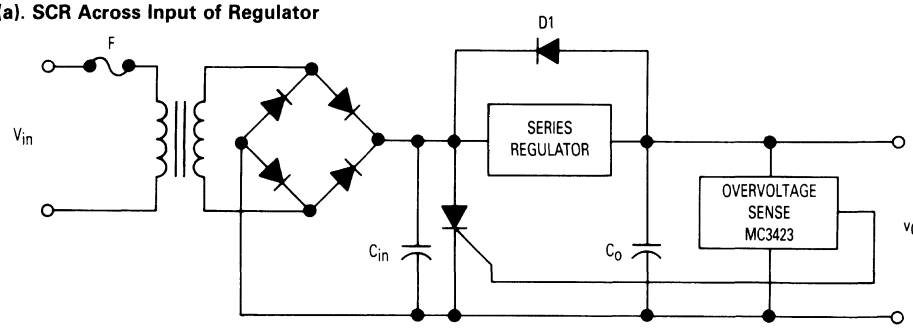


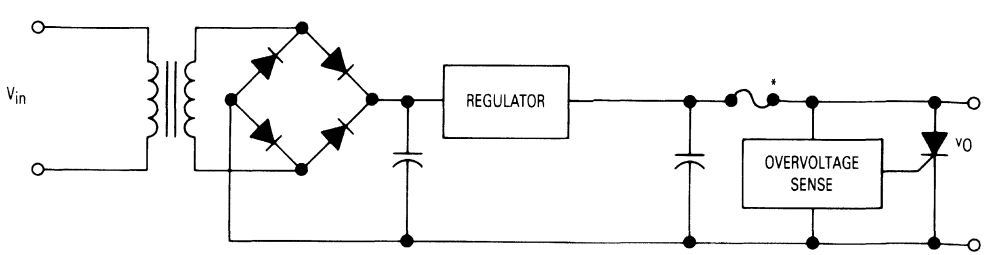
Figure 5.11. Pulsed Supply Voltage versus Pulse Width

The two possible configurations are illustrated in Figure 5.12, the first case shows the crowbar SCR across the input of the regulator and the second, across the output. For both configurations, the overvoltage comparator senses the load voltage at the remote load terminals, par-

(a). SCR Across Input of Regulator



(b). SCR Across Output of Regulator



*NEEDED IF SUPPLY NOT CURRENT LIMITED

Figure 5.12. Typical Crowbar Configurations

ticularly when the I_R drop of the supply leads can be appreciable. As long as the output voltage is less than that of the comparator reference, the crowbar SCR will be in an off state and draw no supply current. When an over-voltage condition occurs, the comparator will produce a gate trigger to the SCR, firing it, and thus clamping the regulator input, as in the first case — to the SCRs on-state drop of about 1 to 1.5 V, thereby protecting the load.

Placing the crowbar across the input filter capacitors, although effectively clamping the output, has several disadvantages.

1. There is a stress placed on the input rectifiers during the crowbarring short circuit time before the line fuse opens, particularly under repeated operation.
2. Under low line conditions, the minimum short circuit current can be of the same magnitude as the maximum primary line current at high line, high load, making the proper fuse selection a difficult choice.
3. The capacitive energy to be crowbarred (input and output capacitor through rectifier D1) can be high.

When the SCR crowbar and the fuse are placed in the dc load circuit, the above problems are minimized. If crowbarring occurs due to an external transient on the line and the regulator's current limiting is working properly, the SCR only has to crowbar the generally smaller output filter capacitor and sustain the limited regulator current.

If the series pass devices were to fail (short), even with current limiting or foldback disabled, the crowbarred energy would generally be less than of the previous case. This is due to the higher impedance of the shorted regulator (due to emitter sharing and current sensing resistors) relative to that of rectifier D1.

Fuse selection is much easier as a fault will now give a greater percentage increase in dc load current than when measuring transformer primary or secondary rms current. The disadvantage, however, of placing the fuse in the dc load is that there is no protection for the input rectifier, capacitor, and transformer, if one of these components were to fail (short). Secondly, the one fuse must protect not only the load and regulator, but also have adequate clearing time to protect the SCR, a situation which is not always readily accomplished. The input circuitry can be protected with the addition of a primary fuse or a circuit breaker.

HOW MUCH ENERGY HAS TO BE CROWBARRED?

This is dictated by the power supply filter capacitors, which are a function of output current. A survey of several linear power supply manufacturers showed the output filter capacitor size to be from about 100 to 400 microfarads per ampere with about 200 μF/A being typical. A 30 A regulator might therefore have a 6000 μF output filter capacitor.

Additionally, the usually much larger input filter capacitor will have to be dumped if the regulator were to short, although that energy to be dissipated will be dependent on the total resistance in the circuit between that capacitor and the SCR crowbar.

The charge to be crowbarred would be

$$Q = CV = I_T,$$

the energy,

$$E = 1/2\ CV^2,$$

and the peak surge current

$$i_{pk} = \frac{V_C}{R_T}$$

When the SCR crowbars the capacitor, the current waveform will be similar to that of Figure 5.13, with the peak surge current, i_{pk}, being a function of the total impedance in the circuit (Figure 5.14) and will thus be limited by the Equivalent Series Resistance (ESR) and inductance (ESL) of the capacitor plus the dynamic impedance of the SCR, any external current limiting resistance, (and inductance) of the interconnecting wires and circuit board conductors.

The ESR of computer grade capacitors, depending on the capacitor size and working voltage, might vary from 10 to 1000 milliohms (mΩ). Those used in this study were in the 25 to 50 mΩ range.

The dynamic impedance of the SCR (the slope of the on-state voltage, on-state current curve), at high currents, might be in the 10 to 20 mΩ range. As an example, from the on-state characteristics of the MCR70, 35 A rms SCR, the dynamic impedance is

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{(4.5 - 3.4)V}{(300 - 200)A} = \frac{1.1\ V}{100\ A} \cong 11\ m\Omega.$$

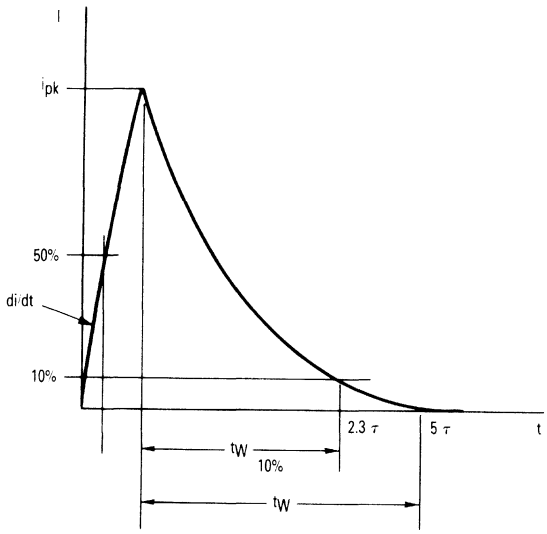
The interconnecting wire might offer an additional 5 mΩ (#20 solid copper wire $\cong$ 20 mΩ/ft) so that the total circuit resistance, without additional current limiting, might be in the 40 to 70 mΩ range. The circuit inductance was considered low enough to ignore so far as i_{pk} is concerned for this exercise, being in hundreds of nanohenry range (ESL $\cong$ 3 nH, L wire $\cong$ 500 nH/ft). However, di/dt will be affected by the inductance.

HOW MUCH ENERGY CAN THE CROWBAR SCR SUSTAIN?

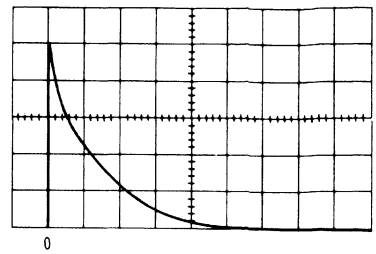
There are several factors which contribute to possible SCR failures or degradation — the peak surge current, di/dt, and a measure of the device's energy capability, I^2t.

If the peak current and/or duration of the surge is large, destruction of the device due to excessive dissipation can occur. Obviously, the i_{pk} can be reduced by inserting additional impedance in the crowbar path, at an increase in dump time. However, this time, which is a measure of how long the overvoltage is present, should be within the SOA of the load.

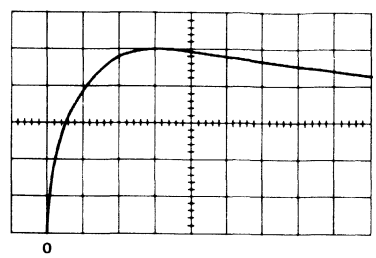
The energy stored in the capacitor being a constant for a particular voltage would suggest that the I^2t integral for any limiting resistance is also a constant. In reality,



CROWBAR CURRENT TERMS



t = 0.5 ms/Div



t = 10 μs/Div

I = 200 A/Div
MCR69
C = 22,000 μF

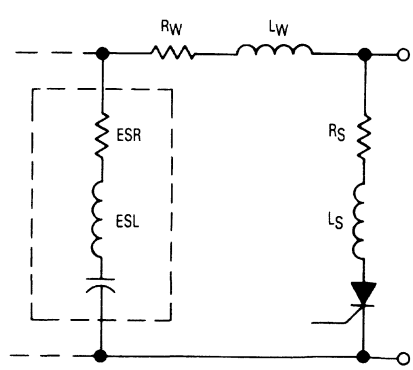
R_S = 0
V_C = 30 V
I_{GT} = 200 mA

Figure 5.13. Typical SCR Crowbar Waveform

this is not the case as the thermal response of the device must be taken into consideration. It has been shown that the dissipation capability of a device varies as to the $\sqrt{t}$ for the first tens of milliseconds of the thermal response and, in effect, the measure of a device's energy capability would be closer to $i^2\sqrt{t}$. This effect is subsequently illustrated in the empirically derived i_{pk} versus time derating curves being a non-linear function. However, for comparison with fuses, which are rated in I^2t, the linear time base, "t," will be used.

The di/dt of the current surge pulse is also a critical parameter and should not exceed the device's ratings (typically about 200 A/μs for 50 A or less SCRs). The magnitude of di/dt that the SCR can sustain is controlled by the device construction and, to some extent, the gate drive conditions. When the SCR gate region is driven on, conduction across the junction starts in a small region and progressively propagates across the total junction. Anode current will initially be concentrated in this small conducting area, causing high current densities which can degrade and ultimately destroy the device. To minimize this di/dt effect, the gate should be turned on hard and fast such that the area turned on is initially maximized. This can be accomplished with a gate current pulse approaching five times the maximum specified continuous gate current, I_{gt}, and with a fast rise time (< 1 μs). The gate current pulse width should be greater than the propagation time; a figure of 10 μs minimum should satisfy most SCRs with average current ratings under 50 A or so.

The wiring inductance alone is generally large enough to limit the di/dt. Since most SCRs are good for over 100 A/μs, this effect is not too large a problem. However, if the di/dt is found excessive, it can be reduced by placing



R_W, L_W: INTERCONNECTING WIRE IMPEDANCE
R_S, L_S: CURRENT LIMITING IMPEDANCE

Figure 5.14. Circuit Elements Affecting SCR Surge Current

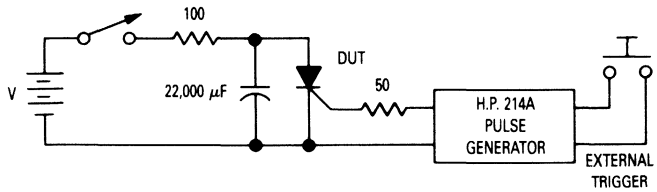


Figure 5.15

an inductance in the loop; but, again, this increases the circuit's response time to an overvoltage and the trade-off should be considered.

Since many SCR applications are for 60 Hz line operation, the specified peak non-repetitive surge current I_{TSM} and circuit fusing I^2t are based on 1/2 cycle (8.3 ms) conditions. For some SCRs, a derating curve based on up to 60 or 100 cycles of operation is also published. This rating, however, does not relate to crowbar applications. To fully evaluate a crowbar system, the SCR must be characterized with the capacitor dump exponential surge current pulse.

A simple test circuit for deriving this pulse is shown in Figure 5.15, whereby a capacitor is charged through a limiting resistor to the supply voltage, V, and then the charge is dumped by the SCR device under test (DUT). The SCR gate pulse can be varied in magnitude, pulse width, and rise time to produce the various I_{GT} conditions. An estimate of the crowbar energy capability of the DUT is determined by first dumping the capacitor charged to a low voltage and then progressively increasing the voltage until the DUT fails. This is repeated for several devices to establish an average and minimum value of the failure points cluster.

This procedure was used to test several different SCRs of which the following Table 5.IV describes several of the pertinent energy specifications and also the measured crowbar surge current at the point of device failure.

This one-shot destruct test was run with a gate current of five $I_{GT(MAX)}$ and a 22,000 μF capacitor whose ESR produced the exponentially decaying current pulse about 1.5 ms wide at its 10% point. Based on an appropriate derating, ten devices of each line where then successfully tested under the following conditions.

Device	V_C	i_{pk}	t
MCR68	12 V	250 A	1.5 ms
MCR69	30 V	800 A	1.5 ms
MCR70	30 V	800 A	1.5 ms

To determine the effect of gate drive on the SCRs, three devices from each line were characterized at non-destruct levels using three different capacitors (200, 6,000, and 22,000 μF), three different capacitor voltages (10, 20, and 30 V), and three different gate drives ($I_{GT(MAX)}$, 5 $I_{GT(MAX)}$, and a ramp $I_{GT(MAX)}$ with a di/dt of about 1 mA/μs). Due to its energy limitations, the MCR68 was tested with only 10 V across the larger capacitors.

The slow ramp, I_{GT}, was used to simulate overvoltage sense applications where the gate trigger rise time can be slow such as with a coupling zener diode.

No difference in SCR current characteristics were noted with the different gate current drive conditions; the peak currents were a function of capacitor voltage and circuit impedance, the fall times related to R_TC, and the rise times, t_r, and di/dt, were more circuit dependent (wiring inductance) and less device dependent (SCR turn-on time, t_{on}). Since the wiring inductance limits, t_r, the effect of various I_{GT}s was masked, resulting in virtually identical waveforms.

The derated surge current, derived from a single (or low number) pulse test, does not truly reflect what a power supply crowbar SCR might have to see over the life of the supply. Life testing over many cycles have to be performed; thus, the circuit described in Appendix IV was developed. This life test fixture can simultaneously

Table 5.IV. Specified and Measured Current Characteristics of Three SCRs

Device	Case	Maximum Specified Values					Measured Crowbar Surge Current I_{pk}		
		$I_{T(rms)}$ (A)	$I_{T(AV)}$ (A)	I_{TSM}* (A)	I^2t (A^2s)	$I_{GT(Max)}$ (mA)	Min (A)	Max (A)	Ave (A)
MCR68	TO-220	12	8	100	40	30	380	750	480
MCR69	TO-220	25	16	300	375	30	1050	1250	1100
MCR70	TO-208	35	22	350	510	30	1100	1300	1200

*I_{TSM} = Peak Non-Repetitive Surge Current, 1/2 cycle sine wave, 8.3 ms.

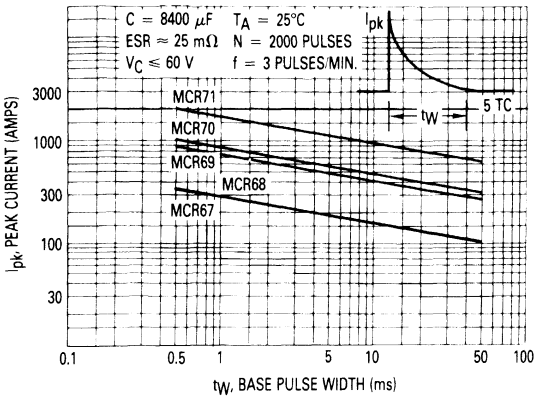
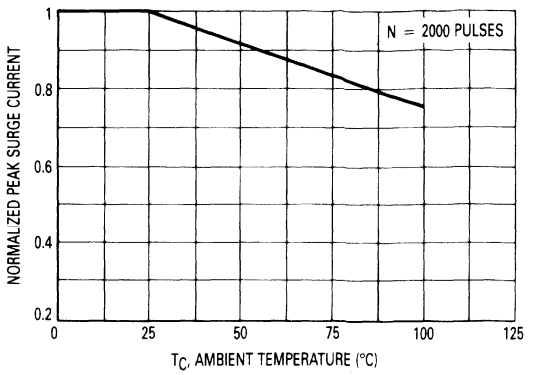


Figure 5.16(a). Peak Surge Current versus Pulse Width



(b). Peak Surge Current versus Ambient Temperature

test ten SCRs under various crowbar energy and gate drive conditions.

Each of the illustrated SCRs of Figure 5.16(a) were tested with as many as four limiting resistors (0, 50, 100, and 240 mΩ) and run for 1000 cycles at a nominal energy level. If no failures occurred, the peak current was progressively increased until a failure(s) resulted. Then the current was reduced by 10% and ten new devices were tested for 2000 cycles (about six hours at 350 cycles/hour). If this test proved successful, the data was further derated by 20% and plotted as shown on log-log paper with a slope of − 1/4. This theoretical slope, due to the $I^2\sqrt{t}$ one-dimensional heat-flow relationship (see Appendix VI), closely follows the empirical results. Of particular interest is that although the peak current increases with decreasing time, as expected, the I^2t actually decreases.

Figure 5.16(b) shows the effect of elevated ambient temperature on the peak current capability of the illustrated SCRs.

FUSE CHARACTERISTICS

SCRs, like rectifiers, are generally rated in terms of average forward current, $I_{T(AV)}$, due to their half-wave operation. Additionally, an rms forward current, $I_{T(rms)}$, a peak forward surge current, I_{TSM}, and a circuit-fusing energy limit, I^2t, may be shown. However, these specifications, which are based one-half cycle 60 Hz operation, are not related to the crowbar current pulse and some means must be established to define their relationship. Also, fuses which must ultimately match the SCR and the load, are rated in rms currents.

The crowbar energy curves are based on an exponentially decaying surge current waveform. This can be converted* to I_{rms} by the equation.

$$I_{rms} = 0.316\ i_{pk}$$

which now allows relating the SCR to the fuse.

The logic load has its own overvoltage SOA as a function of time (Figure 5.11). The crowbar SCR must clamp the overvoltage within a specified time, and still be within its own energy rating; thus, the series-limiting resistance, R_S, in the crowbar path must satisfy both the load and SCR energy limitations. The overvoltage response time is set by the total limitations. The overvoltage response time is set by the total limiting resistance and dumped capacitor(s) time constant. Since the SOA of the TTL used in this exercise was derived by a rectangular overvoltage pulse (in effect, over-energy), the energy equivalent of the real-world exponentially falling voltage waveform must be made. An approximation can be made by using an equivalent rectangular pulse of 0.7 times the peak power and 0.7 times the base time.

Once an overvoltage is detected and the crowbar is enabled, in addition to sustaining the peak current, the SCR must handle the regulator short-circuit current for the time it takes to open the fuse.

Thus, all three elements are tied together — the load can take just so much overvoltage (over-energy) and the crowbar SCR must repeatedly sustain for the life of the equipment an rms equivalent current pulse that lasts for the fuse response time.

It would seem that the matching of the fuse to the SCR would be straightforward — simply ensure that the fuse rms current rating never exceed the SCR rms current rating (Figure 5.17), but still be sufficient to handle steady-state and normal overload currents. The more exact relationship would involve the energy dissipated in the system $\int I^2R dt$, which on a comparative basis, can be reduced to I^2t. Thus, the "let-through" I^2t of the fuse should not exceed I^2t capability of the SCR under all operating conditions. These conditions are many, consisting of "available fault current," power factor of the load, supply voltage, supply frequency, ambient temperature, and various fuse factors affecting the I^2t.

There has been much detailed information published on fuse characteristics and, rather than repeat the text which would take many pages, the reader is referred to those sources. Instead, the fuse basics will be defined

*See Appendix V

and an example of matching the fuse to the SCR will be shown.

In addition to interrupting high current, the fuse should limit the current, thermal energy, and overvoltage due to the high current. Figure 5.18 illustrates the condition of the fuse at the moment the over-current starts. The peak let-through current can be assumed triangular in shape for a first-order approximation, lasting for the clearing time of the fuse. This time consists of the melting or pre-arcing time and the arcing time. The melting time is an inverse function of over-current and, at the time that the fuse element is opened, an arc will be formed causing the peak arc voltage. This arc voltage is both fuse and circuit dependent and under certain conditions can exceed the peak line voltage, a condition the user should ensure does not overstress the electronics.

The available short-circuit current is the maximum current the circuit is capable of delivering and is generally limited by the input transformer copper loss and reactance when the crowbar SCR is placed at the input to the regulator or the regulator current limiting when placed at the output. For a fuse to safely protect the circuit, it should limit the peak let-through current and clear the fault in a short time, usually less than 10 ms.

Fuse manufacturers publish several curves for characterizing their products. The current-time plot, which describes current versus melting time (minimum time being 10 ms), is used in general industrial applications, but is not adequate for protecting semiconductors where the clearing time must be in the subcycle range. Where protection is required for normal multicycle overloads, this curve is useful.

Two other useful curves, the total clearing I^2t characteristic and the peak let-through current I_{PLT} characteristic, are illustrated in Figures 5.19 and 5.20 respectively. Some vendors also show total clearing time curves (overlayed on Figure 5.19 as dotted lines) which then allows direct comparison with the SCR energy limits. When this clearing time information is not shown, then the designer should determine the I_{PLT} and I^2t from the respective curves and then solve for the clearing time from the approximate equation relating these two parameters. Assuming a triangular waveform for I_{PLT}, the total clearing time, t_c, would then approximately be

$$t_c \approx \frac{3\, I^2t}{I_{PLT}^2}$$

Once t_c of the fuse is known, the comparison with the SCR can readily be made. As long as the I^2t of the fuse is less than the I^2t of the SCR, the SCR is protected. It should be pointed out that these calculations are predicated on a known value of available fault current. By inspection of Figure 5.20, it can be seen that I_{PLT} can vary greatly with available fault current, which could have a marked effect on the degree of protection. Also, the illustrated curves are for particular operating conditions; the curves will vary somewhat with applied voltage and frequency, initial loading, load power factor, and ambient temperature. Therefore, the reader is referred to the manufacturer's data sheet in those cases where extrapolation will be required for other operating conditions. The final proof is obtained by testing the fuse in the actual circuit under worst-case conditions.

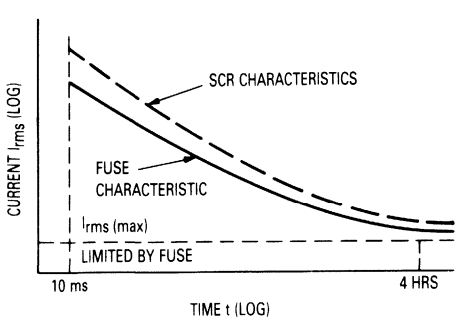


Figure 5.17. Time-Current Characteristic Curves of a Crowbar SCR and a Fuse

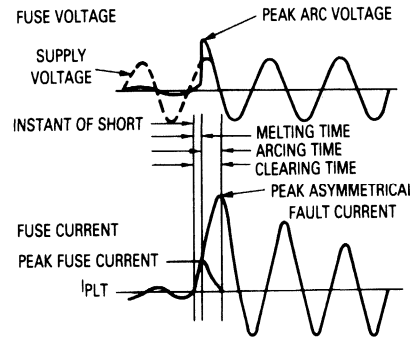


Figure 5.18. Typical Fuse Timing Waveforms During Short Circuit

CROWBAR EXAMPLE

To illustrate the proper matching of the crowbar SCR to the load and the fuse, consider the following example. A 50 A TTL load, powered by a 60 A current limited series regulator, has to be protected from transients on the supply bus by crowbarring the regulator output. The output filter capacitor of 10,000 μF (200 μF/A) contributes most of the energy to be crowbarred (the input capacitor is current limited by the regulator). The transients can reach 18 V for periods of 100 ms.

Referring to Figure 5.11, it is seen that this transient exceeds the empirically derived SOA. To ensure safe operation, the overvoltage transient must be crowbarred within 5 ms. Since the TTL SOA is based on a rectangular power pulse even though plotted in terms of voltage, the equivalent crowbarred energy pulse should also be derived. Thus, the exponentially decaying voltage waveform should be multiplied by the exponentially decaying current to result in an energy waveform proportional to

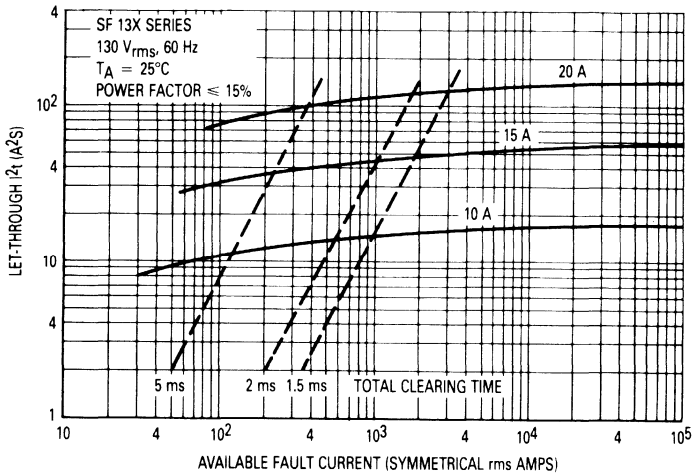


Figure 5.19. Maximum Clearing I^2t Characteristics for 10 to 20 A Fuses

e^{-2x}. The rectangular equivalent will have to be determined and then compared with the TTL SOA. However, for simplicity, by using the crowbarred exponential waveform, a conservative rating will result.

To protect the SCR, a fuse must be chosen that will open before the SCR's I^2t is exceeded, the current being the regulator limiting current which will also be the available fault current to the fuse.

The fuse could be eliminated by using a 60 A SCR, but the cost versus convenience trade-off of not replacing the fuse is not warranted for this example. A second fuse or circuit breaker will protect the rectifiers and regulator for internal faults (shorts), but its selection, which is based on the respective energy limits of those components, is not part of this exercise.

If a crowbar discharge time of 3 ms were chosen, it would not only be within the rectangular pulsed SOA, but also be well within the derived equivalent rectangular model of the exponential waveform. It would also require about 1.3 time constants for the overvoltage to decay from 18 V to 5 V; thus, the RC time constant would be 3 ms/1.3 or 2.3 ms.

The limiting resistance, R_S would simply be

$$R_S = \frac{2.3\ \text{ms}}{10{,}000\ \mu\text{F}} = 0.23\ \Omega \cong 0.2\ \Omega$$

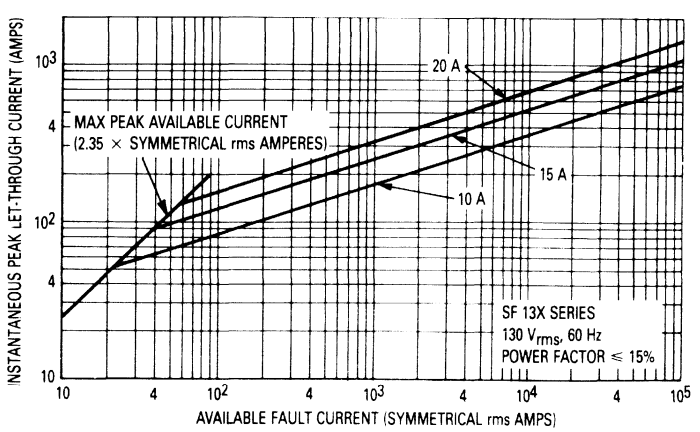


Figure 5.20. Peak Let-Through Current versus Fault Current for 10 to 20 A Fuses

Since the capacitor quickly charges up to the overvoltages V_{CC1} of 18 V, the peak capacitor discharge current would be

$$I_{pk} = \frac{V_{CC1}}{R_S} = \frac{18\ V}{0.2\ \Omega} = 90\ A$$

The rms current equivalent for this exponentially decaying pulse would be

$$I_{rms} = 0.316\ I_{pk} = 0.316(90) = 28.4\ A\ rms$$

Now referring to the SCR peak current energy curves (Figure 5.16), it is seen that the MCR68 can sustain 210 A peak for a base time of 3 ms. This 12 A SCR must also sustain the 60 A regulator limited current for the time required to open the fuse. The MCR68 has a specified peak forward surge current rating of 100 A (1/2 cycle, sine wave, 60 Hz, non-repetitive) and a circuit fusing rating of 40 A^2s.

The non-repetitive rating implies that the device can sustian 100 occurrences of this 1/2 cycle surge over the life of the device; the SCR crowbar surge current curves were based on 2000 cycles.

For the 3 ms time frame, the $I_1{}^2t_1$ for the exponential waveform is

$$I_1{}^2t_1 = (28.4\ A)^2(3\ ms) = 2.4\ A^2s$$

Assuming that the fuse will open within 6 ms, the approximate energy that the SCR must sustain would be 60 A for an additional 3 ms. By superposition, this would amount to

$$I_2{}^2t_2 = (60\ A)^2(6\ ms) = 21.6\ A^2s$$

which, when added to the exponential energy, would result in 24 A^2.

The MCR68 has a 40 A^2s rating based on a 1/2 cycle of 8.3 ms. Due to the one-dimensional heat flow in the device, the energy capability is not linearly related to time, but varies as to the $\sqrt{t}$. Therefore, with a 6 ms 1/2-cycle sine wave, the 40 A^2t rating would now decrease to approximately (see Appendix VI for derivation).

$$\begin{aligned} I_2{}^2t_2 &= I_1{}^2t_1\left(\frac{t_2}{t_1}\right)^{1/2} \\ &= 40\ A^2s\left(\frac{6\ ms}{8.3\ ms}\right)^{1/2} \\ &= 34\ A^2s \end{aligned}$$

Although the 1/2 cycle extrapolated rating is greater than the actual crowbar energy, it is only characterized for 100 cycles of operation.

To ensure 2000 cycles of operation, at a somewhat higher cost, the 25 A MCR69 could be chosen. Its exponential peak current capability, at 3 ms, is about 560 A and has a specified I_{TSM} of 300 A for 8.3 ms. The I^2t rating is not specified, but can be calculated from the equation

$$I^2t = \frac{(I_{TSM})^2}{2}t = \frac{(300\ A)^2}{2}(8.3\ ms) = 375\ A^2s$$

Extrapolating to 6 ms results in about 318 A^2s, an I^2t rating much greater than the circuit 24 A^2s value.

The circuit designer can then make the cost/performance trade-offs.

All of these ratings are predicated on the fuse opening within 6 ms.

With an available fault current of 60 A, Figure 5.19 shows that a 10 A (SF13X series) fuse will have a let-through I^2t of about 10 A^2 s and a total clearing time of about 6 ms, satisfying the SCR requirements, that is,

$$I^2t\ fuse < I^2t\ SCR$$

$$t_c \leq 6\ ms$$

Figure 5.20 illustrates that for the same conditions, instantaneous peak let-through current of about 70 A would result. For fuse manufacturers that don't show the clearing time information, the approximate time can be calculated from the triangular model, as follows

$$t_c = \frac{3\ I^2t}{I_{PLT}{}^2} = \frac{3(10)}{(70)^2} = 6.1\ ms$$

The fuse is now matched to the SCR which is matched to the logic load. Other types of loads can be similarly matched, if the load energy characteristics are known.

CHARACTERIZING SWITCHES AS LINE-TYPE MODULATORS

In the past, hydrogen thyratrons have been used extensively as discharge switches for line type modulators. In general, such devices have been highly satisfactory from an electrical performance standpoint, but they have some major drawbacks including relatively large size and weight, low efficiency (due to filament power requirements), and short life expectancy compared with semiconductor devices, now can be eliminated through the use of silicon controlled rectifiers.

A line type modulator is a modulator whose output-pulse characteristics are determined by a lumped-constant transmission line (pulse forming network) and by the proper match of the line impedance (PFN) to the load impedance.

A switch for this type modulator should only initiate conduction and should have no effect on pulse characteristics. This is in contrast to a hard switch modulator where output pulse characteristics are determined by the "hard" relationship of grid (base) control of conduction through a vacuum tube (transistor) switch.

Referring to the schematic (Figure 5.27), when the power supply is first turned on, no charge exists in the PFN, and energy is transferred from the power supply to the PFN via the resonant circuit comprising the charging choke and PFN capacitors. At the time that the voltage across the PFN capacitors reaches twice the power supply voltage, current through the charging choke tries to reverse and the power supply is disconnected due to the back biased impedance of the hold-off diode. If we assume this diode to be perfect, the energy remains stored in the PFN until the discharge switch is triggered to its on state. When this occurs, assuming that the pulse transformer has been designed to match the load impedance to the PFN impedance, all energy stored in the PFN re-

actance will be transferred to the load if we neglect switch losses. Upon completion of the transfer of energy the switch must return to its off condition before allowing transfer of energy once again from the power supply to the PFN storage element.

OPTIMUM SWITCH CHARACTERISTICS

FORWARD BREAKOVER VOLTAGE

Device manufacturers normally apply the variable-amplitude output of a half-wave rectifier across the SCR. Thus, forward voltage is applied to the device for only a half cycle and the rated voltage is applied only as an ac peak. While this produces a satisfactory rating for ac applications, it does not hold for dc.

An estimated 90% of devices tested for minimum breakover voltage (V_{BO}) in a dc circuit will not meet the data sheet performance specifications. A switch designed for the pulse modulator application should therefore specify a minimum continuous forward breakover voltage at rated maximum leakage current for maximum device temperatures.

THE OFF SWITCH

The maximum forward leakage current of the SCR must be limited to a low value at maximum device temperature. During the period of device nonconduction it is desired that the switch offer an off impedance in the range of megohms to hundreds of megohms. This is required for two reasons: (1) to prevent diminishing the efficiency of recharge by an effective shunt path across the PFN, and (2) to prevent the bleeding off of PFN charge during the interpulse period. This second factor is especially important in the design of radar tansponders wherein the period between interrogations is variable. Change of the PFN voltage during the interpulse period could result in frequency shift, pulse instabilities, and loss of power from the transmitter being modulated.

THE ON SWITCH

At present, SCR design is more limited in the achievable maximum forward sustaining voltage than in the current that the device will conduct. For this reason modulators utilizing SCRs can be operated at lower impedance levels than comparable thyratron circuits of yesterday. It is not uncommon for the characteristic impedance of the pulse forming network to be in the order of 5 to 10 ohms or less. Operating the SCR at higher current to switch the same equivalent pulse power as a thyratron requires the SCR on impedance to be much lower so that the I^2R loss is a reasonable value, in order to maintain circuit efficiency. Low switch loss, moreover, is mandatory because internal power dissipation can be directly translated into junction-temperature-rise and associated leakage current increase which, if excessive, could result in thermal runaway.

TURN-ON TIME

In radar circuits the *pulse-power* handling capability of an SCR, rather than the normally specified *average-power* capability, is of primary importance.

For short pulses at high PRFs the major portion of semiconductor dissipation occurs during the initial turn-on during the time that the anode rises from its forward leakage value to its maximum value. It is necessary, therefore, that turn-on time be as short as possible to prevent excessive power dissipation.

The function of radar is to provide distance information measured as a function of time. It is important, therefore, that any delay introduced by a component be fixed in relation to some variable parameter such as signal strength or temperature. For radar pulse modulator applications, a minimal delay variation versus temperature is required and any such variation must be repetitive from SCR to SCR, in production lots, so that adequate circuit compensation may be provided.

PULSE GATE CURRENT TO FIRE

The time of delay, the time of rise, and the delay variation versus temperature associated with SCR turn-on are functions of the gate triggering current available and the trigger pulse duration. In order to predict pulse circuit operation of the SCR, the pulse gate current required to turn the device on when switching the low-impedance modulator should be specified and the limits of turn-on-time variation for the specified pulse trigger current and collector load should be given at the high and low operating temperature extremes.

RECOVERY TIME

After the cessation of forward conducting current in the on device, a time of SCR circuit isolation must be provided to allow the semiconductor to return to its off state. Recovery time cannot be given as an independent parameter of device operation, but must include factors as determined by the external circuit, such as: (1) pulse current and rate of decay; (2) availability of an inverse voltage immediately following pulse-current conduction; (3) level of base bias following pulse current conduction; (4) rate of rise of reapplied positive voltage and its amplitude in relation to SCR breakover voltage; and (5) maximum circuit ambient temperature.

In the reverse direction the controlled rectifier behaves like a conventional silicon diode. Under worst circuit conditions, if an inverse voltage is generated through the existence of a load short circuit, the current available will be limited only by the impedance of the pulse forming network and SCR inverse characteristics. The reverse current is able to sweep out some of the carriers from the SCR junctions. Intentional design of the load impedance to something less than the network impedance allows development of an inverse voltage across the SCR immediately after pulse conduction, enhancing switch turn-off time. Careful use of a fast clamp diode in series with a fast zener diode, the two in shunt across the SCR, allows application of a safe value of circuit-inverse-voltage without preventing the initial useful reverse current. Availability of a negative base-bias following pulse current conduction provides a similar enhancement of switch turn-off time.

If removal of carriers from the SCR junction enables a

faster switch recovery time, then, conversely, operation of the SCR at high temperatures with large forward currents and with slow rate of current decay all increase device recovery time.

HOLDING CURRENT

One of the anomalies that exist in the design of a pulse SCR is the requirement for a high holding current. This need can be determined by examining the isolation component that disconnects the power supply from the discharge circuit during the time that PFN energy is being transferred to the transmitter and during the recovery time of the discharge switch. An inductance resonating with the PFN capacitance at twice the time of recharge is normally used for power supply isolation. Resonant charging restricts the initial flow of current from the power supply, thereby maximizing the time at which power supply current flow will exceed the holding current of the SCR. If the PFN recharge current from the power supply exceeds the holding current of the SCR before it has recovered, the SCR will again conduct without the application of a trigger pulse. As a result continuous conduction occurs from the power supply through the low impedance path of the charging choke and on switch. This lock-on condition can completely disable the equipment employing the SCR switch.

The charging current passed by the inductance is given as (the PFN inductance is considered negligible):

$$i_c(t) = \frac{E_{bb} - V_n(0)}{\sqrt{L_c/C_n}} \left(\frac{\cos \dfrac{T_r - 2t}{2\sqrt{L_c C_n}}}{\sin \dfrac{T_r}{2\sqrt{L_c C_n}}} \right)$$

Where

E_{bb} = power supply voltage
$V_n(0)$ = 0 volts if the PFN employs a clamp diode or is matched to the load
T_r = time of resonant recharge and is usually equal to $\frac{1}{PRF}$
L_c = value of charging inductance
C_n = value of total PFN capacity

For a given radar pulse modulator design, the values of power supply voltage, time of resonant recharge, charging choke inductance, and PFN capacitance are established. If the time (t) represents the recovery time of the SCR being used as the discharge switch, i_c then represents the minimum value of holding current required by the SCR to prevent power supply lock-on. Conversely, if the modulator design is about an existing SCR where holding current, recovery time, and forward breakover voltage are known, the charge parameters can be derived by rewriting the above formula as follows:

$$I_H = \frac{V_{BO} - V_n(0)}{\sqrt{L_c/C_n}} \left(\frac{\cos \dfrac{T_r - 2(\text{recovery time})}{2\sqrt{L_c C_n}}}{\sin \dfrac{T_r}{2\sqrt{L_c C_n}}} \right)$$

The designer may find that for the chosen SCR the desired characteristics of modulator pulse width and pulse repetition frequency are not obtainable.

One means of increasing the effective holding current of an SCR is for the semiconductor to exhibit some turn-off gain characteristic for the residual current flow at the end of the modulator pulse. The circuit designer then can provide turn-off base current, making the SCR more effective as a pulse circuit element.

THE SCR AS A UNIDIRECTIONAL SWITCH

When tirggered to its on state, the SCR, like the hydrogen thyratron, is capable of conducting current in one direction. A load short circuit could result in an inverse voltage across the SCR due to the reflection of voltage from the pulse forming network. The circuit designer may wish to provide an intentional load-to-PFN mismatch such that some inverse voltage is generated across the SCR to enhance its turn-off characteristics. Nevertheless, since the normal circuit application is unidirectional, the semiconductor device designer could take advantage of this fact in restricting the inverse-voltage rating that the SCR must withstand. The circuit designer, in turn, can accommodate this lack of peak-inverse-voltage rating by use of a suitable diode clamp across the PFN or across the SCR.

A PRACTICAL PULSE MODULATOR SCR

Motorola makes several SCRs especially designed as radar modulators, including the 2N4199, MCR729 and MCR1718 families.

One actual use of the MCR729 has been in a radar modulator requiring pulse outputs of 60 and 450 ns at a peak pulse power of 2700 watts and a PRF of 10,000 pps. Detected RF pulse rise time, to a large extent dependent on the SCR rate of current rise, is only 20 ns (Figure 5.21).

A second application (Figure 5.22) uses a single MCR729 to switch 5000 watts of peak pulse power, with a circuit recovery time of 45 μs at an 85°C ambient temperature. Maximum duty cycle of this circuit is 0.0024. The current and detected RF waveforms were obtained using an MCR729-9 with this circuit. The current pulse being switched is 18 amperes. Pulse width is approximately 0.75 μs. The rise and fall times of the detected RF pulse are both less than 50 ns.

Measurements made on the MCR729 prior to circuit use have shown the switch to be stable, fast, and efficient. Pulse "on" impedance has consistently measured less than 0.5 ohm. Delay variation versus temperature is typically ±20 ns measured from −55°C to +105°C. Time of delay averages about 300 ns.

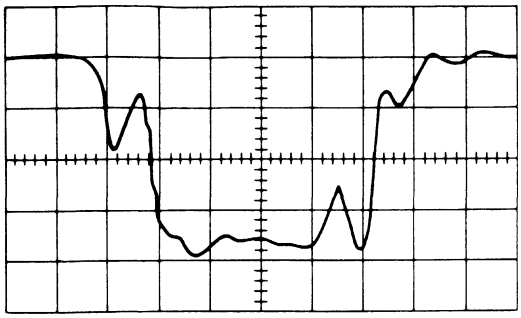


Figure 5.21. Vertical 5 A/cm; Horizontal, 0.2 μs/cm. Current Pulse Through an MCR729-9, Driving Magnetron Load

SCRs TESTS FOR PULSE CIRCUIT APPLICATION

The suitability for pulse circuit applications of SCRs not specifically characterized for such purposes can be determined from measurements carried out with relatively simple test circuits under controlled conditions. Applicable test circuits and procedures are outlined in the following section.

FORWARD BLOCKING VOLTAGE AND LEAKAGE CURRENT

Mount the SCRs to a heat sink and connect the units to be tested as shown in Figure 5.23. Place the assembly in an oven and stabilize at maximum SCR rated temperature. Turn on the power supply and raise the voltage to rated V_{BO}. Allow units to remain with the voltage applied for a minimum of four hours. At the end of the temperature soak, determine if any units exhibit thermal runaway by checking for blown fuses (without removing the power). Reject any units which have blown circuit fuses. The forward leakage current, I_{LF}, of the remaining units may be calculated after measuring the voltage V_L, across resistor R2. Any units with a leakage current greater than manufacturer's rating should be rejected.

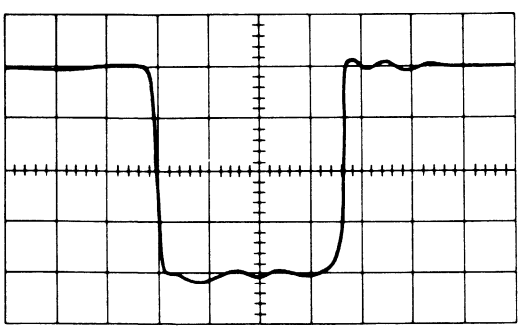


Figure 5.22. Vertical Set to 4 cm, Horizontal 0.2 μs/cm. Detected RF Magnetron Pulse

TURN-ON TIME, VARIATION AND ON IMPEDANCE

This circuit assumes that the pulse gate current required to switch a given modulator load current is specified by the manufacturer or that the designer is able to specify the operating conditions. Typical operating values might be:

Time of trigger pulse t = 1 μs
Pulse gate current I_G = 200 mA
Forward blocking voltage V_{BO} = 400 V
Load current I_{Load} = 30 A

To measure turn-on time using a Tektronix 545 oscilloscope (or equivalent) with a dual trace type CA plug-in, connect probes of Channels A and B to Test Points A and B. Place the Mode selector switch in the Added Algebraically position and the Channel B Polarity switch in the Inverted position. Adjust the HR212A pulse generator to give a positive pulse 1 μs wide (100 pps) as viewed at Test Point A. Adjust the amplitude of the "added" voltage across the 100-ohm base resistor for the specified pulse gate current (200 mA in this example).

Switch the Mode selector knob to the alternate position. Connect Channel A to Test Point D. Leave the oscilloscope probe, Channel B, at Test Point B, thereby displaying the input trigger waveform. Measure the time between the 50 percent voltage amplitudes of the two waveforms. This is the Turn-On Time ($t_D + t_R$).

To measure turn-on time versus temperature, place the device to be tested on a suitable heat sink and place the assembly in a temperature chamber. Stabilize the chamber at minimum rated (cold) temperature. Repeat the above measurements. Raise the chamber temperature to maximum rated (hot) temperature and stabilize. Repeat the measurements above.

To measure the turn-on impedance for the specified

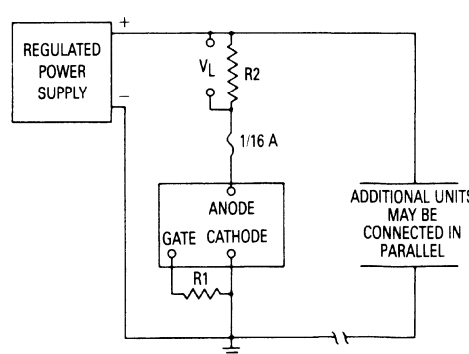


Figure 5.23. Test Setup for SCR Forward Blocking Voltage and Leakage Current Measurements

RESISTOR R1 IS USED ONLY IF MANUFACTURER CALLS FOR BIAS RESISTOR BETWEEN GATE AND CATHODE. RESISTOR R2 CAN HAVE ANY SMALL VALUE WHICH, WHEN MULTIPLIED BY MAXIMUM ALLOWABLE LEAKAGE CURRENT, WILL PROVIDE A CONVENIENT READING OF VOLTAGE V_L.

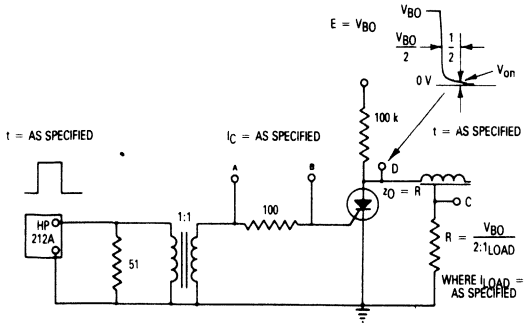


Figure 5.24. Suggested Test Circuit for SCR "On" Measurements

current load, the on impedance can be measured as an SCR forward voltage drop. The point in time of measurement shall be half the output pulse width. For a 1 μs output pulse, the measurement procedure would be:

Connect the oscilloscope probe, Channel B, to Point D shown in Figure 5.24. Use the oscilloscope controls Time/CM and Multiplier to a setting of 0.5 μs per centimeter or faster. With the Amplitude Control set to view 100 volts per centimeter (to prevent amplifier overloading) measure the amplitude of the voltage drop, V_F, across the SCR 0.5 μs after the PFN voltage waveform has dropped to half amplitude. It may be necessary to check ground reference several times during this test to provide the needed accuracy of measurement.

HOLDING CURRENT

The SCR holding current can be measured with or without a gate turn-off current, according to the position of switch S2. The Motorola Trigger Pulse Generator is a transistor circuit capable of generating a 1.5 μs turn-on pulse followed by a variable-duration turn-off pulse. Measurements should be made at the maximum expected temperature of operation. Resistor R1 should be chosen to allow an initial magnitude of current flow at the device pulse current rating.

To measure holding current, connect the SCRs under test as illustrated in Figure 5.25. Place SCRs in oven and stabilize at maximum expected operating temperature. View the waveform across R1 by connecting the oscilloscope probe (Tektronix 2465) Channel A to Point A, and Channel B to Point B. Place the Mode Selector switch in the Added Algebraically position. Place the Polarity swich of Channel B in the Inverted position. Adjust both Volts/CM switches to the same scale factor, making sure that each Variable knob is in its Calibrated position. Adjust pulse generator for a positive pulse, 1 μs wide, and 1,000 pps pulse repetition frequency. Adjust power supply voltage to rated V_{BO}. Adjust input pulse amplitude until unit fully triggers. Measure amplitude of voltage drop across R1, V(A − B), and calculate holding current in mA from the equation

$$mA = \frac{V(A - B)}{R1} + \frac{V_{BO}}{100\ k\Omega}$$

Any unit which turns on but does not turn off has a holding current of less than

$$\frac{V_{BO}\ V}{100\ k\Omega}$$

The approximate voltage setting to view the amplitude of the holding current will be 10 or 20 volts per centimeter. The approximate sweep speed will be 2 to 5 μs per centimeter. These settings will, of course, vary, depending upon the holding current of the unit under test.

SCR recovery time is greatly dependent upon the circuit in which the device is used. However, any test of SCR recovery time should suffice to compare devices of various manufacturers, as long as the test procedure is standardized. Further evaluation of the selected devices could be made in an actual modulator circuit tester wherein techniques conducive to SCR turn-off are used.

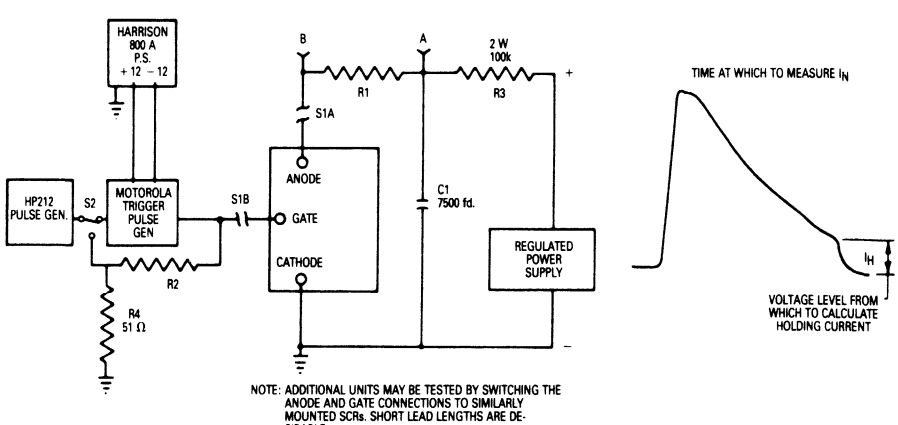


Figure 5.25. Test Setup for Measuring Holding Current

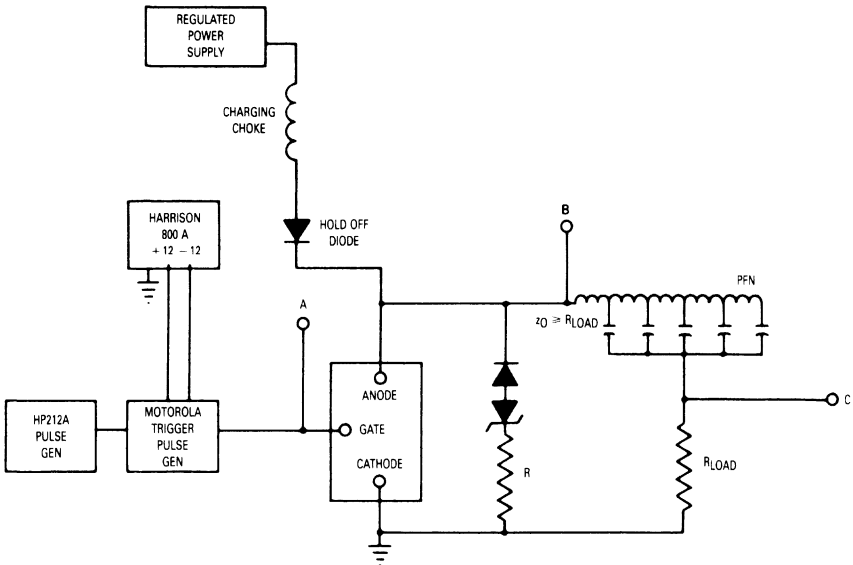


Figure 5.26. Modulator Circuit for SCR Tests

The above circuit setup shown in Figures 5.26 and 5.27 can be employed for such tests. A slight load to PFN mismatch is called for to generate an inverse voltage across the SCR at the termination of the output pulse. An SCR gate turn-off pulse is used. The recharge component is a charging choke, providing optimized conditions of reapplied voltage to the PFN (and across the SCR). Adequate heat sinking of the SCR should be provided.

PARALLEL CONNECTED SCRs

When an application requires current capability in excess of a single economical SCR, it can be worthwhile to consider paralleling two or more devices. To help deter-

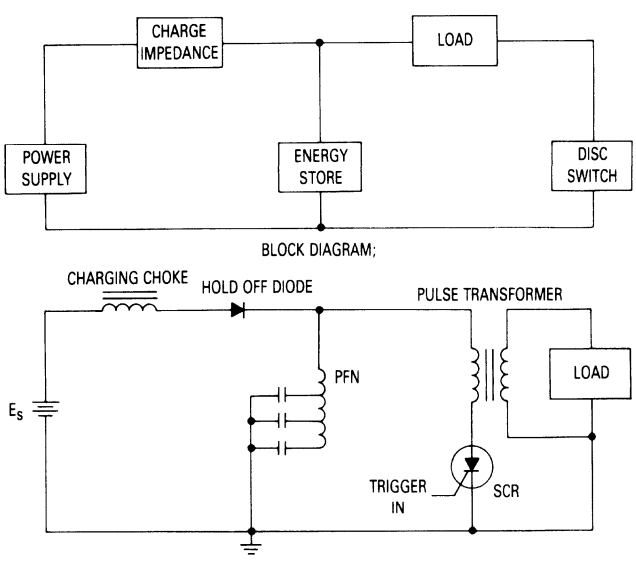


Figure 5.27. Radar Modulator, Resonant Line Type

mine if two or more SCRs in parallel are more cost effective than one high current SCR, some of the advantages and disadvantages are listed for parallel devices.

Advantages
1. Less expensive to purchase
2. Less expensive to mount
3. Less expensive to replace, in case of failure
4. Ease of mounting
5. Ease of isolation from sink

Disadvantages
1. Increased SCR count
2. Selected or matched devices
3. Increased component count
4. Greater R & D effort

There are several factors to keep in mind in paralleling and many are pertinent for single SCR operations as well.

GATE DRIVE

The required gate current (I_{GT}) amplitude can vary greatly and can depend upon SCR type and load being switched. As a general rule for parallel SCRs, I_{GT} should be at least two or three times the $I_{GT(MAX)}$ specification on the data sheet and ideally close to, but never exceeding, the maximum specified gate power dissipation or peak current. Adequate gate current is necessary for rapid turn-on of all the parallel SCRs and to ensure simultaneous turn-on without excessive current crowding across any of the individual die. The rise time of the gate drive pulse should be fast, ideally $\leq$ 100 ns. Each gate should be driven from a good current source and through its own resistor, even if transformer drive is used. Gate pulse width requirements vary but should be of sufficient width to ensure simultaneous turn-on and last well beyond the turn-on delay of the slowest device, as well as beyond the time required for latching of all devices. Ideally, gate current would flow for the entire conduction period to ensure latching under all operating conditions.

With low voltage switching, which includes conduction angles near 180° and near zero degrees, the gate drive requirements can be more critical and special emphasis may be required of gate pulse amplitude and width.

PARAMETER MATCHING

For reliable current sharing with parallel SCRs, there are certain device parameters that should be matched or held within close tolerances. The degree of matching required varies and can be affected by type of load (resistive, inductive, incandescent lamp or phase controlled loads) being switched.

The most common device parameters that can effect current sharing are:

1) t_d — turn-on delay time
2) t_r — turn-on rise time of anode current
3) $V_{A(MIN)}$ — minimum anode voltage at which device will turn on
4) Static on-state voltage and current
5) I_L — Latching current

The four parameters shown in Table 5.VI were measured with a curve tracer and are:

I_L, latching current; V_{TM}, on-state voltage; I_{GT} and V_{GT}, minimum gate current and voltage for turn on.

Of the four parameters, I_L and V_{TM} can greatly affect current sharing.

The latching current of each SCR is important at turn-on to ensure each device turns on and will stay on for the entire conduction period. On-state voltage determines how well the SCRs share current when cathode ballasting is not used.

Table 5.V gives turn-on delay time (t_d) and turn-on rise time (t_r) of the anode-cathode voltage and the minimum forward anode voltage for turn-on. These parameters were measured in the circuits shown in Figures 5.30 and 5.31. One SCR at a time was used in the circuit shown in Figure 5.30.

Turn-on delay on twenty-five SCRs was measured (only ten are shown in Table 5.V) and they could be from one or more production lots. The variation in t_d was slight and ranged from 35 to 44 ns but could vary considerably on other production lots and this possible variation in t_d would have to be considered in a parallel application.

Waveforms for minimum forward anode voltage for turn-on are shown in Figure 5.28. The trailing edge of the gate current pulse is phase delayed (R_3) so that the SCR is not turned on. The width of the gate current pulse is now increased (R_5) until the SCR turns on and the forward anode voltage switches to the on-state at about 0.73 V. This is the minimum voltage at which this SCR will turn on with the circuit conditions shown in Figure 5.28.

For dynamic turn-on current sharing, t_d, t_r and $V_{A(MIN)}$ are very important. As an example, with a high wattage incandescent lamp load, it is very important that the inrush current of the cold filament be equally shared by the parallel SCRs. The minimum anode voltage at which a device turns on is also very important. If one of the

Table 5.V. 2N6394 Turn-On Delay, Rise Time and Minimum Forward Anode Voltage For Turn-On

Device	Turn-On Delay and Rise Time Off-State Voltage = 8 V Peak R_L = 10 Ohms, $I_A \cong$ 6.5 A Peak I_G = 100 mA (PW = 100 μs) Conduction Angle 90 Degrees		Minimum Anode Voltage For Turn-On Off-State Voltage = 4 V Peak R_L = 0.5 Ohm I_A = 5A I_G = 100 mA
	$t_{d(ns)}$	$t_{r(\mu s)}$	(Volts)
1	35	0.80	0.70
2	38	0.95	0.81
3	45	1	0.75
4	44	1	0.75
5	44	0.90	0.75
6	43	0.85	0.75
7	38	1.30	0.75
8	38	1.25	0.70
9	38	1	0.75
10	37	0.82	0.70

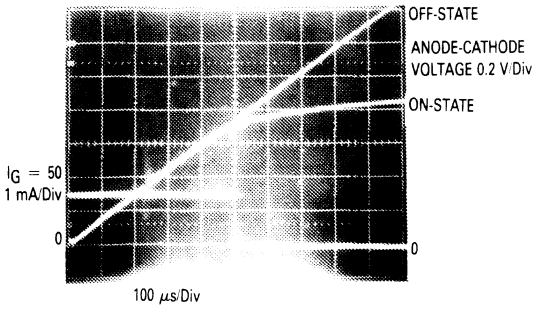


Figure 5.28. Minimum Anode Voltage For Turn-On Off-State Voltage = 4 V Peak, R_L = 0.5 Ohm, $I_A \approx$ 5 A, I_G = 75 mA

parallel devices turns on before the other devices and its on-state voltage is lower than the required minimum anode voltage for turn-on of the unfired devices, they therefore cannot turn on. This would overload the device which turned on, probably causing failure from overcurrent and excessive junction temperature.

Turn-off time — t_q is important in higher frequency applications which require the SCR to recover from the forward conduction period and be able to block the next cycle of forward voltage. Thus, t_q matching for high frequency operation can be as important as t_d, t_r and $V_{A(MIN)}$ matching for equal turn-on current sharing.

Due to the variable in t_q measurement, no further attempt will be made here to discuss this parameter and the reader is referred to Application Note AN914.

The need for on-state matching of current and voltage is important, especially in unforced current sharing circuits.

UNFORCED CURRENT SHARING

When operating parallel SCRs without forced current sharing, such as without cathode ballasting using resistors or inductors, it is very important that the device parameters be closely matched. This includes t_d, t_r, minimum forward anode voltage for turn-on and on-state voltage matching. The degree of matching determines the success of the circuit.

In circuits without ballasting, it is especially important that physical layout, mounting of devices and resistance paths be identical for good current sharing, even with on-state matched devices.

Figure 5.29 shows how anode current can vary on devices closely matched for on-state voltage (1, 3 and 4) and a mismatched device (2). Without resistance ballasting, the matched devices share peak current within one ampere and device 2 is passing only nine amps, seven amps lower than device 1. Table 5.VI shows the degree of match or mismatch of V_{TM} of the four SCRs.

With unforced current sharing (R_K = 0), there was a greater tendency for one device (1) to turn-on, preventing the others from turning on when low anode switching voltage (≤ 10 V rms) was tried. Table 5.V shows that the minimum anode voltage for turn-on is from 7 to 14% lower for device 1 than on 2, 3 and 4. Also, device 1 turn-on delay is 35 ns versus 38, 45 and 44 ns for devices 2, 3 and 4.

The tendency for device 1 to turn on, preventing the other three from turning on, is most probably due to its lower minimum anode voltage requirement and shorter turn on delay. The remedy would be closer matching of the minimum anode voltage for turn-on and driving the gates hard (but less than the gate power specifications) and increasing the width of the gate current pulse.

FORCED CURRENT SHARING

Cathode ballast elements can be used to help ensure good static on-state current sharing. Either inductors or resistors can be used and each has advantages and disadvantages. This section discusses resistive ballasting, but it should be kept in mind that the inductor method is usually better suited for the higher current levels. Although they are more expensive and difficult to design, there is less power loss with inductor ballasting as well as other benefits.

The degree of peak current sharing is shown in Figure 5.29 for four parallel 2N6394 SCRs using cathode resistor ballasting with an inductive anode load. With devices 1, 3 and 4, on-state voltage is matched within 10 mV at an anode current of 15 A (See Table 5.VI) and are within 1 A of each other in Figure 5.29, with cathode resistance (R_K) equal to zero. As R_K increases, the current sharing becomes even closer. The unmatched device 2, with a V_{TM} of 1.41 V (Table 5.VI), is not carrying its share of current (Figure 5.29) with R_K equal zero. As R_K increases, device 2 takes a greater share of the total current and with R_K around 0.25 ohm, the four SCRs are sharing peak current quite well. The value of R_K depends on how close the on-state voltage is matched on the SCRs and the degree of current sharing desired, as well as the permissible power dissipation in R_K.

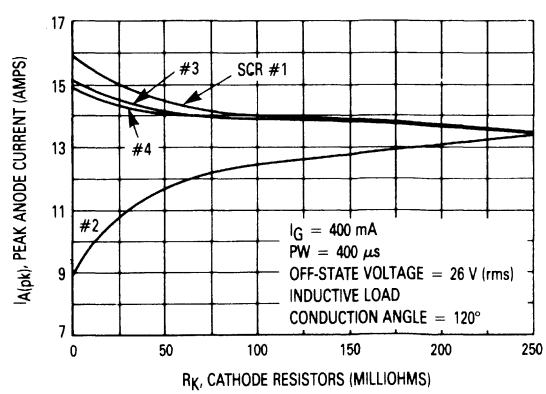


Figure 5.29. Effects Of Cathode Resistor On Anode Current Sharing

Table 5.VI. 2N6394 Parameters Measured On Curve Tracer, T_C = 25°C

Device #	I_L, Latching Current V_D = 12 Vdc I_G = 100 mA	V_{TM}, On-State Voltage I_A = 15 A PW = 300 μs	Minimum Gate Current & Voltage for Turn-On V_D = 12 Vdc, R_L = 140 Ω	
			I_{GT}	V_{GT}
1	13 mA	1.25 V	5.6 mA	0.615 V
2	27	1.41	8.8	0.679
3	28	1.26	12	0.658
4	23	1.26	9.6	0.649
5	23	1.28	9.4	0.659
6	23	1.26	9.6	0.645
7	18	1.25	7.1	0.690
8	19	1.25	7	0.687
9	19	1.25	8.4	0.694
10	16	1.25	6.9	0.679

LINE SYNCHRONIZED DRIVE CIRCUIT

Gate drive for phase control of the four parallel SCRs is accomplished with one complementary MOS hex gate, MC14572, and two bipolar transistors (Figure 5.30). This adjustable line-synchronized driver permits SCR conduction from near zero to 180 degrees. A Schmitt trigger clocks a delay monostable multivibrator that is followed by a pulse-width monostable multi-vibrator.

Line synchronization is achieved through the half-wave section of the secondary winding of the full-wave, center-tapped transformer (A). This winding also supplies power to the circuit through rectifiers D_1 and D_2.

The full-wave signal is clipped by diode D_5, referenced to a +15 volt supply, so that the input limit of the CMOS chip is not exceeded. The waveform is then shaped by the Schmitt trigger, which is composed of inverters U_{1-a} and U_{1-b}. A fast switching output signal B results.

The positive-going edge of this pulse is differentiated by the capacitive-resistive network of C_1 and R_2 and triggers the delay multivibrator that is composed of U_{1-c} and U_{1-d}. As a result, the normally high output is switched low. The trailing edge of this pulse (C) then triggers the following multivibrator, which is composed of NAND gate U_{1-e} and inverter U_{1-f}. The positive going output pulse (waveform D) of this multivibrator, whose width is set by potentiometer R_6, turns on transistors Q_1 and Q_2, which drives the gates of the four SCRs. Transistor Q_2 supplies about 400 mA drive current to each gate through 100 ohm resistors and has a rise time of ≤ 100 ns.

PARALLEL SCR CIRCUIT

The four SCRs are 2N6394s, housed in the TO-220 package, rated at 12 A rms, 50 V and are shown schematically

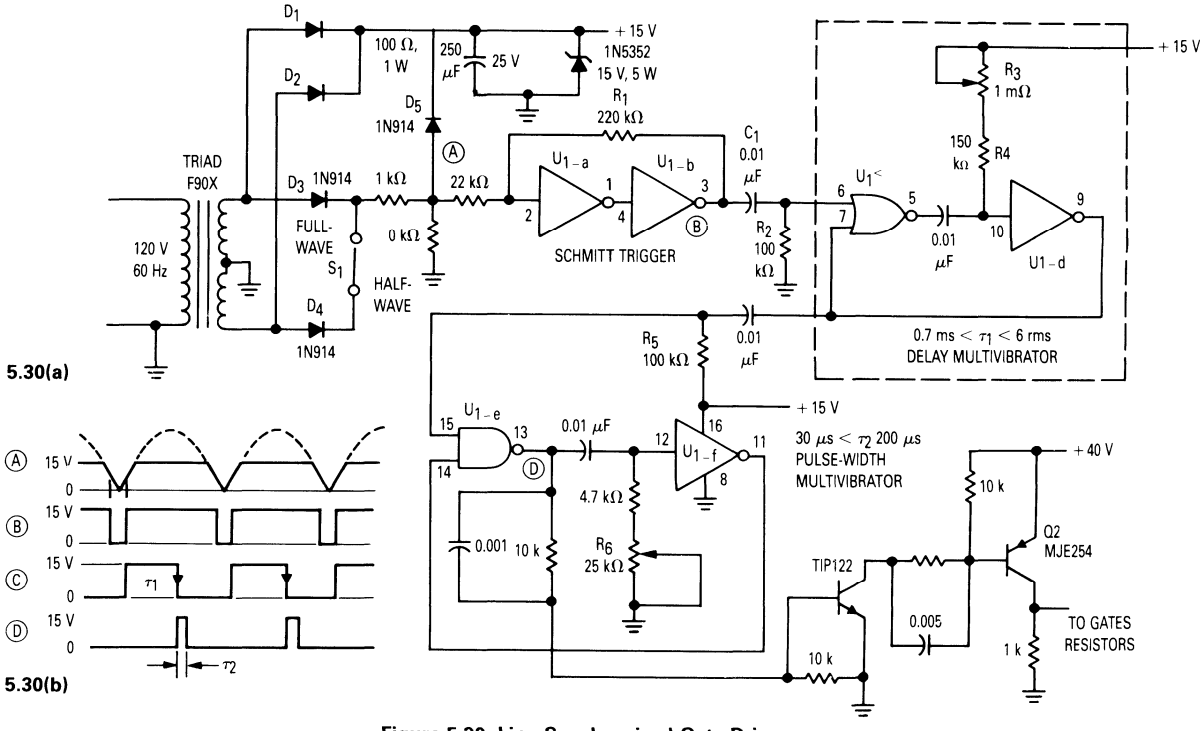


Figure 5.30. Line-Synchronized Gate Driver

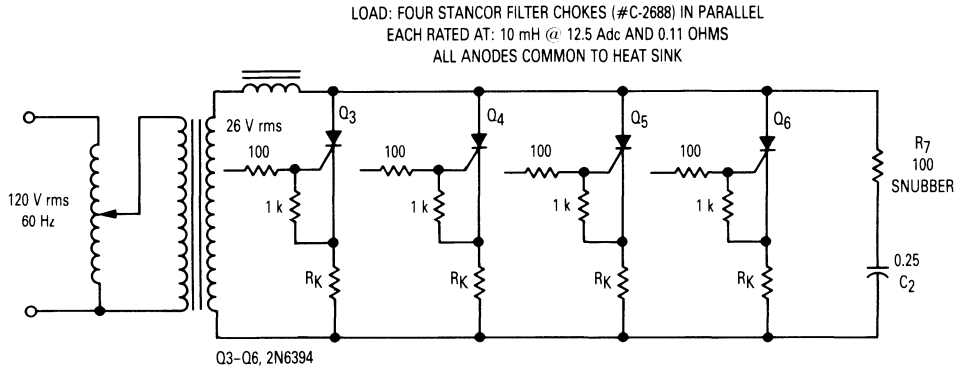


Figure 5.31. Parallel Thyristors

in Figure 5.31. Due to line power limitations, it was decided to use a voltage step down transformer and not try working directly from the 120 V line. Also, line isolation was desirable in an experiment of this type.

The step down transformer ratings were 120 V rms primary, 26 V rms secondary, rated at 100 A, and was used with a variable transformer for anode voltage adjustment. The inductive load consisted of four filter chokes in parallel (Stancor #C-2688 with each rated at 10 mH, 12.5 Adc and 0.11 ohm).

For good current sharing with parallel SCRs, symmetry in layout and mounting is of primary importance. The four SCRs were mounted on a natural finish aluminum heat sink and torqued to specification which is 8 inch pounds. Cathode leads and wiring were identical, and when used, the cathode resistors R_K were matched within 1%. An RC snubber network (R_7 and C_2) was connected across the anodes-cathodes to slow down the rate-of-rise of the off-state voltage, preventing unwanted turn-on.

CHARACTERIZING RFI SUPPRESSION IN THYRISTOR CIRCUITS

In order to understand the measures for suppression of EMI, characteristics of the interference must be explored first. To have interference at all, we must have a transmitter, or creator of interference, and a receiver, a device affected by the interference. Neither the transmitter nor the receiver need be related in any way to those circuits commonly referred to as radio-frequency circuits. Common transmitters are opening and closing of a switch or relay contacts, electric motors with commutators, all forms of electric arcs, and electronic circuits with rapidly changing voltages and currents. Receivers are generally electronic circuits, both low and high impedance which are sensitive to pulse or high frequency energy. Often the very circuits creating the interference are sensitive to similar interference from other circuits nearby or on the same power line.

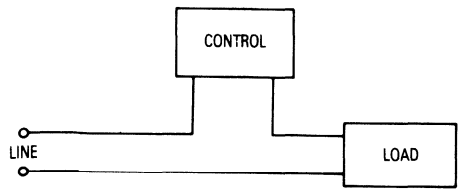
EMI can generally be separated into two categories — radiated and conducted. Radiated interference travels by way of electro-magnetic waves just as desirable RF energy does. Conducted interference travels on power, communications, or control wires. Although this separation and nomenclature might seem to indicate two neat little packages, independently controllable, such is not the case. The two are very often interdependent such that in some cases control of one form may completely eliminate the other. In any case, both interference forms must be considered when interference elimination steps are taken.

Phase control circuits using thyristors (SCRs, triacs, etc.) for controlling motor speed or resistive lighting and heating loads are particularly offensive in creating interference. They can completely obliterate most stations on any AM radio nearby and will play havoc with another control on the same power line. These controls are generally connected in one of the two ways shown in the block diagrams of Figure 5.32.

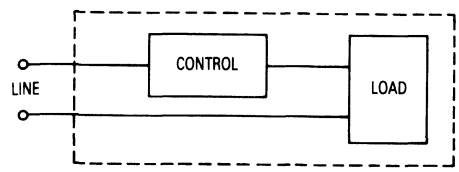
A common example of the connection of 5.32(a) is the wall mounted light dimmer controlling a ceiling mounted lamp. A motorized appliance with a built-in control such as a food mixer is an example of the connection shown in 5.32(b).

Figure 5.32(a) may be re-drawn as shown in Figure 5.33, illustrating the complete circuit for RF energy. The switch in the control box represents the thyristor, shown in its blocking state. In phase control operation, this switch is open at the beginning of each half cycle of the power line alternations. After a delay determined by the remainder of the control circuitry, the switch is closed and remains that way until the instantaneous current drops to zero. This switch is the source from which the RF energy flows down the power lines and through the various capacitors to ground.

If the load is passive, such as a lamp or a motor which does not generate interference, it may be considered as an impedance bypassed with the wire-to-wire capacitance of its leads. If it is another RF energy source, however, such as a motor with a commutator, it must be treated separately to reduce interference from that



(a). Separately Mounted Control



(b). Control and Load in the Same Enclosure

Figure 5.32. Block Diagrams of Control Connections

source. The power supply may be considered as dc since the interference pulse is extremely short (10 μs) compared to the period of the power line frequency (16 ms for 60 Hz). The inductance associated with the power source comes from two separate phenomena. First is the leakage impedance of the supply transformer, and second is the self-inductance of the wires between the power line transformer and the load.

One of the most difficult parameters to pin down in the system is the effect of grounding. Most industrial and commercial wiring and many homes use a grounded conduit system which provides excellent shielding of radiated energy emanating from the wiring. However, a large number of homes are being wired with two to three wire insulated cable without conduit. In three-wire systems, one wire is grounded independently of the power system even though one of the power lines is already grounded. The capacitances to ground shown in Figure 5.33 will be greatly affected by the type of grounding used. Of course, in any home appliance, filtering must be provided suitable for all three different systems.

Before the switch in the control is closed, the system is in a steady-state condition with the upper line of the power line at the system voltage and the bottom line and the load at ground potential. When the switch is closed, the upper line potential instantaneously falls due to the line and source inductance, then it rises back to its original value as the line inductance is charged. While the upper line is rising, the line from the control to the load also rises in potential. The effect of both of these lines increasing in potential together causes an electro-static field change which radiates energy. In addition, any other loads connected across the power lines at point A, for example, would be affected by a temporary loss of voltage created by the closing of the switch and by the line and source inductance. This is a form of conducted interference.

A second form of radiated interference is inductive coupling in which the power line and ground form a one-turn primary of an air core transformer. In this mode, an unbalanced transient current flows down the power lines with the difference current flowing to ground through the various capacitive paths available. The secondary is the radio antenna or the circuit being affected. This type of interference is a problem only when the receiver is within about one wavelength of the transmitter at the offending frequency.

Radiated interference from the control circuit proper is of little consequence due to several factors. The lead lengths in general are so short compared to the wavelengths in question that they make extremely poor antenna. In addition, most of these control circuits are mounted in metal enclosures which provide shielding for radiated energy generated within the control circuitry.

A steel box will absorb radiated energy at 150 kHz such that any signal inside the box is reduced 12.9 dB per mil of thickness of the box. In other words, a 1/16 inch thick steel box will attenuate radiated interference by over 800 dB! A similar aluminum box will attenuate 1 dB per mil or 62.5 dB total. Thus, even in an aluminum box, the control circuitry will radiate very little energy.

Both forms of radiated interference which are a problem are a result of conducted interference on the power lines which is in turn caused by a rapid rise in current. Thus, if this current rise is slowed, all forms of interference will be reduced.

RFI SOLUTIONS

Since the switch in Figure 5.33, when it closes, provides a very low impedance path, a capacitor in parallel with it will show little benefit in slowing down the rise of current. The capacitor will be charged to a voltage deter-

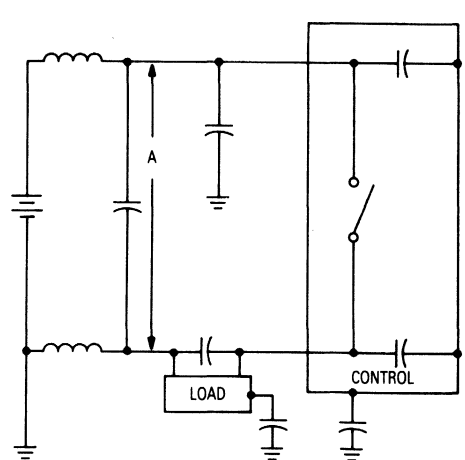


Figure 5.33. RF Circuit for Figure 5.32(a)

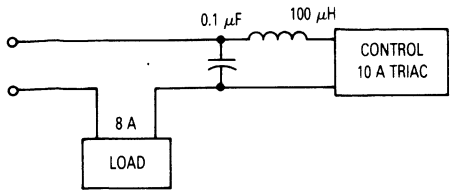


Figure 5.34. One Possible EMI Reduction Circuit

1

mined by the circuit constants and the phase angle of the line voltage just before the switch closes. When the switch closes, the capacitor will discharge quickly, its current limited only by its own resistance and the resistance of the switch. However, a series inductor will slow down the current rise in the load and thus reduce the voltage transient on all lines. A capacitor connected as shown in Figure 5.34 will also help slow down the current rise since the inductor will now limit the current out of the capacitor. Thus, the capacitor voltage will drop slowly and correspondingly the load voltage will increase slowly.

Although this circuit will be effective in many cases, the filter is unbalanced, providing an RF current path through the capacitances to ground. It has, therefore, been found advantageous to divide the inductor into two parts and to put half in each line to the control. Figure 5.35 illustrates this circuit showing the polarity marks of two coils which are wound on the same core.

A capacitor at point A will help reduce interference further. This circuit is particularly effective when used with the connection of Figure 5.32(b) where the load is not always on the grounded side of the power line. In this case, the two halves of the inductor would be located in the power line leads, between the controlled circuit and the power source.

Where the control circuit is sensitive to fast rising line transients, a capacitor at point B will do much to eliminate this problem. The capacitor must charge through the impedance of the inductor, thus limiting the rate of voltage change (dv/dt) applied to the thyristor while it is in the blocking state.

DESIGN CRITERIA

Design equations for the split inductor have been developed based on parameters which should be known before attempting a design. The most difficult to determine is t_r, the minimum allowable current rise time which will not cause objectionable interference. The value of this parameter must be determined empirically in each situation if complete interference reduction is needed. Motorola has conducted extensive tests using an AM radio as a receiver and a 600 Watt thyristor lamp dimmer as a transmitter. A rate of about 0.35 Amp per μs seems to be effective in eliminating objectionable interference as well as materially reducing false triggering of the thyristor due to line transients. The value of t_r may be calculated by dividing the peak current anticipated by the allowable rate of current rise.

Ferrite core inductors have proved to be the most practical physical configuration. Most ferrites are effective; those with highest permeability and saturation flux density are preferred. Those specifically designed as high frequency types are not necessarily desirable.

Laminated iron cores may also be used; however, they require a capacitor at point A in Figure 5.35 to be at all effective. At these switching speeds, the iron requires considerable current in the windings before any flux change can take place. We have found currents rising to half their peak value in less than one μs before the inductance begins to slow down the rise. The capacitor supplies this current for the short period without dropping in voltage, thus eliminating the pulse on the power line.

Once a core material has been selected, wire size is the next decision in the design problems. Due to the small number of turns involved (generally a single layer) smaller sizes than normally used in transformers may be chosen safely. Generally, 500 to 800 circular mills per ampere is acceptable, depending on the enclosure of the filter and the maximum ambient temperature expected.

An idea of the size of the core needed may be determined from the equation:

$$(1) \quad A_c A_w = \frac{26\, A_{wire}\, E_{rms}\, t_r}{B_{MAX}}$$

where:

A_c = the effective cross-sectional area of the core in in^2
A_w = available core window area in in^2
A_{wire} = wire cross section in circular mils
B_{MAX} = core saturation flux density in gauss
t_r = allowable current rise time in seconds
E_{rms} = line voltage

(A factor of 3 has been included in this equation to allow for winding space factor.) Once a tentative core selection has been made, the number of turns required may be found from the equation:

$$(2) \quad N = \frac{11\, E_{rms}\, t_r \times 10^6}{B_{MAX} A_c}$$

where:

N = the total number of turns on the core

The next step is to check how well the required number of turns will fit onto the core. If the fit is satisfactory, the core design is complete; if not, some trade-offs will have to be made.

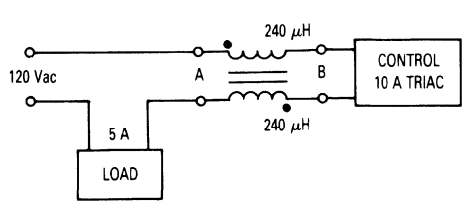


Figure 5.35. Split Inductor Circuit

In most cases, the inductor as designed at this point will have far too much inductance. It will support the entire peak line voltage for the time selected as t_r and will then saturate quickly, giving much too fast a current rise. The required inductance should be calculated from the allowable rise time and load resistance, making the rise time equal to two time constants. Thus:

$$\frac{2L}{R} = t_r \quad \text{or} \quad L = \frac{R\,t_r}{2} \tag{3}$$

Paper or other insulating material should be inserted between the core halves to obtain the required inductance by the equation:

$$l_g = \frac{3.19\,N^2\,A_c \times 10^{-8}}{L} - \frac{l_c}{\mu} \tag{4}$$

where:

l_g = total length of air gap in inches
μ = effective ac permeability of the core material at the power line frequency
l_c = effective magnetic path length of the core in inches
A_c = effective cross sectional area of the core in square inches
L = inductance in henries

DESIGN EXAMPLE

Consider a 600 watt, 120 Volt lamp dimmer using a Motorola 2N6148 triac. Line current is $\frac{600}{120} = 5$ amperes.

#16 wire will provide about 516 circular mils per ampere.

For core material, type 3C5 of Ferroxcube Corporation of America, Saugerties, New York, has a high B_{max} and μ. The company specifies B_{MAX} = 3800 gauss and μ = 1900 for material.

As was previously mentioned, a current rise rate of about 0.35 ampere per μs has been found to be acceptable for interference problems with ac-dc radios in most wiring situations. With 5 amperes rms, 7 amperes peak,

$$t_r = \frac{7}{0.35} = 20\ \mu s$$

Then by equation (1):

$$A_cA_w = \frac{26 \times 2580 \times 120 \times 20 \times 10^{-6}}{3800 \text{ gauss}} = 0.044$$

Core part number 1F30 of the same company in a U-1 configuration has an A_cA_w product of 0.0386, which should be close enough.

$$N = \frac{10.93 \times 120 \times 20 \times 10^{-6} \times 10^6}{3800 \times 0.137} = 42 \text{ turns}$$

Two coils of 21 turns each should be wound on either one or two legs and be connected as shown in Figure 5.35.

The required inductance of the coil is found from equation (3).

$$L = \frac{R\,t_r}{2} = \frac{E_{rated}}{I_{rated}} \times \frac{t_r}{2} = \frac{120}{5} \times \frac{20}{2} \times 10^{-6} = 240 \times 10^{-6}$$

$$L = 240\ \mu H$$

To obtain this inductance, the air gap should be

$$l_g = \frac{3.19 \times 42^2 \times 0.137 \times 10^{-8}}{240 \times 10^{-6}} - \frac{3.33}{1900} = 0.0321 - 0.00175$$

$$l_g = 0.03035$$

Thus, 15 mils of insulating material in each leg will provide the necessary inductance.

If a problem still exists with false triggering of the thyristor due to conducted interference, a capacitor at point B in Figure 5.35 will probably remedy the situation.

CHAPTER 6
APPLICATIONS

1

Because they are reliable solid state switches, thyristors have many applications, especially as controls.

One of the most common uses for thyristors is to control ac loads such as electric motors. This can be done either by controlling the part of each ac cycle when the circuit conducts current (phase control) or by controlling the number of cycles per time period when current is conducted (cycle control).

In addition, thyristors can serve as the basis of relaxation oscillators for timers and other applications. Most of the devices covered in this book have control applications.

PHASE CONTROL WITH THYRISTORS

The most common method of electronic ac power control is called *phase control.* Figure 6.1 illustrates this concept. During the first portion of each half-cycle of the ac sine wave, an electronic switch is opened to prevent the current flow. At some specific phase angle, α, this switch is closed to allow the full line voltage to be applied to the load for the remainder of that half-cycle. Varying α will control the portion of the total sine wave that is applied to the load (shaded area), and thereby regulate the power flow to the load.

The simplest circuit for accomplishing phase control is shown in Figure 6.2. The electronic switch in this case is a triac (Q) which can be turned on by a small current pulse to its gate. The TRIAC turns off automatically when the current through it passes through zero. In the circuit shown, capacitor C_T is charged during each half-cycle by the current flowing through resistor R_T and the load. The fact that the load is in series with R_T during this portion of the cycle is of little consequence since the resistance of R_T is many times greater than that of the load. When the voltage across C_T reaches the breakdown voltage of the DIAC bilateral trigger (D), the energy stored in capacitor C_T is released. This energy produces a current pulse in the DIAC, which flows through the gate of the TRIAC and turns it on. Since both the DIAC and the TRIAC are bidirectional devices, the values of R_T and C_T will determine the phase angle at which the TRIAC will be triggered in both the positive and negative half-cycles of the ac sine wave.

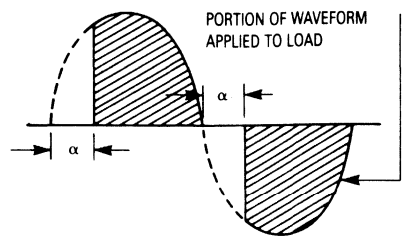


Figure 6.1. Phase Control of AC Waveform

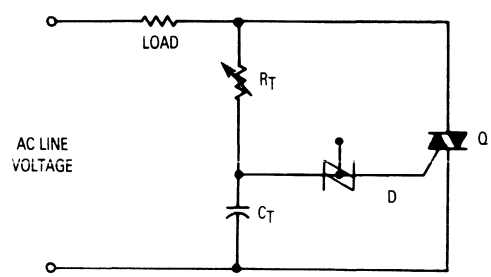


Figure 6.2. Simplest Circuit for Phase Control

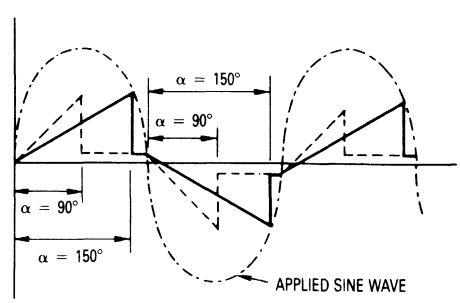


Figure 6.3. Waveforms of Capacitor Voltage at Two Phase Angles

The waveform of the voltage across the capacitor for two typical control conditions (α = 90° and 150°) is shown in Figure 6.3. If a silicon controlled rectifier is used in this

circuit in place of the TRIAC, only one half-cycle of the waveform will be controlled. The other half-cycle will be blocked, resulting in a pulsing dc output whose average value can be varied by adjusting R_T.

CONTROL OF INDUCTION MOTORS

Shaded-pole motors driving low-starting-torque loads such as fans and blowers may readily be controlled using any of the previously described full-wave circuits. One needs only to substitute the winding of the shaded-pole motor for the load resistor shown in the circuit diagrams.

Constant-torque loads or high-starting-torque loads are difficult, if not impossible, to control using the voltage controls described here. Figure 6.4 shows the effect of varying voltage on the speed-torque curve of a typical shaded-pole motor. A typical fan-load curve and a constant-torque-load curve have been superimposed upon this graph. It is not difficult to see that the torque developed by the motor is equal to the load torque at two different points on the constant-torque-load curve, giving two points of equilibrium and thus an ambiguity to the speed control. The equilibrium point at the lower speed is a condition of high motor current because of low counter EMF and would result in burnout of the motor winding if the motor were left in this condition for any length of time. By contrast, the fan speed-torque curve crosses each of the motor speed-torque curves at only one point, therefore causing no ambiguities. In addition, the low-speed point is one of low voltage well within the motor winding's current-carrying capabilities.

Permanent-split-capacitor motors can also be controlled by any of these circuits, but more effective control is achieved if the motor is connected as shown in Figure 6.5. Here only the main winding is controlled and the capacitor winding is continuously connected to the entire ac line voltage. This connection maintains the phase shift between the windings, which is lost if the capacitor phase is also controlled. Figure 6.6(a) shows the effect of voltage on the speed-torque characteristics of this motor and a superimposed fan-load curve.

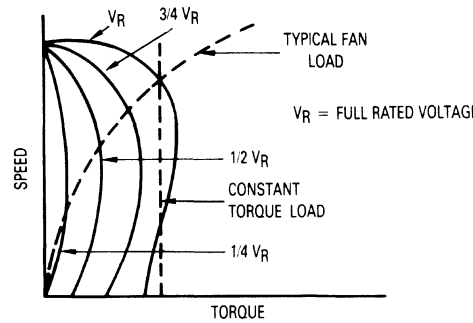


Figure 6.4. Characteristics of Shaded-Pole Motors at Several Voltages

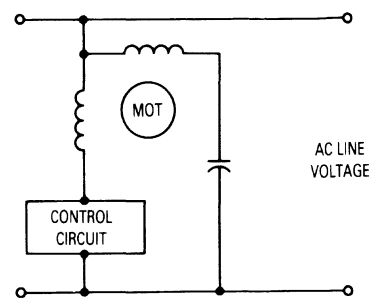
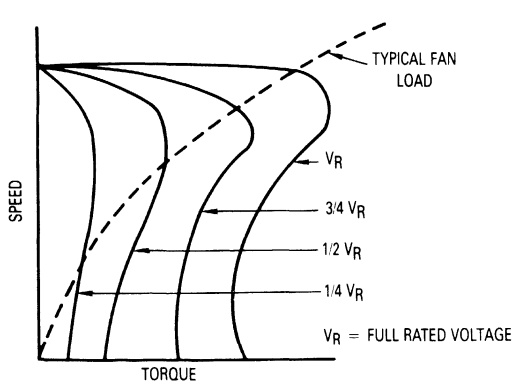
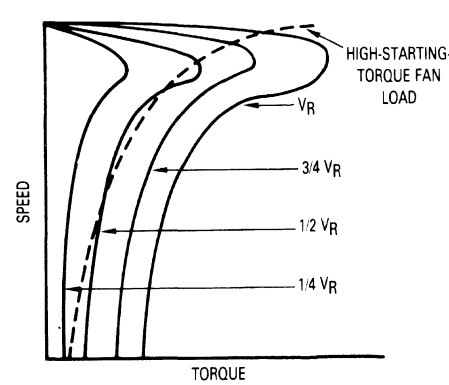


Figure 6.5. Connection Diagram for Permanent-Split-Capacitor Motors

Not all induction motors of either the shaded-pole or the permanent-split-capacitor types can be controlled effectively using these techniques, even with the proper loads. Motors designed for the highest efficiencies and, therefore, low slip also have a very low starting torque and may, under certain conditions, have a speed-torque



(a). High-Starting-Torque Motor



(b). High-Efficiency Motor

Figure 6.6. Speed-Torque Curves for Permanent-Split-Capacitor Motors at Various Applied Voltages

characteristic that could be crossed twice by a specific fan-load speed-torque characteristic. Figure 6.6(b) shows motor torque-speed characteristic curves upon which has been superimposed the curve of a fan with high starting torque. It is therefore desirable to use a motor whose squirrel-cage rotor is designed for medium-to-high impedance levels and, therefore, has a high starting torque. The slight loss in efficiency of such a motor at full rated speed and load is a small price to pay for the advantage of speed control.

A unique circuit for use with *capacitor-start motors* in explosive or highly corrosive atmospheres, in which the arcing or the corrosion of switch contacts is severe and undesirable, is shown in Figure 6.7. Resistor R1 is connected in series with the main running winding and is of such a resistance that the voltage drop under normal full-load conditions is approximately 0.2 V peak. Since starting currents on these motors are quite high, this peak voltage drop will exceed 1 V during starting conditions, triggering the TRIAC, which will cause current to flow in the capacitor winding. When full speed is reached, the current through the main winding will decrease to about 0.2 V, which is insufficient to trigger the TRIAC — thus the capacitor winding will no longer be energized. Resistor R2 and capacitor C2 form a dv/dt suppression network; this prevents the TRIAC from turning on due to line transients and inductive switching transients.

CONTROL OF UNIVERSAL MOTORS

Any of the half-wave or full-wave controls described previously can be used to control universal motors. *Non-feedback,* manual controls, such as those shown in Figure 6.2, are simple and inexpensive, but they provide very little torque at low speeds. A comparison of typical speed-torque curves using a control of this type with those of *feedback* control is shown in Figure 6.8.

These motors have some unique characteristics which allow their speed to be controlled very easily and efficiently with a feedback circuit such as that shown in Figure 6.9. This circuit provides phase-controlled half-wave power to the motor; that is, on the negative half-cycle, the SCR blocks current flow in the negative direction causing the motor to be driven by a pulsating direct current whose amplitude is dependent on the phase control of the SCR.

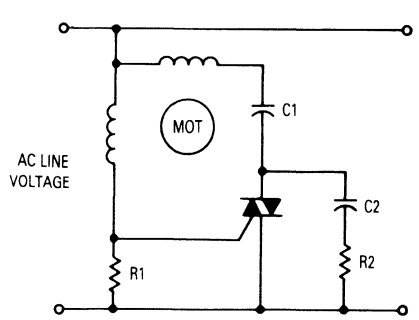


Figure 6.7. Circuit Diagram for Capacitor-Start Motor

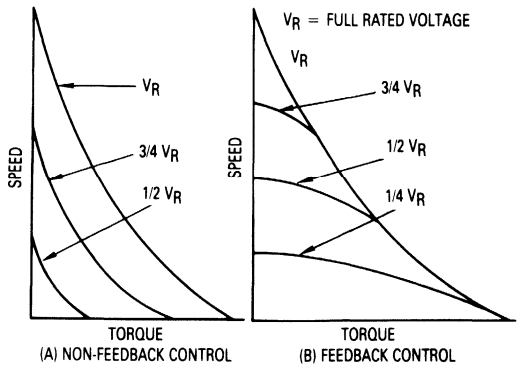


Figure 6.8. Comparison of Feedback Control with Non-Feedback Control

The theory of operation of this control circuit is not at all difficult to understand. Assuming that the motor has been running, the voltage at point A in the circuit diagram must be larger than the forward drop of Diode D1, the gate-to-cathode drop of the SCR, and the EMF generated by the residual MMF in the motor, to get sufficient current flow to trigger the SCR.

The waveform at point A (V_A) for one positive half-cycle is shown in 6.9(b), along with the voltage levels of the SCR gate (V_{SCR}), the diode drop (V_D), and the motor-generated EMF (V_M). The phase angle (α) at which the SCR would trigger is shown by the vertical dotted line. Should the motor for any reason speed up so that the generated motor voltage would increase, the trigger point would move upward and to the right along the curve so that the SCR would trigger later in the half-cycle and thus provide less power to the motor, causing it to slow down again.

Similarly, if the motor speed decreased, the trigger point would move to the left and down the curve, causing the TRIAC to trigger earlier in the half-cycle providing more power to the motor, thereby speeding it up.

Resistors R1, R2, and R3, along with diode D2 and capacitor C1 form the ramp-generator section of the circuit. Capacitor C1 is charged by the voltage divider R1, R2, and R3 during the positive half-cycle. Diode D2 prevents negative current flow during the negative half-cycle, therefore C1 discharges through only R2 and R3 during that half-cycle. Adjustment of R3 controls the amount by which C1 discharges during the negative half-cycle. Because the resistance of R1 is very much larger than the ac impedance of capacitor C1, the voltage waveform on C1 approaches that of a perfect cosine wave with a dc component. As potentiometer R2 is varied, both the dc and the ac voltages are divided, giving a family of curves as shown in 6.9(c).

The gain of the system, that is, the ratio of the change of effective SCR output voltage to the change in generator

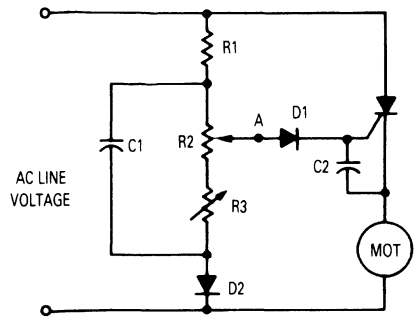
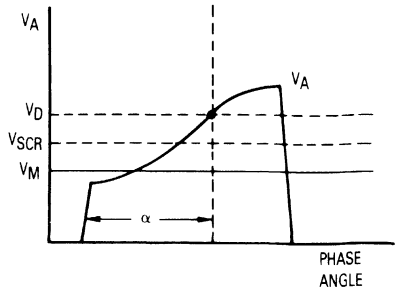
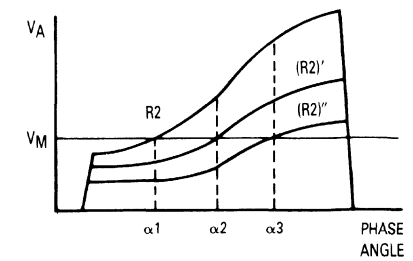


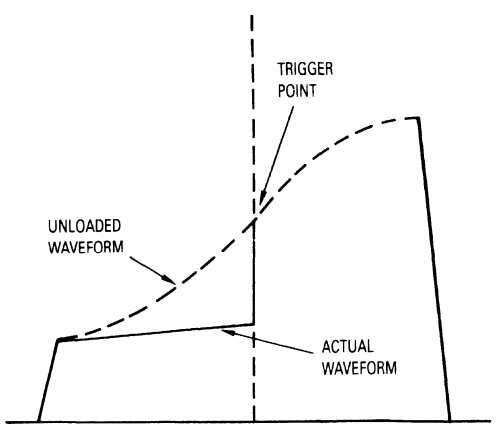
Figure 6.9 (a). Speed-Control Scheme for Universal Motors



(b). Waveform for One Positive Half-Cycle Circuit



(c). Voltage Waveform at Point "A" for Three Settings of Potentiometer R2



(d). Point "A" Voltage with Excessive Resistance R1

EMF, is considerably greater at low speed settings than it is at high speed settings. This high gain coupled with a motor with a very low residual EMF will cause a condition sometimes known as cycle skipping. In this mode of operation, the motor speed is controlled by skipping entire cycles or groups of cycles, then triggering one or two cycles early in the period to compensate for the loss in speed. Loading the motor would eliminate this condition; however, the undesirable sound and vibration of the motor necessitate that this condition be eliminated. This can be done in two ways.

The first method is used if the motor design is fixed and cannot be changed. In this case, the impedance level of the voltage divider R1, R2, and R3 can be lowered so that C1 will charge more rapidly, thus increasing the slope of the ramp and lowering the system gain. The second method, which will provide an overall benefit in improved circuit performance, involves a redesign of the motor so that the residual EMF becomes greater. In general, this means using a lower grade of magnetic steel for the laminations. As a matter of fact, some people have found that ordinary cold-rolled steel used as rotor laminations makes a motor ideally suited for this type of electronic control.

Another common problem encountered with this circuit is that of thermal runaway. With the speed control set at low or medium speed, at high ambient temperatures the speed may increase uncontrollably to its maximum value. This phenomenon is caused by an excessive impedance in the voltage-divider string for the SCR being triggered. If the voltage-divider current is too low, current will flow into the gate of the SCR without turning it on, causing the waveform at point A to be as shown in 6.9(d). The flat portion of the waveform in the early part of the half-cycle is caused by the SCR gate current loading the voltage divider before the SCR is triggered. After the SCR is triggered, diode D1 is back-biased and a load is no longer on the voltage divider so that it jumps up to its unloaded voltage. As the ambient temperature increases, the SCR becomes more sensitive, thereby requiring less gate current to trigger, and is triggered earlier in the half-cycle. This early triggering causes increased current in the SCR, thereby heating the junction still further and increasing still further the sensitivity of the SCR until maximum speed has been reached.

The solutions to this problem are the use of the most sensitive SCR practical and a voltage divider network of sufficiently low impedance. As a rough rule of thumb, the average current through the voltage divider during the positive half-cycle should be approximately three times the current necessary to trigger the lowest-

sensitivity (highest gate current) SCR being used.

In addition to the type of steel used in the motor laminations, consideration should also be given to the design of motors used in this half-wave speed control. Since the maximum rms voltage available to the motor under half-wave conditions is 85 V, the motor should be designed for use at that voltage to obtain maximum speed. However, U.L. requirements state that semiconductor devices used in appliance control systems must be able to be short-circuited without causing danger. Many designers have found it advantageous, therefore, to use 115 V motors with this system and provide a switch to apply full-wave voltage to the motor for high-speed operation. Figure 6.10 shows the proper connection for this switch. If one were to simply short-circuit the SCR for full-speed operation, a problem could arise. If the motor were operating at full speed with the switch closed, and the switch were then opened during the negative half-cycle, the current flowing in the inductive field of the motor could then break down the SCR in the negative direction and destroy the control. With the circuit as shown, the energy stored in the field of the motor is dissipated in the arc of the switch before the SCR is connected into the circuit.

CONTROL OF PERMANENT-MAGNET MOTORS

As a result of recent developments in ceramic permanent-magnet materials that can be easily molded into complex shapes at low cost, the permanent-magnet motor has become increasingly attractive as an appliance component. Electronic control of this type of motor can be easily achieved using techniques similar to those just described for the universal motor. Figure 6.11 is a circuit diagram of a control system that we have developed and tested successfully to control permanent-magnet motors presently being used in blenders. Potentiometer R3 and diode D1 form a dc charging path for capacitor C1; variable resistor R1 and resistor R2 form an ac charging path which creates the ramp voltage on the capacitor. Resistor R4 and diode D2 serve to isolate the motor control circuit from the ramp generator during the positive and negative half-cycles, respectively.

A small amount of cycle skipping can be experienced at low speeds using this control, but not enough to necessitate further development work. Since the voltage generated during off time is very high, the thermal runaway problem does not appear at all. Typical speed-torque curves for motors of this type are shown in Figure 6.12.

MOTOR SPEED CONTROL WITH FEEDBACK

While many motor speed control circuits have used SCRs, the TRIAC has not been very popular in this application. At first glance, it would appear that the TRIAC would be perfect for speed control because of its bilateral characteristics. There are a couple of reasons why this is not true. The major difficulty is the TRIAC's dv/dt characteristic. Another reason is the difficulty of obtaining a feedback signal because of the TRIAC's bilateral nature.

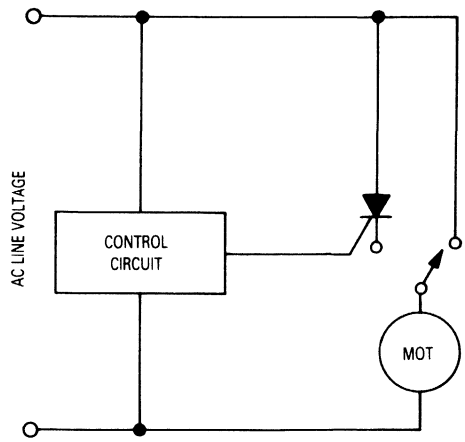


Figure 6.10. Switching Scheme for Full-Wave Operation

While the TRIAC has its disadvantages, it does offer some advantages. In a SCR speed control either two SCRs must be used, or the line voltage must be full-wave rectified using relatively high current rectifiers, or the control must be limited to half-wave. The TRIAC eliminates all these difficulties. By using a TRIAC the part count, package size, and cost can be reduced. Figure 6.13 shows a TRIAC motor speed control circuit that derives its feedback from the load current and does not require separate connections to the motor field and armature windings. Therefore, this circuit can be conveniently built into an appliance or used as a separate control.

The circuit operates as follows: When the TRIAC conducts, the normal line voltage, less the drop across the TRIAC and resistor R5, is applied to the motor. By delaying the firing of the TRIAC until a later portion of the cycle, the rms voltage applied to the motor is reduced and its speed is reduced proportionally. The use of feedback maintains torque at reduced speeds.

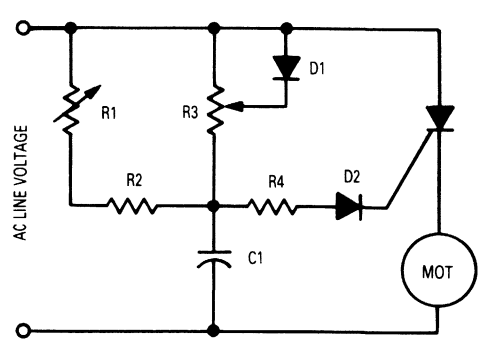


Figure 6.11. Circuit Diagram for Controlling Permanent-Magnet Motors

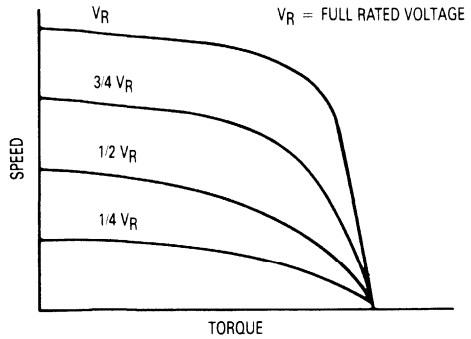


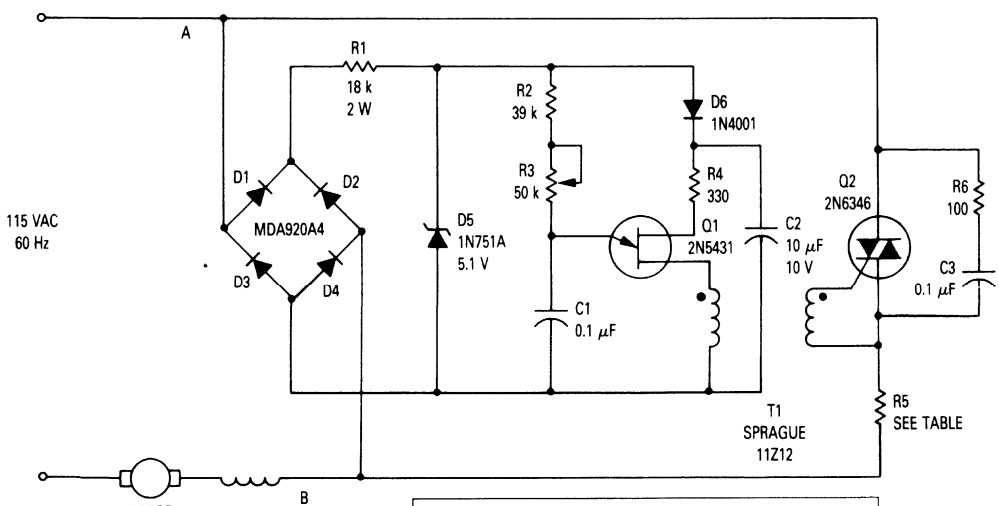
Figure 6.12. Speed-Torque Characteristic of Permanent-Magnet Motors at Various Applied Voltages

Diodes D1 through D4 form a bridge which applies full-wave rectified voltage to the phase-control circuit. Phase control of the TRIAC is obtained by the charging of capacitor C1 through resistors R2 and R3 from the voltage level established by zener diode D5. When C1 charges to the firing voltage of unijunction transistor Q1, the TRIAC is triggered through transformer T1. C1 discharges through the emitter of Q1. While the TRIAC is conducting, the voltage drop between points A and B falls below the breakdown voltage of D5. Therefore, during the conduction period, the voltage on C1 is determined by the voltage drop from A to B and by resistors R1, R2, and R3. Since the voltage between A and B is a function of motor current due to resistor R5, C1 is charged during the conduction period to a value which is proportional to the motor current. The value of R5 is chosen so that C1 cannot charge to a high enough voltage to fire Q1 during the conduction period. However, the amount of charging required to fire Q1 has been decreased by an amount proportional to the motor current. Therefore, the firing angle at which Q1 will fire has been advanced in proportion to the motor current. As the motor is loaded and draws more current, the firing angle of Q1 is advanced even more, causing a proportionate increase in the rms voltage applied to the motor, and a consequent increase in its available torque.

Since the firing voltage of Q1 depends on the voltage from base one to base two, it is necessary to support the base two voltage during the conduction portion of the cycle to prevent the feedback voltage from firing Q1. D6 and C2 perform this function.

Because the motor is an inductive load, it is necessary to limit the commutation dv/dt for reliable circuit operation. R6 and C3 perform this function.

Nominal values for R5 can be obtained from the table or they can be calculated from the equation given. Exact values for R5 depend somewhat on the motor characteristics. Therefore, it is suggested that R5 be an adjust-



NOMINAL R5 VALUES			
Motor Rating (Amperes)	R5 OHMS	R5 Watts	$R5 = \frac{2}{I_M}$
2	1	5	
3	0.67	10	I_M = Max. Rated Motor Current (rms)
6.5	0.32	15	

Figure 6.13. Motor Speed Control with Feedback

able wirewound resistor which can be calibrated in terms of motor current, and the speed control can be adapted to many different motors. If the value of R5 is too high, feedback will be excessive and surging or loss of control will result. If the value is too low, a loss of torque will result. The maximum motor current flows through R5, and its wattage must be determined accordingly.

This circuit has been operated successfully with 2 and 3 ampere 1/4-inch drills and has satisfactorily controlled motor speeds down to 1/3 or less of maximum speed with good torque characteristics.

CONSTANT SPEED MOTOR CONTROL USING TACHOMETER FEEDBACK

Tachometer feedback sensing rotor speed provides excellent performance with electric motors. The principal advantages to be gained from tachometer feedback are the ability to apply feedback control to shaded-pole motors, and better brush life in universal motors used in feedback circuits. This latter advantage results from the use of full-wave rather than half-wave control, reducing the peak currents for similar power levels.

THE TACHOMETER

The heart of this system is, of course, the speed-sensing tachometer itself. Economy being one of the principal goals of the design, it was decided to use a simple magnetic tachometer incorporating the existing motor fan as an integral part of the magnetic circuit. The generator consists of a coil wound on a permanent magnet which is placed so that the moving fan blades provide a magnetic path of varying reluctance as they move past the poles of the magnet. Several possible configurations of the magnetic system are shown in Figure 6.14.

Flux in a magnetic circuit can be found from the "magnetic Ohm's law":

$$\phi = \frac{MMF}{R},$$

where ϕ = the flux,

MMF = the magnetomotive force (strength of the magnet), and

R = the reluctance of the magnetic path.

Assuming the MMF of the permanent magnet to be constant, it is readily apparent that variations in reluctance will directly affect the flux. The steel fan blades provide a low-reluctance path for the flux once it crosses the air gap between them and the poles of the magnet. If the magnet used has a horseshoe or U shape, and is placed so that adjacent fan blades are directly opposite each pole in one position of the motor armature, the magnetic path will be of relatively low reluctance; then as the motor turns the reluctance will increase until one fan blade is precisely centered between the poles of the magnet. As rotation continues, the reluctance will then alternately increase and decrease as the fan blades pass the poles of the magnet. If a bar- or L-shaped magnet is used so that one pole is close to the shaft or the frame of the motor and the other is near the fan blades, the magnetic path reluctance will vary as each blade passes the magnet pole near the fan. In either case the varying reluctance causes variations in the circuit flux and a voltage is generated in the coil wound around the magnet. The voltage is given by the equation:

$$e = -N \frac{d\phi}{dt} \times 10^{-8},$$

where e = the coil voltage in volts,

N = the number of turns in the coil, and

$\frac{d\phi}{dt}$ = the rate of change of flux in lines per second.

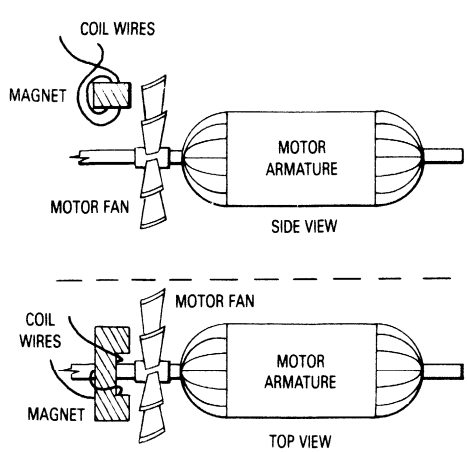
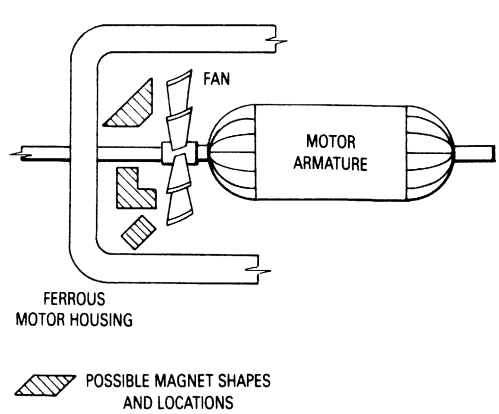


Figure 6.14(a). Locations for Magnetic Sensing Tachometer Generator Using a Horseshoe Magnet



(b). Locations for Magnetic Sensing Tachometer Generator Using an "L" or Bar Magnet

In a practical case, a typical small horseshoe magnet wound with 1000 turns of wire generated a voltage of about 0.5 volts/1000 rpm when mounted in a blender.

Since both generated voltage and frequency are directly proportional to the motor speed, either parameter can be used as the feedback signal. However, circuits using voltage sensing are less complex and therefore less expensive. Only that system will be discussed here.

THE ELECTRONICS

In one basic circuit, which is shown in Figure 6.15, the generator output is rectified by rectifier D1, then filtered and applied between the positive supply voltage and the base of the detector transistor Q1. This provides a negative voltage which reduces the base-voltage on Q1 when the speed increases.

The emitter of the detector transistor is connected to a voltage divider which is adjusted to the desired tachometer output voltage. In normal operation, if the tachometer voltage is less than desired, the detector transistor, Q1, is turned on by current through R1 into its base. Q1 then turns on Q2 which causes the timing capacitor for unijunction transistor Q3 to charge quickly. Standard unijunction transistor circuitry is used to trigger the thyristor.

As the tachometer output approaches the voltage desired, the base-emitter voltage of Q1 is reduced to the point at which Q1 is almost cut off. Thereby, the collector current of Q2, which charges the unijunction timing capacitor, is reduced, causing that capacitor to charge slowly and trigger the thyristor later in the half cycle. In this manner, the average power to the motor is reduced until just enough power to maintain the desired motor speed is allowed to flow.

Input circuit variations are used when the tachometer output voltage is too low to give a usable signal with a silicon rectifier. In the variation shown in Figure 6.15(b), the tachometer is connected between a voltage divider and the base of the amplifier transistor. The voltage divider is set so that with no tachometer output the transistor is just barely in conduction. As the tachometer output increases, Q_T is cut off on negative half cycles and conducts on positive half cycles. Resistors R9 and R10 provide a fixed gain for this amplifier stage, providing the h_{FE} of Q_T is much greater than the ratio of R9 to R10. Thus the output of the amplifier is a fixed multiple of the positive values of the tachometer waveform. The rectifier diode D1 prevents C1 from discharging through R9 on negative half cycles of the tachometer. The remainder of the filter and control circuitry is the same as the basic circuit.

In the second variation, shown in 6.15(c), R8 has been replaced by a semiconductor diode, D2. Since the voltage and temperature characteristics more closely match those of the transistor base-to-emitter junction, this circuit is easier to design and needs no initial adjustments as does the circuit in 6.15(b). The remainder of this circuit is identical to that of Figure 6.14.

In the second basic circuit, which is shown in Figure 6.16, the rectified and filtered tachometer voltage is added to the output voltage of the voltage divider formed by R1 and R2. If the sum of the two voltages is less than $V1 - V_{BE\ Q1}$ (where $V_{BE\ Q1}$ is the base-emitter voltage of Q1), Q1 will conduct a current proportional to $V1 - V_{BE\ Q1}$, charging capacitor C. If the sum of the two voltages is greater than $V1 - V_{BE\ Q1}$, Q1 will be cut off and no current will flow into the capacitor. The operation of the remainder of the circuit is the same as the previously described circuits.

All of the circuits that have been described show a unijunction transistor as the trigger device. A three-layer bilateral trigger diode may also be used as shown in Figure 6.17. The rectifier diode which is connected to the pulsing dc voltage, V2, discharges the capacitor at the end of each half cycle of the line voltage alternations, providing synchronization to the line voltage.

Complete circuit diagrams using the two basic circuits are shown in Figure 6.18.

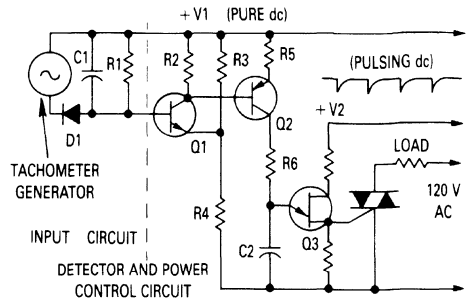
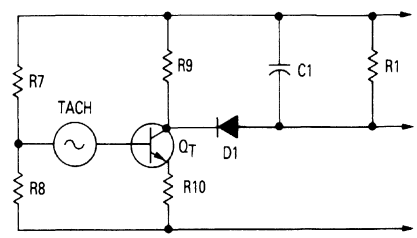
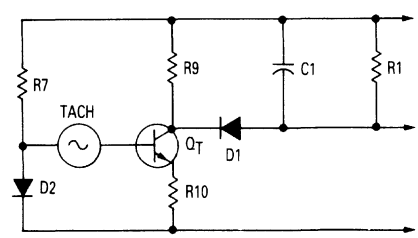


Figure 6.15(a). Basic Tachometer Control Circuit



(b). Variation Used when the Tachometer Output is Too Low for Adequate Control



(c). Variation Providing Better Temperature Tracking and Easier Initial Adjustment

PHASE CONTROL WITH TRIGGER DEVICES

Phase control using thyristors is one of the most common means of controlling the flow of power to electric motors, lamps, and heaters. With an ac voltage applied to the circuit, the gated thyristor (SCR, TRIAC, etc.) remains in its off-state for the first portion of each half cycle of the power line, then, at a time (phase angle) determined by the control circuit, the thyristor switches on for the remainder of the half cycle. By controlling the phase angle at which the thyristor is switched on, the relative power in the load may be controlled.

PHASE CONTROL WITH UNIJUNCTION TRANSISTORS

Unijunction transistors provide a simple, convenient

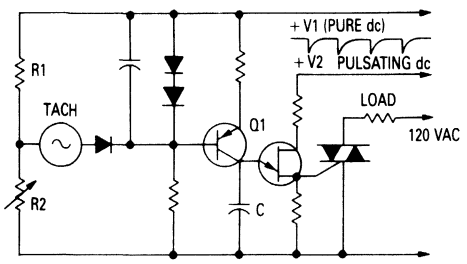


Figure 6.16. Another Basic Tachometer Circuit

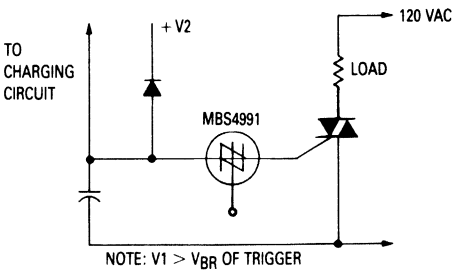


Figure 6.17. Use of a Bidirectional Switch as the Triggering Device Instead of the Unijunction Transistors Shown in Other Figures

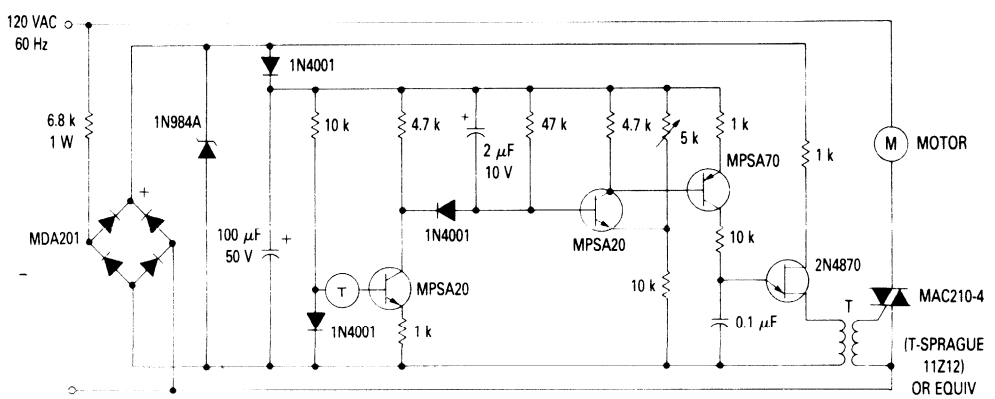


Figure 6.18(a). Complete Diagram of Tachometer Speed Control Shown in 6.15

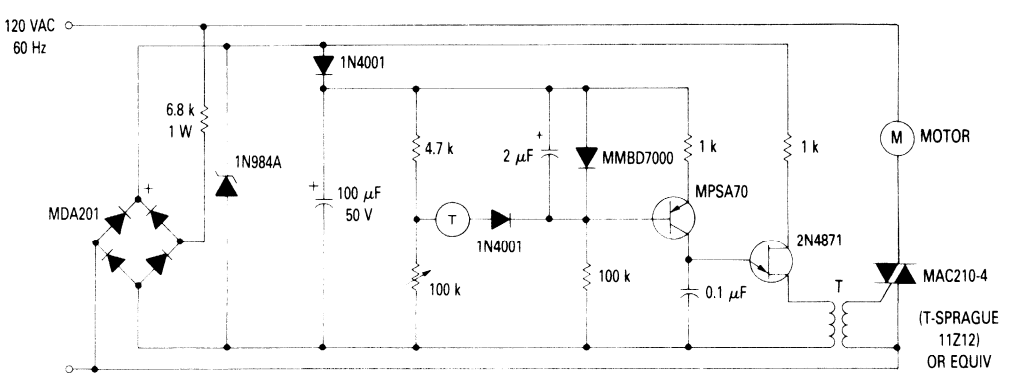


Figure 6.18(b). Complete Diagram of Tachometer Speed Control Shown in 6.16

means for obtaining the thyristor trigger pulse synchronized to the ac line at a controlled phase angle.

These circuits are all based on the simple relaxation oscillator circuit of Figure 6.19. R_T and C_T in the figure form the timing network which determines the time between the application of voltage to the circuit (represented by the closing of S1) and the initiation of the pulse. In the case of the circuit shown, with V_S pure dc, the oscillator is free running, R_T and C_T determine the frequency of oscillation. The peak of the output pulse voltage is clipped by the forward conduction voltage of the gate to cathode diode in the thyristor. The principal waveforms associated with the circuit are shown in Figure 6.19(b).

Operation of the circuit may best be described by referring to the capacitor voltage waveform. When the power is applied, C_T charges at the rate determined by its own capacitance and the value of R_T until its voltage reaches the peak point voltage of the UJT emitter. At that time the UJT switches into the conduction condition, discharging C_T through R_{B1} and the gate of the thyristor. With V_S pure dc, the cycle then repeats immediately; however, in many cases V_S is derived from the anode voltage of the thyristor so that the timing cycle cannot start again until the thyristor is blocking forward voltage and once again provides V_S.

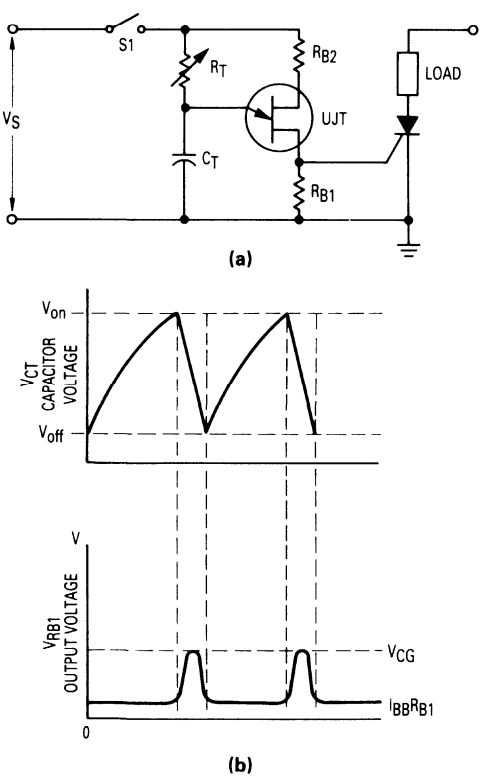


Figure 6.19. Basic Relaxation Oscillator Circuit (a) and Waveforms (b)

During the time in which the capacitor is being charged, current flows through the interbase resistance (r_{BB}) of the unijunction. R_{B1} is included in the circuit to provide a path for this current so that it does not flow through the gate of the thyristor and cause an undesirable turn on. Its value is selected so that a maximum voltage developed across it will be less than 0.2 volt. For a typical unijunction with r_{BB} = 4 to 9 kohms, and a typical operating voltage of 20 volts, the value of R_{B1} would be:

$$R_{B1} = \frac{0.2\ R_{BB(MIN)}}{V_S} = \frac{0.2 \times 4\ k}{20} = 40 \text{ ohms}$$

R_{B2} is necessary only if some degree of temperature compensation is necessary. In most cases, particularly in the feedback systems described later, it may be left out and base 2 of the unijunction may be connected to the positive side of V_S.

It is often necessary to synchronize the timing of the output pulses to the power line voltage zero-crossing points. One simple method of accomplishing synchronization is shown in Figure 6.20. Zener diode D1 clips the rectified supply voltage resulting in a V_S as shown in 6.20(b). Since V_{BB}, and therefore the peak point voltage of the unijunction drops to zero each time the line voltage corsses zero, C_T is discharged at the end of every half cycle and begins each half cycle in the discharged state. Thus, even if the UJT has not triggered during one half cycle, the capacitor begins the next half cycle discharged so that the phase angle at which the pulse occurs is directly controlled for each cycle by the values of R_T and C_T. The zener diode also provides voltage stabilization for the timing circuit giving the same pulse phase angle regardless of normal line voltage fluctuations.

APPLICATIONS

The most elementary application of the UJT trigger circuit, shown in Figure 6.21, is a half-wave control circuit. In this circuit, R_D is selected to limit the current through D_1 so that the diode dissipation capability is not exceeded. Dividing the allowable diode dissipation by one-half the zener voltage will give the allowable positive current in the diode since it is conducting in the voltage regulating mode only during positive half cycles. Once the positive half-cycle current is found, the resistor value may be calculated by subtracting 0.7 times the zener voltage from the rms line voltage and dividing the result by the positive current:

$$R_D = \frac{E_{rms} - 0.7\ V_z}{I_{positive}}$$

The power rating of R_D must be calculated on the basis of full wave conduction as D1 is conducting on the negative half cycle acting as a shunt rectifier as well as providing V_S on the positive half cycle.

The thyristor is acting both as a power control device and a rectifier, providing variable power to the load during the positive half cycle and no power to the load during

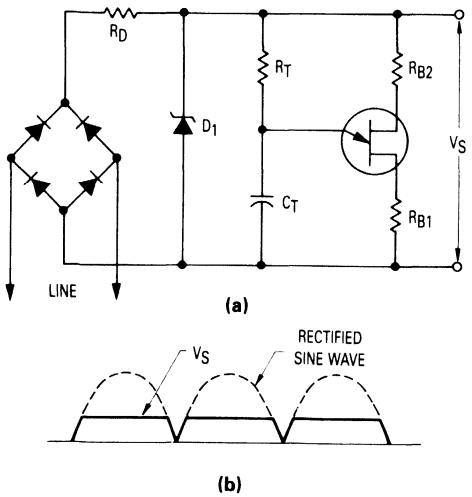


Figure 6.20. Control Circuit (a) with Zener Clipped, Rectified Voltage (b)

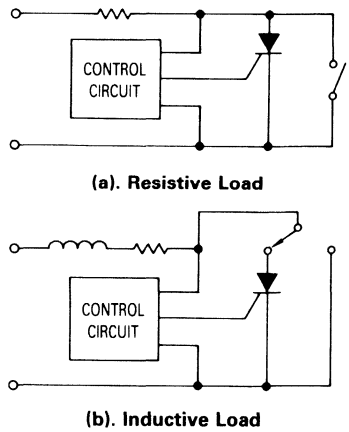


Figure 6.22. Half Wave Controls with Switching for Full Wave Operation

the negative half cycle. The circuit is designed to be a two terminal control which can be inserted in place of a switch. If full wave power is desired as the upper extreme of this control, a switch can be added which will short circuit the SCR when R_T is turned to its maximum power position. The switch may be placed in parallel with the SCR if the load is resistive; however, if the load is inductive, the load must be transferred from the SCR to the direct line as shown in Figure 6.22.

Full wave control may be realized by the addition of a bridge rectifier, a pulse transformer, and by changing the thyristor from an SCR to a TRIAC, shown in Figure 6.23. In this circuit R_{B1} is not necessary since the pulse transformer isolates the thyristor gate from the steady-state UJT current.

Occasionally a circuit is required which will provide constant output voltage regardless of line voltage changes. Adding potentiometer P1 to the circuits of Figures 6.21 and 6.23 will provide an approximate solution to this problem. The potentiometer is adjusted to provide reasonably constant output over the desired range of line voltage. As the line voltage increases, so does the voltage on the wiper of P1 increasing V_{BB} and thus the peak point voltage of the UJT. The increased peak point voltage results in C_T charging to a higher voltage and thus taking more time to trigger. The additional delay reduces the thyristor conduction angle and maintains the average voltage at a reasonably constant value.

FEEDBACK CIRCUITS

The circuits described so far have been manual control circuits; i.e., the power output is controlled by a potentiometer turned by hand. Simple feedback circuits may be constructed by replacing R_T with heat or light-dependent sensing resistors; however, these circuits have no means of adjusting the operating levels. The addition of a transistor to the circuits of Figures 6.21 and 6.23 allows complete control.

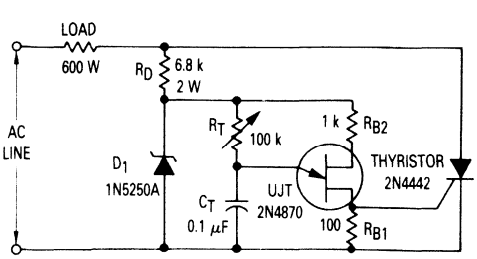


Figure 6.21. Half Wave Control Circuit with Typical Values for a 600 Watt Resistive Load

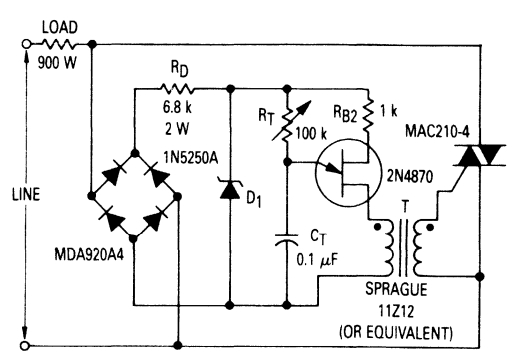


Figure 6.23. A Simple Full Wave Trigger Circuit with Typical Values for a 900 Watt Resistive Load

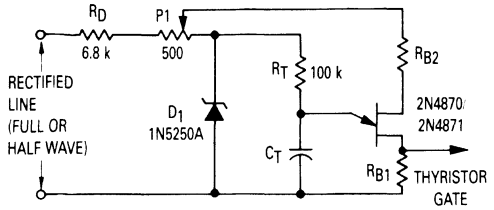


Figure 6.24. Circuit for Line Voltage Compensation

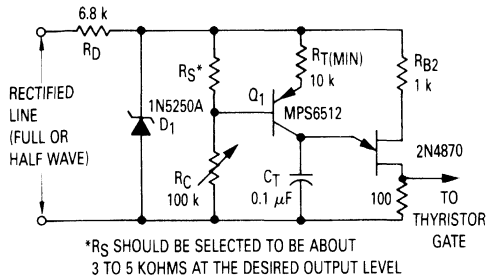


Figure 6.25. Feedback Control Circuit

Figure 6.25 shows a feedback control using a sensing resistor for feedback. The sensing resistor may respond to any one of many stimuli such as heat, light, moisture, pressure, or magnetic field. R_S is the sensing resistor and R_C is the control resistor that establishes the desired operating point. Transistor Q_1 is connected as an emitter follower such that an increase in the resistance of R_S decreases the voltage on the base of Q_1, causing more current to flow. Current through Q_1 causes voltage to charge C_T, triggering the UJT at some phase angle. As R_S becomes larger, more current flows into the capacitor, the voltage builds up faster, causing the UJT to trigger at a smaller phase angle and more power is applied to the load. When R_S decreases, less power is applied to the load. Thus, this circuit is for a sensing resistor which decreases in response to too much power in the load. If the sensing resistor increases with load power, then R_S and R_C should be interchanged.

If the quantity to be sensed can be fed back to the circuit in the form of an isolated, varying dc voltage such as the output of a tachometer, it may be inserted between the voltage divider and the base of Q1 with the proper polarity. In this case, the voltage divider would be a potentiometer to adjust the operating point. Such a circuit is shown in Figure 6.26.

In some cases, average load voltage is the desired feedback variable. In a half wave circuit this type of feedback usually requires the addition of a pulse transformer, shown in Figure 6.27. The RC network, R_1, R_2, C_1, averages load voltage so that it may be compared with the set point on R_S by Q_1. Full wave operation of this type of circuit requires dc in the load as well as the control circuit. Figure 6.28 is one method of obtaining this full wave control.

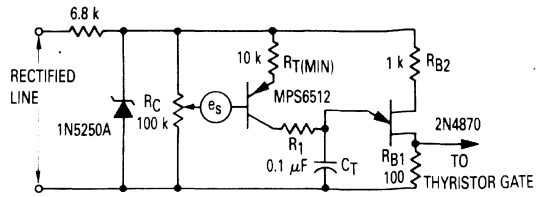


Figure 6.26. Voltage Feedback Circuit

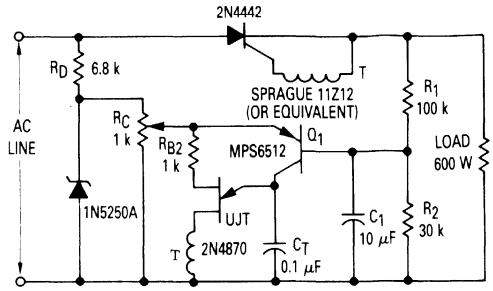


Figure 6.27. Half Wave, Average Voltage Feedback

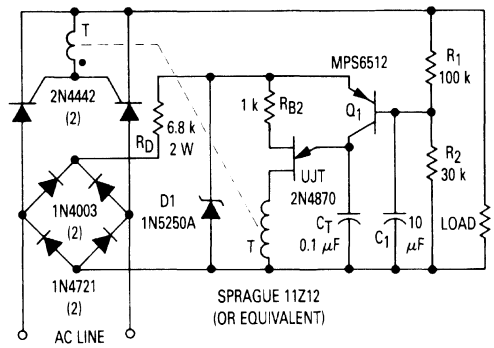


Figure 6.28. Full Wave, Average Voltage Feedback Control

There are, of course, many more sophisticated circuits which can be derived from the basic circuits discussed here. If, for example, very close temperature control is desired, the circuit of Figure 6.25 might not have sufficient gain. To solve this problem a dc amplifier could be inserted between the voltage divider and the control transistor gate to provide as close a control as desired. Other modifications to add multiple inputs, switched gains, ramp and pedestal control, etc., are all simple additions to add sophistication. Basically, however, it is the UJT itself which provides the fast rising, high current pulse, which is desirable for reliable thyristor operation. The ease of adding feedback and relative insensitivity to line voltage changes are additional benefits gained from using this trigger device.

CYCLE CONTROL WITH OPTICALLY ISOLATED TRIAC DRIVERS

In addition to the phase control circuits, TRIAC drivers can also be used for ac power control by on-off or burst control, of a number of ac cycles. This form of power control allows logic circuits and microprocessors to easily control ac power with TRIAC drivers of both the zero-crossing and non zero-crossing varieties.

USING NON-ZERO CROSSING OPTICALLY ISOLATED TRIAC DRIVERS

USING THE MOC3011 ON 240 VAC LINES

The rated voltage of a MOC3011 is not sufficiently high for it to be used directly on 240 V line; however, the designer may stack two of them in series. When used this way, two resistors are required to equalize the voltage dropped across them as shown in Figure 6.29.

REMOTE CONTROL OF AC VOLTAGE

Local building codes frequently require all 115 V light switch wiring to be enclosed in conduit. By using a MOC3011, a TRIAC, and a low voltage source, it is possible to control a large lighting load from a long distance through low voltage signal wiring which is completely isolated from the ac line. Such wiring usually is not required to be put in conduit, so the cost savings in installing a lighting system in commercial or residential buildings can be considerable. An example is shown in Figure 6.29. Naturally, the load could also be a motor, fan, pool pump, etc.

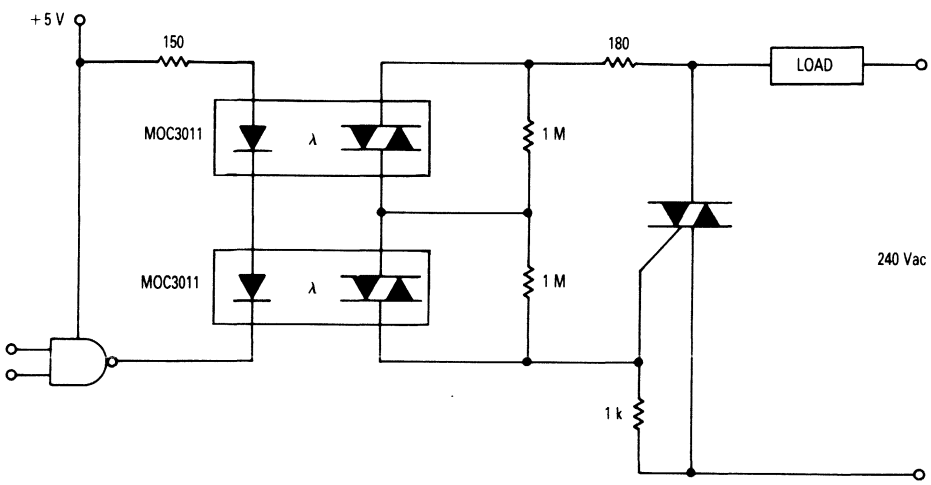


Figure 6.29. Two MOC3011 TRIAC Drivers in Series to Drive 240 V TRIAC

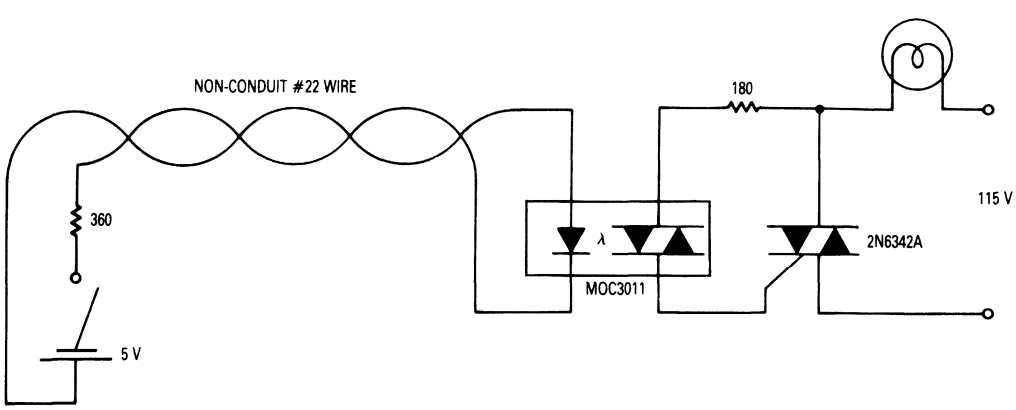


Figure 6.30. Remote Control of AC Loads Through Low Voltage Non-Conduit Cable

SOLID STATE RELAY

Figure 6.30 shows a complete general purpose, solid state relay snubbed for inductive loads with input protection. When the designer has more control of the input and output conditions, he can eliminate those components which are not needed for his particular application to make the circuit more cost effective.

INTERFACING MICROPROCESSORS TO 115 VAC PERIPHERALS

The output of a typical microcomputer input-output (I/O) port is a TTL-compatible terminal capable of driving one or two TTL loads. This is not quite enough to drive the MOC3011, nor can it be connected directly to an SCR or TRIAC, because computer common is not normally referenced to one side of the ac supply. Standard 7400 series gates can provide an input compatible with the output of an MC6821, MC6846 or similar peripheral interface adaptor and can directly drive the MOC3011. If the second input of a 2 input gate is tied to a simple timing circuit, it will also provide energization of the TRIAC only at the zero crossing of the ac line voltage as shown in Figure 6.32. This technique extends the life of incandescent lamps, reduces the surge current strains on the TRIAC, and reduces EMI generated by load switching. Of course, zero crossing can be generated within the microcomputer itself, but this requires considerable software overhead and usually just as much hardware to generate the zero-crossing timing signals.

APPLICATIONS USING THE ZERO CROSSING TRIAC DRIVER

For applications where EMI induced, non-zero crossing-load switching is a problem, the zero crossing TRIAC driver is the answer. This TRIAC driver can greatly simplify the suppression of EMI for only a nominal increased cost. Examples of several applications using the MOC3031, 41 follows.

MATRIX SWITCHING

Matrix, or point-to-point switching, represents a method of controlling many loads using a minimum number of components. On the 115 V line, the MOC3031 is ideal for this application; refer to Figure 6.33. The large static dv/dt rating of the MOC3031 prevents unwanted

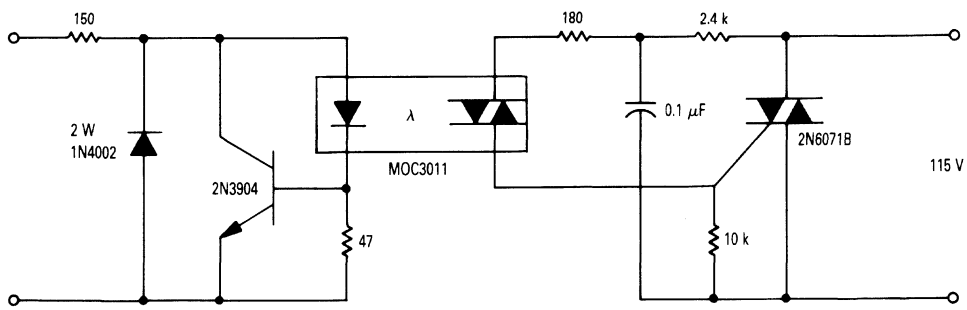


Figure 6.31. Solid-State Relay

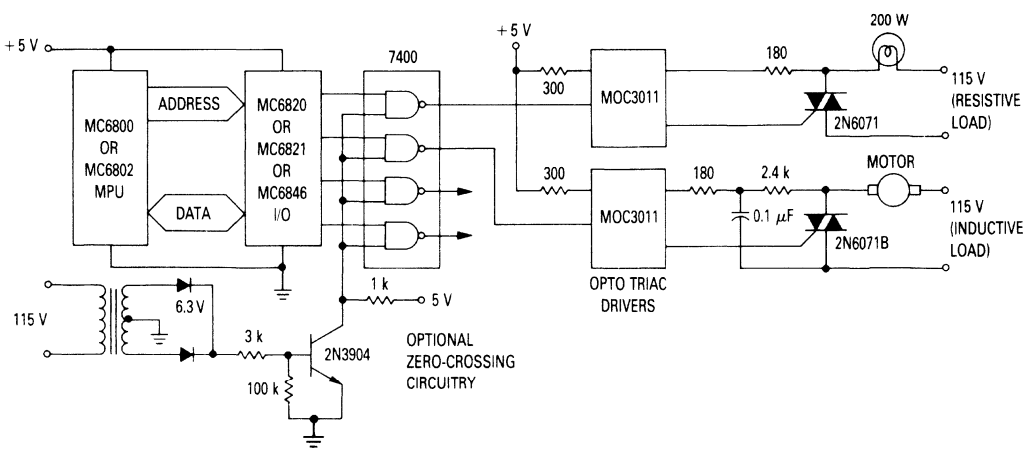


Figure 6.32. Interfacing an M6800 Microcomputer System to 115 Vac Loads

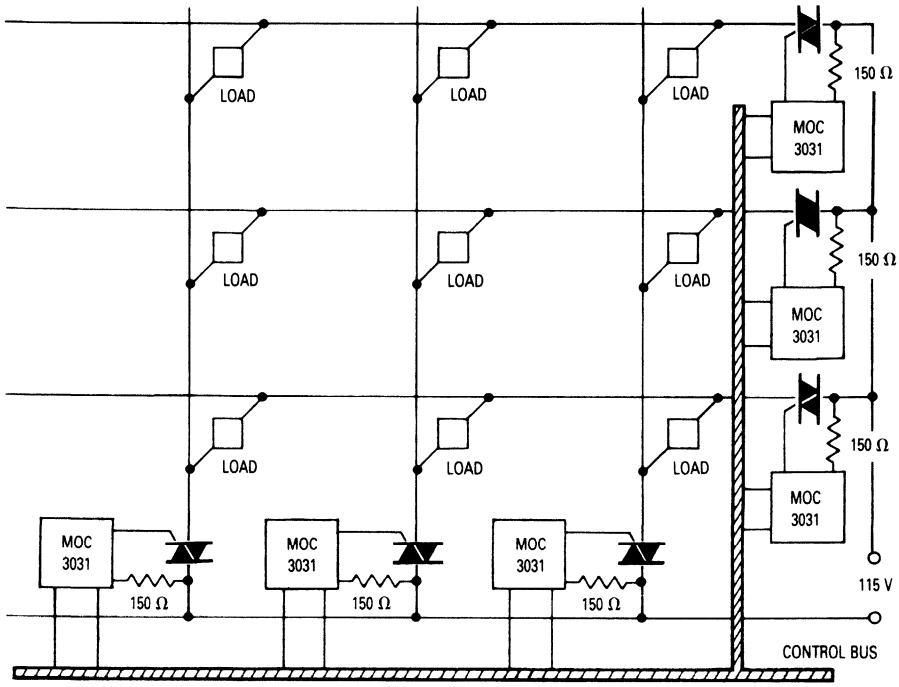


Figure 6.33. Matrix Switching

loads from being triggered on. This might occur, in the case of non-zero crossing TRIAC drivers, when a TRIAC driver on a vertical line was subjected to a large voltage ramp due to a TRIAC on a horizontal line being switched on. Since non-zero crossing TRIAC drivers have lower static dv/dt ratings, this ramp would be sufficiently large to trigger the device on.

R is determined as before:

$$R_{(min)} = \frac{V_{in(pk)}}{I_{TSM}}$$

$$= \frac{170\ V}{1.2\ A} = 150 \text{ ohms}$$

POWER RELAYS

The use of high-power relays to control the application of ac power to various loads is a very widespread practice. Their low contact resistance causes very little power loss and many options in power control are possible due to their multipole-multithrow capability. The MOC3041 is well suited to the use of power relays on the 230 Vac line; refer to Figure 6.34. The large static dv/dt of this device makes a snubber network unnecessary, thus reducing component count and the amount of printed circuit board space required. A non-zero crossing TRIAC

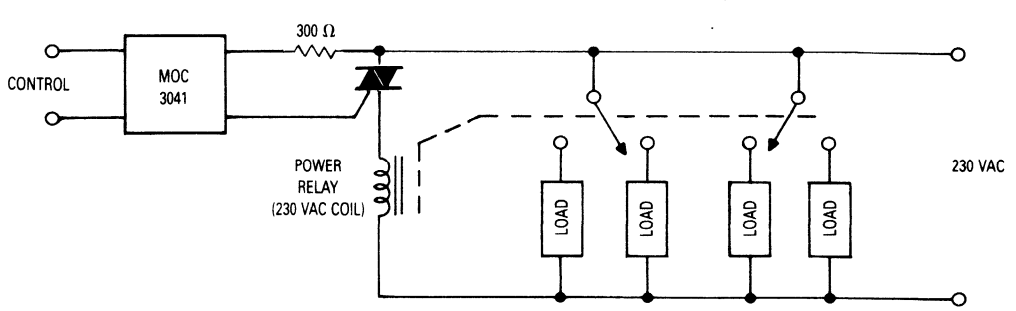


Figure 6.34. Power Relay Control

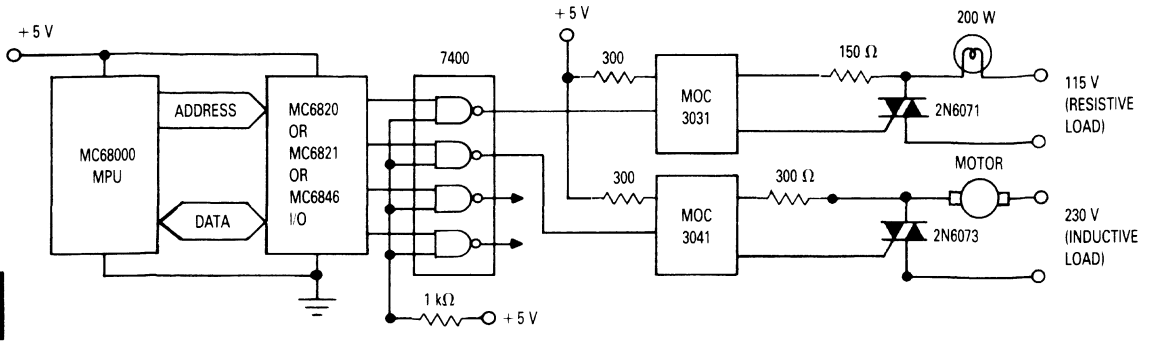


Figure 6.35. M68000 Microcomputer Interface

driver (MOC3021) could be used in this application, but its lower static dv/dt rating would necessitate a snubber network.

MICROCOMPUTER INTERFACE

The output of most microcomputer input/output (I/O) ports is a TTL signal capable of driving several TTL gates. This is insufficient to drive a zero-crossing TRIAC driver. In addition, it cannot be used to drive an SCR or TRIAC directly, because computer common is not usually referenced to one side of the ac supply. However, standard 7400 NAND gates can be used as buffers to accept the output of the I/O port and in turn, drive the MOC3031 and/or MOC3041; refer to Figure 6.35.

The zero-crossing feature of these devices extends the life of incandescent lamps, reduces inrush currents and minimizes EMI generated by load switching.

AC MOTORS

The large static dv/dt rating of the zero-crossing TRIAC drivers make them ideal when controlling ac motors. Figure 6.36 shows a circuit for reversing a two phase motor using the MOC3041. The higher voltage MOC3041 is required, even on the 115 Vac line, due to the mutual and self-inductance of each of the motor windings, which may cause a voltage much higher than 115 Vac to appear across the winding which is not conducting current.

DETERMINING LIMITING RESISTOR R FOR A HIGH-WATTAGE INCANDESCENT LAMP

Many high-wattage incandescent lamps suffer shortened lifetimes when switched on at ac line voltages other than zero. This is due to a large inrush current destroying the filament. A simple solution to this problem is the use of the MOC3041 as shown in Figure 6.37. The MOC3041 may be controlled from a switch or some form of digital logic.

The minimum value of R is determined by the maximum surge current rating of the MOC3041 (I_{TSM}):

$$R_{(min)} = \frac{V_{in(pk)}}{I_{TSM}} = \frac{V_{in(pk)}}{1.2\ A} \qquad (10)$$

On a 230 Vac Line:

$$R_{(min)} = \frac{340\ V}{1.2\ A} = 283\ \text{ohms} \qquad (11)$$

In reality, this would be a 300 ohm resistor.

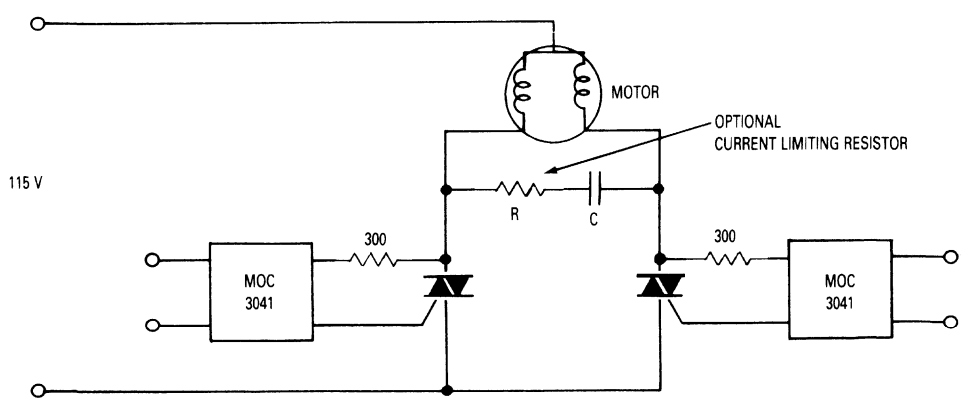


Figure 6.36. Reversing Motor Circuit

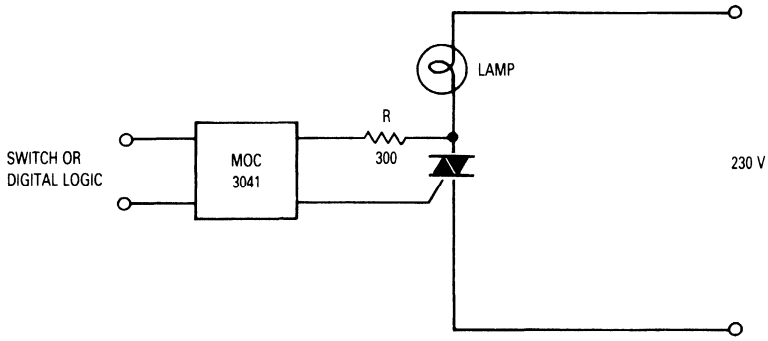


Figure 6.37. High-Wattage Lamp Control

AC POWER CONTROL WITH SOLID-STATE RELAYS

The Solid-State Relay (SSR) as described below, is a relay function with:

a. Four Terminals (Two Input, Two Output)
b. DC or AC Input
c. Optical Isolation Between Input and Output
d. Thyristor (SCR or TRIAC) Output
e. Zero Voltage Switching Output (Will Only Turn On Close to Zero Volts)
f. AC Output (50 or 60 Hz)

Figure 6.38 shows the general format and waveforms of the SSR. The input on/off signal is conditioned (perhaps only by a resistor) and fed to the Light-Emitting-Diode (LED) of an optoelectronic-coupler. This is ANDed with a go signal that is generated close to the zero-crossing of the line, typically ≤ 10 Volts. Thus, the output is not gated on via the amplifier except at the zero-crossing of the line voltage. The SSR output is then re-gated on at the beginning of every half-cycle until the input on signal is removed. When this happens, the thyristor output stays on until the load current reaches zero, and then turns off.

ADVANTAGES AND DISADVANTAGES OF SSRs

The SSR has several advantages that make it an attractive choice over its progenitor, the Electromechanical Relay (EMR) although the SSR generally costs more than its electromechanical counterpart. These advantages are:

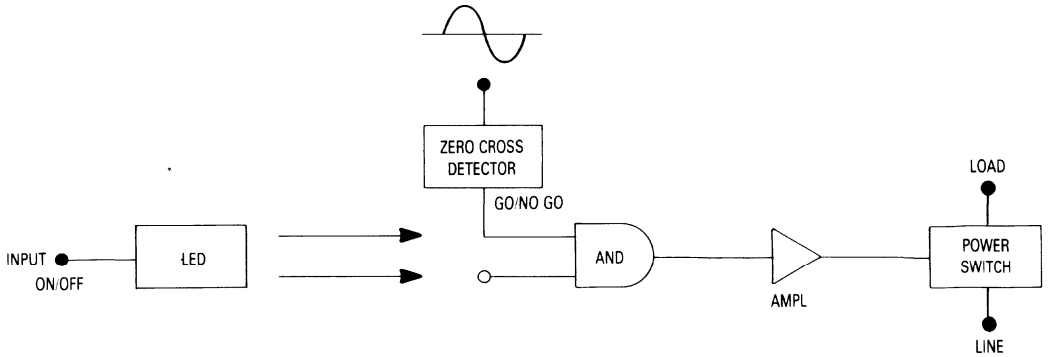
1) No Moving Parts — the SSR is all solid-state. There are no bearing surfaces to wear, springs to fatigue, assemblies to pick up dust and rust. This leads to several other advantages.
2) No Contact Bounce — this in turn means no contact wear, arcing, or Electromagnetic Interference (EMI) associated with contact bounce.
3) Fast Operation — usually less than 10 μs. Fast turn-on time allows the SSR to be easily synchronized with line zero-crossing. This also minimizes EMI and can greatly increase the lifetime of tungsten lamps, of considerable value in applications such as traffic signals.
4) Shock and Vibration Resistance — the solid-state contact cannot be "shaken open" as easily as the EMR contact.
5) Absence of Audible Noise — this devolves from the lack of moving mechanical parts.
6) Output Contact Latching — the thyristor is a latching device, and turns off only at the load current zero-crossing, minimizing EMI.
7) High Sensitivity — the SSR can readily be designed to interface directly with TTL and CMOS logic, simplifying circuit design.
8) Very Low Coupling Capacitance Between Input and Output. This is a characteristic inherent in the opto-electronic-coupler used in the SSR, and can be useful in areas such as medical electronics where the reduction of stray leakage paths is important.

This list of advantages is impressive, but of course, the designer has to consider the following disadvantages:

1) Voltage Transient Resistance — the ac line is not the clean sine wave obtainable from a signal generator. Superimposed on the line are voltage spikes from motors, solenoids, EMRs (ironical), lightning, etc. The solid-state components in the SSR have a finite voltage rating and must be protected from such spikes, either with RC networks (snubbing), zener diodes, MOVs or selenium voltage clippers. If not done, the thyristors will turn on for part of a half cycle, and at worst, they will be permanently damaged, and fail to block voltage. For critical applications a safety margin on voltage of 2 to 1 or better should be sought.

   The voltage transient has at least two facets — the first is the sheer amplitude, already discussed. The second is its frequency, or rate-of-rise of voltage (dv/dt). All thyristors are sensitive to dv/dt to some extent, and the transient must be snubbed, or "soaked up," to below this level with an RC network.(1) Typically this rating ("critical" or "static"

(1) For a more thorough discussion of snubbers, see page 1-3-9.



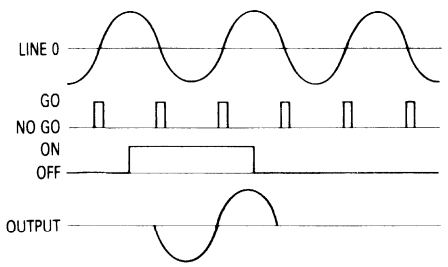


Figure 6.38. SSR Block Diagram

dv/dt) is 50 to 100 V/μs at maximum temperature. Again the failure mode is to let through, to a half-cycle of the line, though a high energy transient can cause permanent damage. Table 6.I gives some starting points for snubbing circuit values. The component values required depend on the characteristics of the transient, which are usually difficult to quantify. Snubbing across the line as well as across the SSR will also help.

Load Current A rms	Resistance Ω	Capacitance μF
5	47	0.047
10	33	0.1
25	10	0.22
40	22	0.47

Table 6.I. Typical Snubbing Values

2) Voltage Drop — The SSR output contact has some offset voltage — approximately 1 V, depending on current, causing dissipation. As the thyristor has an operating temperature limit of +125°C, this heat must be removed, usually by conduction to air via a heat sink or the chassis.
3) Leakage Current — When an EMR is open, no current can flow. When an SSR is open however, it does not have as definite an off condition. There is always some current leakage through the output power switching thyristor, the control circuitry, and the snubbing network. The total of this leakage is usually 1 to 10 mA rms — three or four orders of magnitude less than the on-state current rating.
4) Multiple Poles — are costly to obtain in SSRs, and three phase applications may be difficult to implement.
5) Nuclear Radiation — SSRs will be damaged by nuclear radiation.

TRIAC SSR CIRCUIT

Many SSR circuits use a TRIAC as the output switching device. Figure 6.39(a) shows a typical TRIAC SSR circuit. The control circuit is used in the SCR relay as well, and is defined separately. The input circuit is TTL compatible. Output snubbing for inductive loads will be described later.

A sensitive-gate SCR (SCR1) is used to gate the power TRIAC, and a transistor amplifier is used as an interface between the optoelectronic-coupler and SCR1. (A sensitive-gate SCR and a diode bridge are used in preference to a sensitive gate TRIAC because of the higher sensitivity of the SCR.)

CONTROL CIRCUIT OPERATION

The operation of the control circuit is straightforward. The AND function of Figure 6.38 is performed by the wired-NOR collector configuration of the small-signal transistors Q1 and Q2. Q1 clamps the gate of SCR1 if optoelectronic-coupler OC1 is off. Q2 clamps the gate if there is sufficient voltage at the junction of the potential divider R4, R5 to overcome the V_{BE} of Q2. By judicious selection of R4 and R5, Q2 will clamp SCR1's gate if more than approximately 5 Volts appear at the anode of SCR1; i.e., Q2 is the zero-crossing detector.

If OC1 is on, Q1 is clamped off, and SCR1 can be turned on by current flowing down R6, only if Q2 is also off — which it is only at zero crossing.

The capacitors are added to eliminate circuit race conditions and spurious firing, time ambiguities in operation. Figure 6.39(b) shows the full-wave rectified line that appears across the control circuit. The zero voltage firing

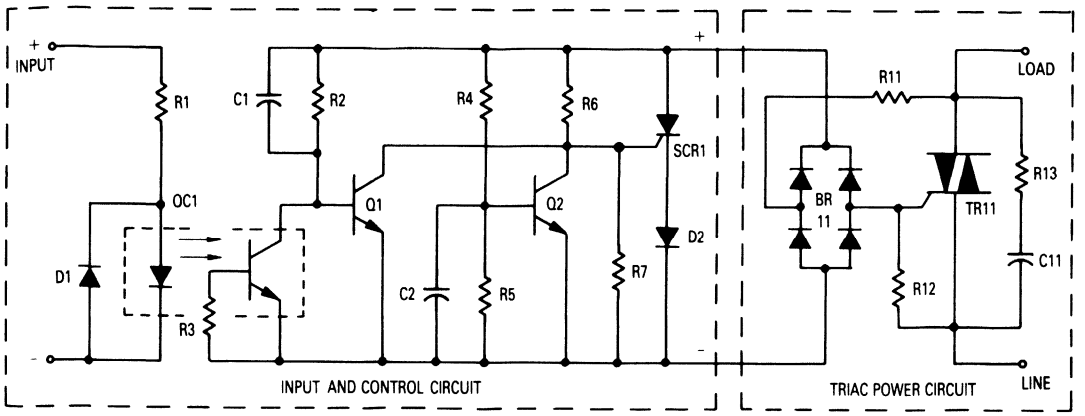


Figure 6.39(a). TRIAC SSR Circuit

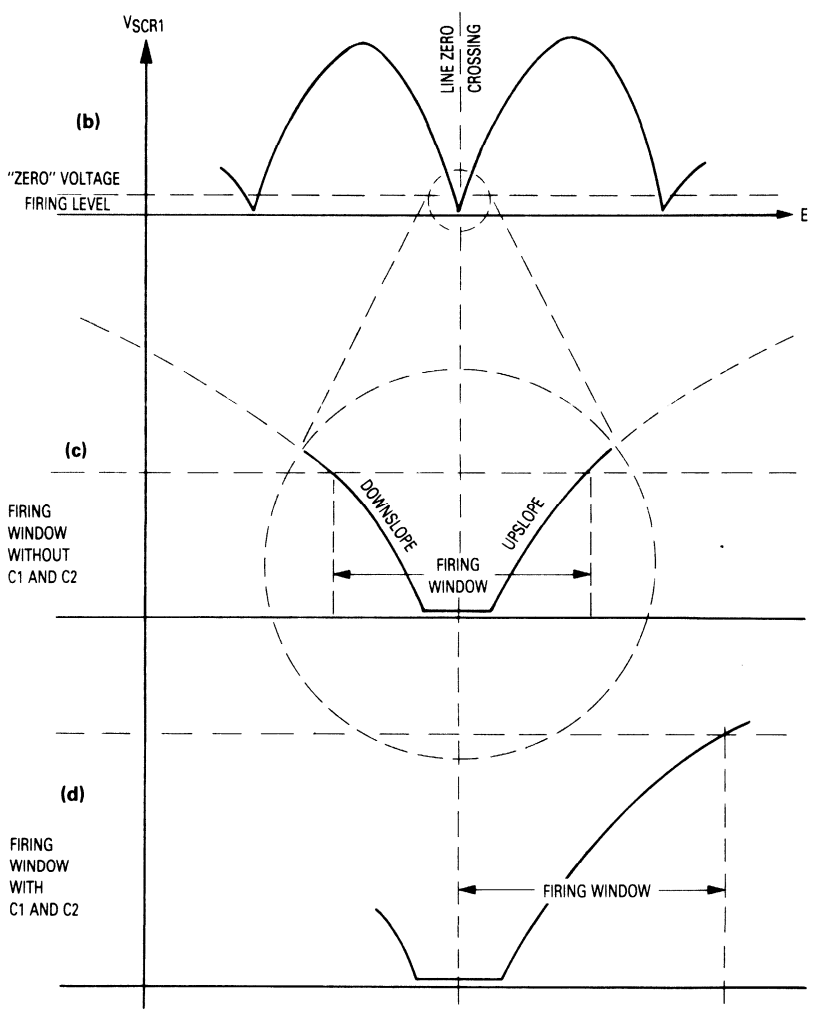


Figure 6.39. Firing Windows

level is shown in 6.39(b) and 6.39(c), expanded in time and voltage. A race condition exists on the up-slope of the second half-cycle in that SCR1 may be triggered via R6 before Q1 has enough base current via R2 to clamp SCR1's gate. C1 provides current by virtue of the rate of change of the supply voltage, and Q1 is turned on firmly as the supply voltage starts to rise, eliminating any possibility of unwanted firing of the SSR; thus eliminating the race condition.

This leaves the possibility of unwanted firing of the SSR on the down-slope of the first half cycle shown. C2 provides a phase shift to the zero voltage potential divider, and Q2 is held on through the real zero-crossing. The resultant window is shown in 6.39(d).

1

CONTROL CIRCUIT COMPONENTS

The parts list for the control circuit at two line voltages is shown in Table 6.II.

R1 limits the current in the input LED of OC1. The input circuit will function over the range of 3 to 33 Vdc.

D1 provides reverse voltage protection for the input of OC1.

D2 allows the gate of SCR1 to be reverse biased, providing better noise immunity and dv/dt performance.

R7 eliminates pickup on SCR1's gate through the zero-crossing interval.

SCR1 is a sensitive gate SCR; the 2N5064 is a TO-92 device, the 2N6240 is a Case 77 device.

Alternatives to the simple series resistor (R1) input circuit will be described later.

POWER CIRCUIT COMPONENTS

The parts list for the TRIAC power circuit in Figure 6.39(a) is shown in Table 6.III for several rms current ratings, and two line voltages. The metal TRIACs are in the half-inch pressfit package in the isolated stud configuration; the plastic TRIACs are in the TO-220 Thermowatt package. R12 is chosen by calculating the peak control circuit off-state leakage current and ensuring that the voltage drop across R12 is less than the $V_{GT(MIN)}$ of the TRIAC.

Table 6.II. Control Circuit Parts List

Part	Line Voltage 120 V rms	Line Voltage 240 V rms
C1	220 pF, 20%, 200 Vdc	100 pF, 20%, 400 Vdc
C2	0.022 μF, 20%, 50 Vdc	0.022 μF, 20%, 50 Vdc
D1	1N4001	1N4001
D2	1N4001	1N4001
OC1	MOC1005	MOC1005
Q1	MPS5172	MPS5172
Q2	MPS5172	MPS5172
R1	1 kΩ, 10%, 1 W	1 kΩ, 10%, 1 W
R2	47 kΩ, 5%, 1/2 W	100 kΩ, 5%, 1 W
R3	1 MΩ, 10%, 1/4 W	1 MΩ, 10%, 1/4 W
R4	110 kΩ, 5%, 1/2 W	220 kΩ, 5%, 1/2 W
R5	15 kΩ, 5%, 1/4 W	15 kΩ, 5%, 1/4 W
R6	33 kΩ, 10%, 1/2 W	68 kΩ, 10%, 1 W
R7	10 kΩ, 10%, 1/4 W	10 kΩ, 10%, 1/4 W
SCR1	2N5064	2N6240

C11 must be an ac rated capacitor, and with R13 provides some snubbing for the TRIAC. The values shown for this network are intended more for inductive load commutating dv/dt snubbing than for voltage transient suppression. Consult the individual data sheets for the dissipation, temperature, and surge current limits of the TRIACs.

TRIACs AND INDUCTIVE LOADS

The TRIAC is a single device which to some extent is the equivalent of two SCRs inverse parallel connected; certainly this is so for resistive loads. Inductive loads however, can cause problems for TRIACs, especially at turn-off.

A TRIAC turns off every line half-cycle when the line current goes through zero. With a resistive load, this coincides with the line voltage also going through zero. The TRIAC must regain blocking-state before there are more than 1 or 2 Volts of the reverse polarity across it — at 120 V rms, 60 Hz line this is approximately 30 μs. The TRIAC has not completely regained its off-state charac-

Table 6.III. TRIAC Power Circuit Parts List

Voltage		120 V rms				240 V rms			
rms Current Amperes		8	12	25	40	8	12	25	40
BR11		MDA102A	MDA102A	MDA102A	MDA102A	MDA104A	MDA104A	MDA104A	MDA104A
C11, μF (10%, line voltage ac rated)		0.047	0.047	0.1	0.1	0.047	0.047	0.1	0.1
R11 (10%, 1 W)		39	39	39	39	39	39	39	39
R12 (10%, 1/2 W)		18	18	18	18	18	18	18	18
R13 (10%, 1/2 W)		620	620	330	330	620	620	330	330
TR11	Plastic	2N6342	2N6342A	—	—	2N6343	2N6343A	—	—
	Metal	—	T4121B	2N6163	T6420B	—	T4121D	T4121D	T6420D

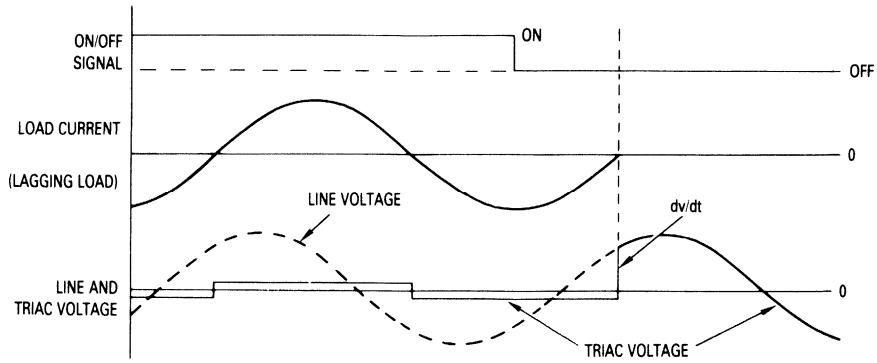


Figure 6.40. Commutating dv/dt

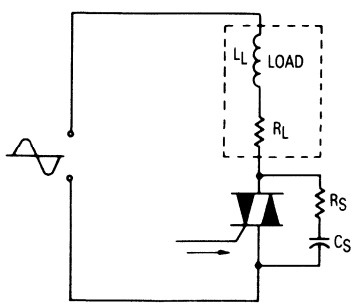


Figure 6.41. TRIAC with Snubber Network

teristics, but does so as the line voltage increases at the 60 Hz rate.

Figure 6.40 indicates what happens with an inductive or lagging load. The on signal is removed asynchronously and the TRIAC, a latching device, stays on until the next current zero. As the current is lagging the applied voltage, the line voltage at that instant appears across the TRIAC. It is this rate-of-rise of voltage, the commutating dv/dt, that must be limited in TRIAC circuits, usually to a few volts per microsecond. This is normally done by use of a snubber network R_S and C_S as shown in Figure 6.41.

SCRs have less trouble as each device has a full half-cycle to turn off and, once off, can resist dv/dt to the critical value of 50 to 100 V/μs.

CHOOSING THE SNUBBING COMPONENTS(1)

There are no easy methods for selecting the values of R_S and C_S in Figure 6.41 required to limit commutating dv/dt. The circuit is a damped tuned circuit comprised by R_S, C_S, R_L and L_L, and to a minor extent the junction capacitance of the TRIAC. At turn-off this circuit receives a step impulse of line voltage which depends on the power factor of the load. Assuming the load is fixed, which is normally the case, the designer can vary R_S and

(1) For a more thorough discussion of snubbers, see page 1-3-9.

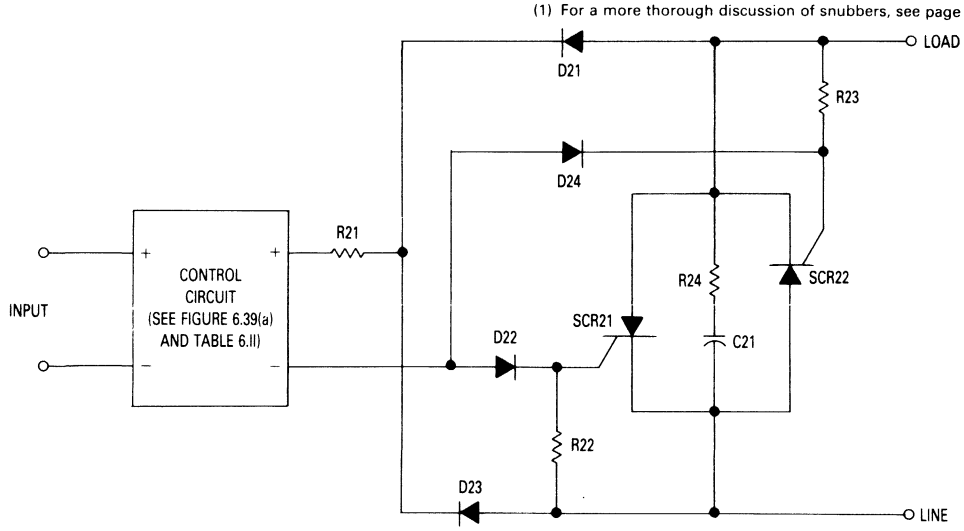


Figure 6.42. SCR SSR Circuit

C_S. C_S can be increased to decrease the commutating dv/dt; R_S can be increased to decrease the resonant overring of the tuned circuit — to increase damping. This can be done empirically, beginning with the values for C11 and R13 given in Table 6.III, and aiming at close to critical damping and the data sheet value for commutating dv/dt. Reduced temperatures, voltages, and off-going di/dt (rate-of-change of current at turn-off) will give some safety margin.

SCR SSR CIRCUIT

The inverse parallel connected Silicon Controlled Rectifier (SCR) pair (shown in Figure 6.42) is less sensitive to commutating dv/dt. Other advantages are the improved thermal and surge characteristics of having two devices; the disadvantage is increased cost.

The SCR power circuit can use the same control circuit as the TRIAC Circuit shown in Figure 6.39(a). In Figure 6.42, for positive load terminal and when the control circuit is gated on, current flows through the load, D21, R21, SCR1, D22, the gate of SCR21 and back to the line, thus turning on SCR21. Operation is similar for the other line polarity. R22 and R23 provide a path for the off-state leakage of the control circuit and are chosen so that the voltage dropped across them is less than the $V_{GT(MIN)}$ of the particular SCR. R24 and C21 provide snubbing and line transient suppression, and may be chosen from Table 6.IV or from the C11, R13 rows of Table 6.III. The latter values will provide less transient protection but also less off-state current, with the capacitor being smaller. Other circuit values are shown in Table 6.IV.

Consult the individual data sheets for packages and dissipation, temperature, and surge current limits.

While the SCRs have much higher dv/dt commutation ability, with inductive loads, attention should be paid to maintaining the dv/dt below data sheet levels.

ALTERNATE INPUT CIRCUITS

CMOS COMPATIBLE

The 1 kΩ resistor, R1, shown in Figure 6.39(a) and Table 6.II, provide an input that is compatible with the current that a TTL gate output can sink. The resistor R1 must be changed for CMOS compatibility, aiming at 2 mA in the LED for adequate performance to 100°C. At 2 mA do not use the CMOS output for any other function, as a LOGIC 0 or 1 may not be guaranteed. Assume a forward voltage drop of 1.1 V for the LED, and then make the Ohm's Law calculation for the system dc supply voltage, thus defining a new value for R1.

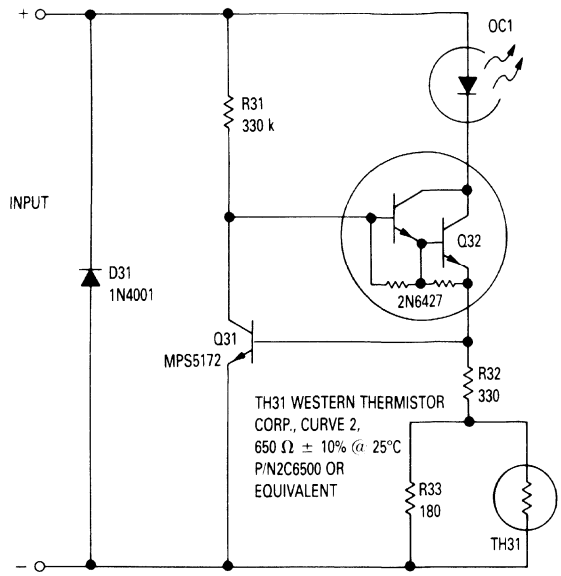


Figure 6.43. TTL/CMOS Compatible Input

TTL/CMOS COMPATIBLE

To be TTL compatible at 5 Volts and CMOS compatible over 3 to 15 Volts, a constant current circuit is required, such as the one in Figure 6.43. The current is set by the V_{BE} of Q31 and the resistance of the R32, R33, and thermistor TH31 network, and is between 1 and 2 mA, higher at high temperatures to compensate for the reduced transmission efficiency of optoelectronic-couplers at higher temperature. The circuit of Figure 6.43 gives an equivalent impedance of approximately 50 kΩ. The circuit

Table 6.IV. SCR Power Circuit Parts List

Voltage		120 V rms				240 V rms			
rms Current Amperes		5	11	22	49	5	11	22	49
C21 (10%, line voltage ac rated)		← SEE TEXT →							
D21–24		1N4003	1N4003	1N4003	1N4003	1N4004	1N4004	1N4004	1N4004
R21 (10%, 1 W)		39	39	39	39	39	39	39	39
R22, 23 (10%, 1/2 W)		18	18	18	18	18	18	18	18
R24		← SEE TEXT →							
SCR21,22	Plastic	2N6239	2N4442	2N6402	—	2N6240	2N4443	2N6403	—
	Metal	—	2N4170	2N6168	2N6172	—	2N4172	2N6169	2N6173

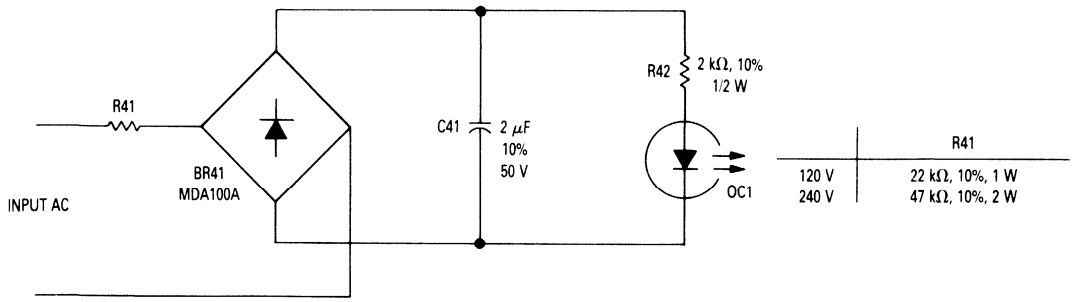


Figure 6.44. AC Compatible Input

performs adequately over 3 to 33 Vdc and −40 to +100°C. Note that though the SSR is protected against damage from improperly connected inputs, the external circuit is not, as D31 acts as a bypass for a wrongly connected input driver.

AC LINE COMPATIBLE

To use SSRs as logic switching elements is inefficient, considering the availability and versatility of logic families such as CMOS. When it is convenient to trigger from ac, a circuit such as shown in Figure 6.44 may be used. The capacitor C41 is required to provide current to the LED of OC1 through the zero-crossing time. An in-phase input voltage gives the worst case condition. The circuit gives 2 mA minimum LED current at 75% of nominal line voltage.

INVERSE PARALLEL SCRs FOR POWER CONTROL

TRIACs are very useful devices. They end up in solid state relays, lamp drivers, motor controls, sensing and detection circuits; just about any industrial full-wave application. But in high-frequency applications or those requiring high voltage or current, their role is limited by their present physical characteristics, and they become very expensive at current levels above 40 amperes rms.

SCRs can be used in an inverse-parallel connection to bypass the limitations of a TRIAC. A simple scheme for doing this is shown in Figure 6.45. Table 6.V. lists suggested SCR's for this circuit configuration. The control device can take any of many forms, shown is the reed relay (Figure 6.45). TRIACs and Opto couplers can be inserted at point A-A to replace the reed relay.

Compared to a TRIAC, an inverse-parallel configuration has distinct advantages. Voltage and current capabilities are dependent solely on SCR characteristics with ratings today of over a thousand volts and several hundred amps. Because each SCR operates only on a half-wave basis, the system's rms current rating is $\sqrt{2}$ times the SCR's rms current rating (see Suggested SCR chart). The system has the same surge current rating as the SCRs do. Operation at 400 Hz is also no problem. While turn-off time and dv/dt limits control TRIAC operating speed, the recovery characteristics of an SCR need only be better than the appropriate half-wave period.

With inductive loads you no longer need to worry about commutating dv/dt, either. SCRs only need to withstand static dv/dt, for which they are typically rated an order of magnitude greater than TRIACs are for commutating dv/dt.

Better reliability can be achieved by replacing the reed relay with a low current TRIAC to drive the SCRs, although some of its limitations come with it. In the preferred circuit of Figure 6.45(b), the main requirements of

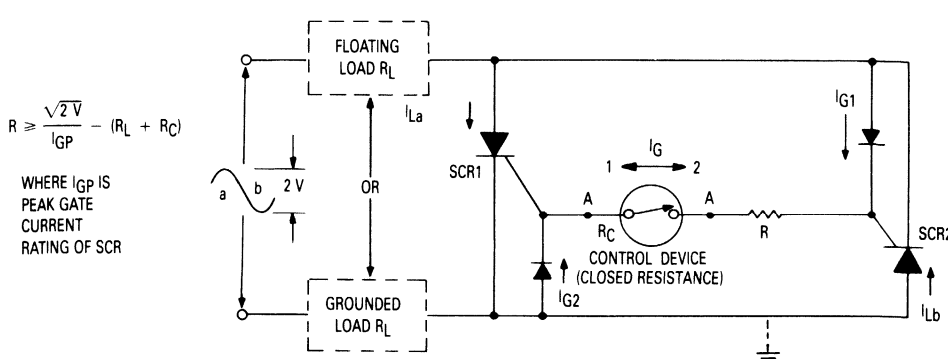


Figure 6.45. Use of Inverse Parallel SCRs

Table 6.V. Suggested SCRs

Line Voltage (rms)	Load Current (rms)	SCR	SCR Current Rating (rms)
120 V	25 A	2N5169	20 A
220 V	25 A	2N5170	20 A
120 V	35 A	2N6506	25 A
220 V	35 A	2N6507	25 A
120 V	50 A	2N3897	35 A
220 V	50 A	2N3898	35 A
120 V	75 A	MCR64-4	55 A
220 V	75 A	MCR64-6	55 A

1

the TRIAC are that it be able to block the peak system voltage and that it have a surge current rating compatible with the gate current requirements of the SCRs. This is normally so small that a TO-92 cased device is adequate to drive the largest SCRs.

In circuits like Figure 6.45, the control devices alternately pass the gate currents I_{G1} and I_{G2} during the "a" and "b" half cycles, respectively. I_{La} and I_{Lb} are the load currents during the corresponding half cycles. Each SCR then gets the other half cycle for recovery time. Heat sinking can also be done more efficiently, since power is being dissipated in two packages, rather than all in one. The load can either be floated or grounded. If the SCRs are not of the shunted-gate variety, a gate-cathode resistance should be added to shunt the leakage current at higher temperatures. The diodes act as steering diodes so the gate-cathode junctions are not avalanched. The blocking capability of the diodes need only be as high as the V_{GT} of the SCRs. A snubber can also be used if conditions dictate.

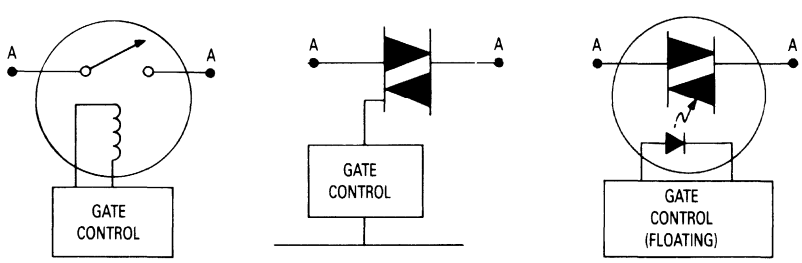
This circuit offers several benefits. One is a considerable increase in gain. This permits driving the TRIAC with almost any other semiconductors such as linear ICs, photosensitive devices and logic, including MOS. If necessary, it can use an optically coupled TRIAC driver to isolate (up to 7500 V isolation) delicate logic circuits from the power circuit (see Figure 6.46(c)). Table 6.VI. lists suggested components. Another benefit is being able to gate the TRIAC with a supply of either polarity. Probably the most important benefit of the TRIAC/SCR combination is its ability to handle variable-phase applications — nearly impossible for non solid-state control devices.

INTERFACING DIGITAL CIRCUITS TO THYRISTOR CONTROLLED AC LOADS

Because they are bidirectional devices, TRIACs are the most common thyristor for controlling ac loads. A TRIAC can be triggered by either a positive or negative gate signal on either the positive or negative half-cycle of applied MT2 voltage, producing four quadrants of operation. However, the TRIAC's trigger sensitivity varies with the quadrant, with quadrants II and III (gate signal negative and MT2 either positive or negative) being the most sensitive and quadrant IV (gate positive, MT2 negative) the least sensitive.

For driving a TRIAC with IC logic, quadrants II and III are particularly desirable, not only because less gate trigger current is required, but also because IC power dissipation is reduced since the TRIAC can be triggered by an "active low" output from the IC.

There are other advantages to operating in quadrants II and III. Since the rate of rise of on-state current of a TRIAC (di/dt) is a function of how hard the TRIAC's gate



(a). Reed Relay **(b). Low-Current TRIAC** **(c). Optically Coupled TRIAC Driver**

Figure 6.46. Control Devices

Table 6.VI. Driver TRIACs

Line Voltage	Gate Negative Or In Phase With Line Voltage	Gate Positive	Optically Coupled
120	MAC97A4	MAC97A4	MOC3030*, 3011
220	MAC97A6	MAC97A6	MOC3020, MOC3021

*Includes inhibit circuit for zero crossover firing.

is turned on, a given IC output in quadrants II and III will produce a greater di/dt capability than in the less sensitive quadrant IV. Moreover, harder gate turn-on could reduce di/dt failure. One additional advantage of quadrant II and III operation is that devices specified in all four quadrants are generally more expensive than devices specified in quadrants I, II and III, due to the additional testing involved and the resulting lower yields.

USING TRIACs

Once the TRIAC load requirements are defined, an appropriate device selection can be made by referring to the TRIAC current ratings of Table 6.VII.

Two important thyristor parameters are gate trigger current (I_{GT}) and gate trigger voltage (V_{GT}).

I_{GT} (Gate Trigger Current) is the amount of gate trigger current required to turn the device on. I_{GT} has a negative temperature coefficient — that is, the trigger current required to turn the device on increases with decreasing temperature. If the TRIAC must operate over a wide temperature range, its I_{GT} requirement could double at the low temperature extreme from that of its 25°C rating.

It is good practice, if possible, to trigger the thyristor with three to ten times the I_{GT} rating for the device. This increases its di/dt capability and ensures adequate gate trigger current at low temperatures.

V_{GT} (Gate Trigger Voltage) is the voltage the thyristor gate needs to ensure triggering the device on. This voltage is needed to overcome the input threshold voltage of the device. To prevent thyristor triggering, gate voltage should be kept to approximately 0.4 V or less.

Like I_{GT}, V_{GT} increases with decreasing temperature.

INDUCTIVE LOAD SWITCHING

Switching of inductive loads, using TRIACs, may require special consideration in order to avoid false triggering. This false-trigger mechanism is illustrated in Figure 6.47 which shows an inductive circuit together with the accompanying waveforms.

Table 6.VII. TRIACs with Various Current Ratings

Sensitive Gate TRIACs	
TRIAC	**$I_{T(rms)}$**
MAC97, 97A, 97B	0.6 A
2N6068A	4 A
MAC228, A Series	8 A
Non-sensitive Gate TRIACs	
TRIAC	**$T_{T(rms)}$**
MAC91, A Series	0.6
2N6071-75	4
2N6342-49	8
2N6342A-49A	12
MAC15A, 15AFP Series	15
MAC223A, 223AFP Series	25
2N6160-65	30
2N5444-46	40

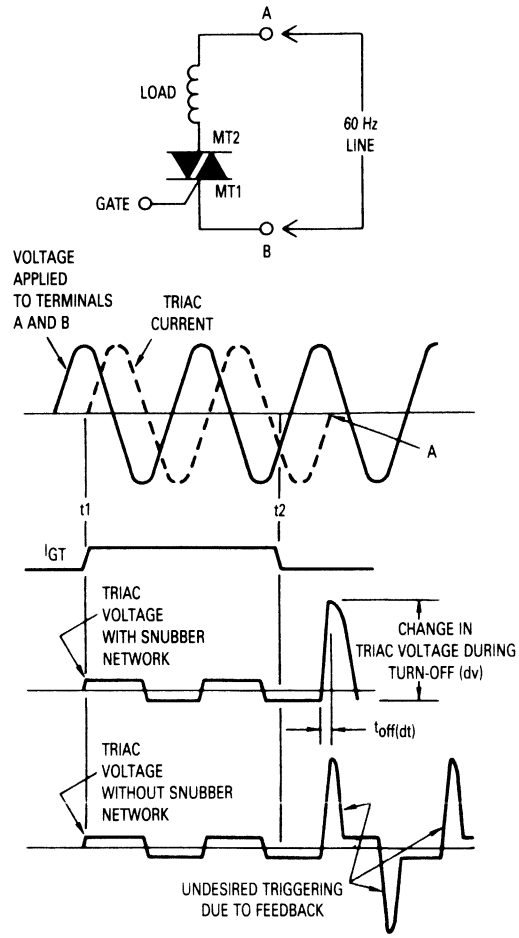


Figure 6.47. Inductive Load TRIAC Circuit and Equivalent Waveforms

As shown, the TRIAC is triggered on, at t1, by the positive gate current (I_{GT}). At that point, TRIAC current flows and the voltage across the TRIAC is quite low since the TRIAC resistance, during conduction, is very low.

From point t1 to t2 the applied I_{GT} keeps the TRIAC in a conductive condition, resulting in a continuous sinusoidal current flow that lags the applied voltage by 90° for this pure inductive load.

At t2, I_{GT} is turned off, but TRIAC current continues to flow until it reaches a value that is less than the sustaining current (I_H), at point A. At that point, TRIAC current is cut off and TRIAC voltage is at a maximum. Some of that voltage is fed back to the gate via the internal capacitance (from MT2 to gate) of the TRIAC.

TTL-TO-THYRISTOR INTERFACE

The subject of interfacing requires a knowledge of the output characteristics of the driving stages as well as the input requirements of the load. This section describes the driving capabilities of some of the more popular TTL circuits and matches these to the input demands of thyristors under various practical operating conditions.

TTL CIRCUITS WITH TOTEM-POLE OUTPUTS (e.g. 5400 SERIES)

The configuration of a typical totem-pole connected TTL output stage is illustrated in Figure 6.48(a). This stage is capable of "sourcing" current to a load, when the load is connected from V_{out} to ground, and of "sinking" current from the load when the latter is connected from V_{out} to V_{CC}. If the load happens to be the input circuit of a TRIAC (gate to MT_1), the TRIAC will be operating in quadrants I and IV (gate goes positive) when connected from V_{out} to ground, and of "sinking" II and III (gate goes negative) when connected from V_{out} to V_{CC}.

QUADRANT I-IV OPERATION

Considering first the gate-positive condition, Figure 6.48(b), the operation of the circuit is as follows:

When V_{in} to the TTL output stage is low (logical "zero"), transistors Q1 and Q3 of that stage are cut off, and Q2 is conducting. Therefore, Q2 sources current to the thyristor, and the thyristor would be triggered on during the $V_{in} = 0$ condition.

When V_{in} goes high (logical "one"), transistors Q1 and Q3 are on and Q2 is off. In this condition depicted by the equivalent circuit transistor Q3 is turned on and its collector voltage is, essentially, $V_{CE(sat)}$. As a result, the TRIAC is clamped off by the low internal resistance of Q3.

QUADRANT II-III OPERATION

When the TRIAC is to be operated in the more sensitive quadrants II and III (negative-gate turn-on), the circuit in Figure 6.49(a) may be employed.

With Q3 in saturation, as shown in the equivalent circuit of 6.49(b), its saturation voltage is quite small, leaving virtually the entire $-V_{EE}$ voltage available for thyristor turn-on. This could result in a TRIAC gate current that exceeds the current limit of Q3, requiring a current-limiting series resistor, ($R_{(lim)}$).

When the V_{out} level goes high, Q3 is turned off and Q2 becomes conductive. Under those conditions, the TRIAC gate voltage is below V_{GT} and the TRIAC is turned off.

DIRECT-DRIVE LIMITATIONS

With sensitive-gate TRIACs, the direct connection of a TRIAC to a TTL circuit may sometimes be practical. However, the limitations of such circuits must be recognized.

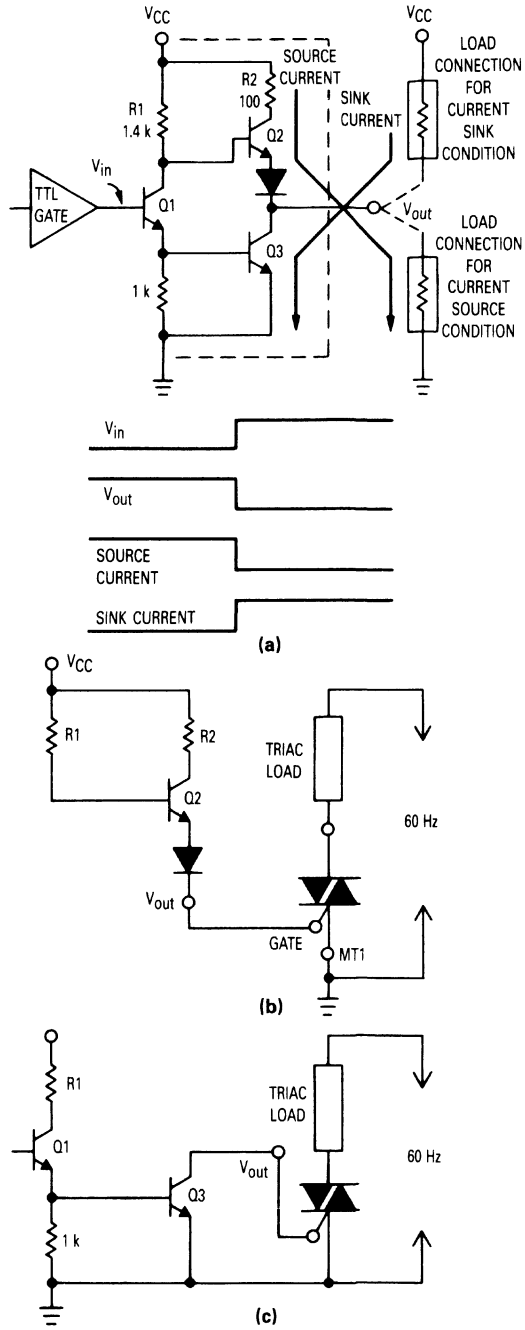


Figure 6.48. Totem-Pole Output Circuit TTL Logic, Together with Voltage and Current Waveforms, (b) Equivalent Circuit for Triggering TRIAC with a Positive Voltage — TRIAC-On Condition, (c) TRIAC-Off Condition

For example:

For TTL circuits, the "high" logic level is specified as 2.4 volts. In the circuit of Figure 6.48(a), transistor Q2 is capable of supplying a short-circuit output current (I_{SC}) of 20 to 55 mA (depending on the tolerances of R1 and R2, and on the h_{FE} of Q2). Although this is adequate to turn a sensitive-gate TRIAC on, the specified 2.4 volt (high) logic level can only be maintained if the sourcing current is held to a maximum of 0.4 mA — far less than the current required to turn on any thyristor. Thus, the direct conneciton is useful only if the driver need not activate other logic circuits in addition to a TRIAC.

A similar limiting condition exists in the Logic "0" condition of the output, when the thyristor is to be clamped off. In this condition, Q3 is conducting and V_{out} equals the saturation voltage ($V_{CE(sat)}$) of Q3. TTL specifications indicate that the low logic level (logic "0") may not exceed 0.4 volts, and that the sink current must be limited to 16 mA in order not to exceed this value. A higher value of sink current would cause ($V_{CE(sat)}$) to rise, and could trigger the thyristor on.

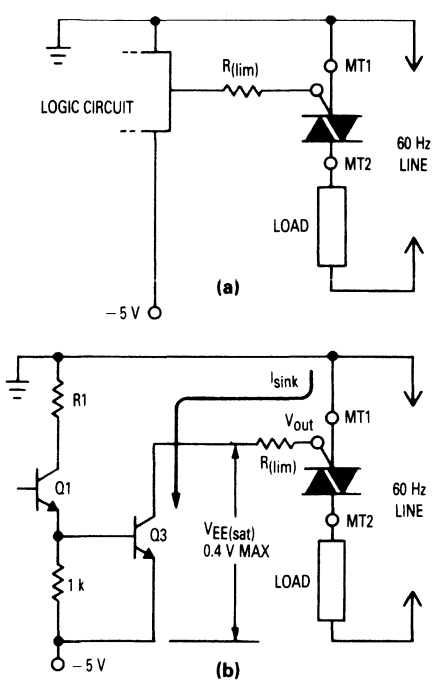


Figure 6.49. TTL Circuit for Quadrant II and III TRIAC Operation Requiring Negative V_{GT}, (b) Schematic Illustrates TRIAC Turn-On Condition, V_{out} = Logical "0"

CIRCUIT DESIGN CONSIDERATIONS

Where a 5400-type TTL circuit is used solely for controlling a TRIAC, with positive-gate turn-on (quadrants I-IV), a sensitive gate TRIAC may be directly coupled to the logic output, as in Figure 6.48. If the correct logic levels must be maintained, however, a couple of resistors must be added to the circuit, as in Figure 6.50(a). In this diagram, R1 is a pull-up which allows the circuit to source more current during a high logical output. Its value must be large enough, however, to limit the sinking current below the 16 mA maximum when V_{out} goes low so that the logical zero level of 0.4 volts is not exceeded.

Resistor R2, a voltage divider in conjunction with R1, insures V_{OH} (the "high" output voltage) to be 2.4 V or greater.

The resistor values may be calculated as follows:

For a supply voltage of 5 V and a maximum sinking current of 16 mA

$$R_1 \geqslant V_{CC}/16\text{ mA} \geqslant 5/0.016 \geqslant 312\ \Omega$$

Thus, 330 Ω, 1/4 W resistor may be used. Assuming R_1 to be 330 Ω and a thyristor gate on voltage (V_{GT}) of 1 V, the equivalent circuit of Figure 6.50(b) exists during the logical "1" output level. Since the logical "1" level must be maintaned at 2.4 volts, the voltage drop across R_2 must be 1.4 V. Therefore,

$$R_2 = 1.4/I_R = 1.4/V_{R_1}/R_2 = 1.4/(2.6/330) \cong 175\ \Omega$$

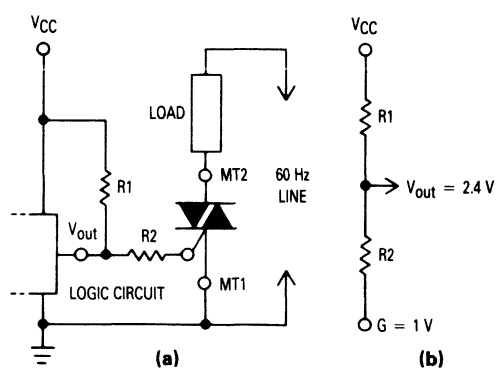


Figure 6.50. Practical Direct-Coupled TTL TRIAC Circuit; (b) Equivalent Circuit Used for Calculation of Resistor Values

A 180 Ω resistor may be used for R_2. If the V_{GT} is less than 1 volt, R_2 may need to be larger.

The MAC97A and 2N6071A TRIACs are compatible devices for this circuit arrangement, since they are guaranteed to be triggered on by 5 mA, whereas the current through the circuit of Figure 6.50(b) is approximately 8 mA, (V_{R1}/R_1).

When the TRIAC is to be turned on by a negative gate voltage, as in Figure 6.49(b), the purpose of the limiting resistor $R_{(lim)}$ is to hold the current through transistor Q3 to 16 mA. With a 5 V supply, a TRIAC V_{GT} of 1 V and a maximum sink current of 16 mA

$$R_{(lim)} = (V_{CC} - V_{GT})/I_{sink} = (5 - 1)/0.016 \geq 250\ \Omega$$

In practice, a 270 Ω, 1/4 W resistor may be used.

1

OPEN COLLECTOR TTL CIRCUIT

The output section of an open-collector TTL gate is shown in Figure 6.51(a).

A typical logic gate of this kind is the 5401 type Q2-input NAND gate circuit. This logic gate also has a maximum sink current of 16 mA (V_{OL} = 0.4 V max.) because of the Q1 (sat) limitations. If this logic gate is to source any current, a pull-up-collector resistor, R_1 (6.51b) is needed. When this TTL gate is used to trigger a thyristor, R_1 should be chosen to supply the maximum trigger current available from the TTL circuit (≈ 16 mA, in this case). The value of R_1 is calculated in the same way and for the same reasons as in Figure 6.50. If a logical "1" level must be maintained at the TTL output (2.4 V min.), the entire circuit of Figure 6.50 should be used.

For direct drive (logical "0") quadrants II and III triggering, the open collector, negative supplied (−5 V) TTL circuit of Figure 6.52 can be used. Resistor R_1 can have a value of 270 Ω, as in Figure 6.49. Resistor R_2 ensures that the TRIAC gate is referenced to MT1 when the TTL gate goes high (off), thus preventing unwanted turn-on. An R_2 value of about 1 k should be adequate for sensitive gate TRIACs and still draw minimal current.

Circuits utilizing Schottky TTL are generally designed in the same way as TTL circuits, although the current source/sink capabilities may be slightly different.

TRIGGERING THYRISTORS FROM LOGIC GATES USING INTERFACE TRANSISTORS

For applications requiring thyristors that demand more gate current than a direct-coupled logic circuit can supply, an interface device is needed. This device can be a small-signal transistor or an opto coupler.

The transistor circuits can take several different configurations, depending on whether a series or shunt switch design is chosen, and whether gate-current sourcing (quadrants I and IV) or sinking (quadrants II and III) is selected. An example of a series switch, high output (logic 1) activation, is shown in Figure 6.53. Any logic family can be used as long as the output characteristics are known. The NPN interface transistor, Q1, is configured in the common-emitter mode — the simplest approach — with the emitter connected directly to the gate of the thyristor.

Depending on the logic family used, resistor R_1 (pull-up resistor) and R_3 (base-emitter leakage resistor) may or may not be required. If, for example, the logic is a typical TTL totem-pole output gate that must supply 5 mA to the base of the NPN transistor and still maintain a "high" (2.4 V) logic output, then R_1 and R_2 are required. If the "high" logic level is not required, then the TTL circuit can directly source the base current, limited by resistor R_2.

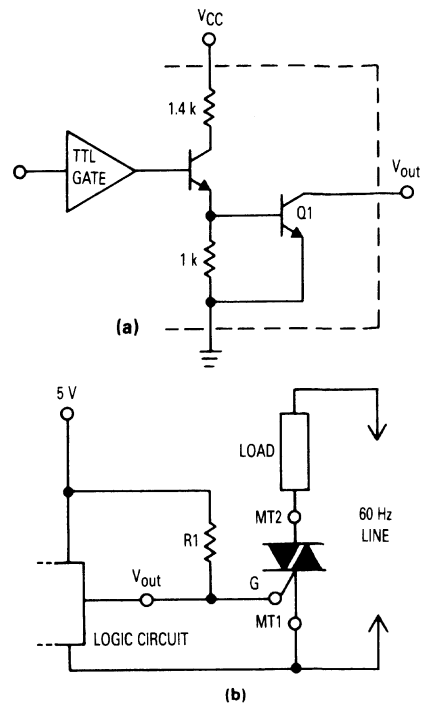


Figure 6.51. Output Section of Open-Collector TTL, (b) For Current Sourcing, A Pull-up Resistor, R1, Must Be Added

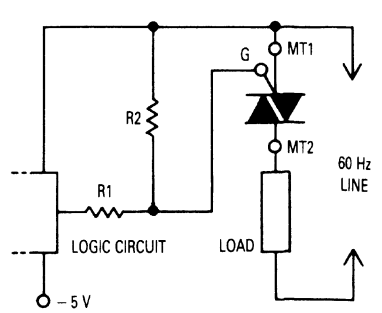


Figure 6.52. Negative-Supplied (−5 V) TTL Gate Permits TRIAC Operation in Quadrants II and III

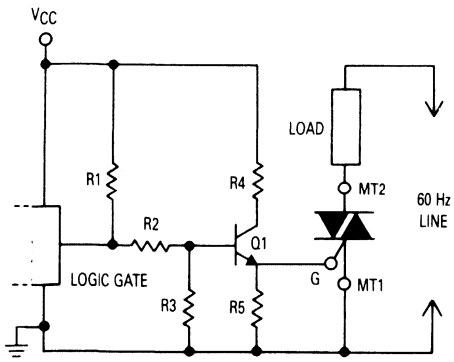


Figure 6.53. Series Switch, High Output (Logic "1")

To illustrate this circuit, consider the case where the selected TRIAC requires a positive-gate current of 100 mA. The interface transistor, a popular 2N4401, has a specified minimum h_{FE} (at a collector current of 150 mA) of 100. To ensure that this transistor is driven hard into saturation, under "worse case" (low temperature) conditions, a forced h_{FE} of 20 is chosen — thus, 5 mA of base current. For this example, the collector supply is chosen to be the same as the logic supply (+ 5 V); but for the circuit configuration, it could be a different supply, if required. The collector-resistor, R_4, is simply

$$R_4 = (V_{CC} - V_{CE(sat)} - V_{GT(typ)})/I_{GT}$$
$$= (5 - 1 - 0.9)/100 \text{ mA} = 40\ \Omega.$$

A 39 ohm, 1 W resistor is then chosen, since its actual dissipation is about 0.4 W.

If the "logic 1" output level is not important, then the base limiting resistor R_2 is required, and the pull-up resistor R_1 is not. Since the collector resistor of the TTL upper totem-pole transistor, Q2, is about 100 Ω, this resistor plus R_2 should limit the base current to 5 mA.

Thus R_2 calculates to

$$R_2 = [(V_{CC} - V_{BE} - V_{GT})/5 \text{ mA}] - 100\ \Omega$$
$$= [(5 - 0.7 - 0.9)/0.005]\ 100\ \Omega$$
$$\approx 560\ \Omega \text{ (specified)}$$

When the TTL output is low, the lower transistor of the totem-pole, Q3, is a clamp, through the 560 Ω resistor, across the 2N4401; and, since the 560 Ω resistor is relatively low, no leakage-current shunting resistor, R_3, is required.

In a similar manner, if the TTL output must remain at "logic 1" level, the resistor R_1 can be calculated as described earlier (R_3 may or may not be required).

For low-logic activation (logic "0"), the circuit of Figure 6.54 can be used. In this example, the PNP-interface transistor 2N4403, when turned on, will supply positive-gate current to the thyristor. To ensure that the high logic level will keep the thyristor off, the logic gate and the transistor emitter must be supplied with the same power supply. The base resistors, as in the previous example, are dictated by the output characteristics of the logic family used. Thus if a TTL gate circuit is used, it must be able to sink the base current of the PNP transistor ($I_{OL(MAX)}$ = 16 mA).

When thyristor operation in quadrants II and III is desired, the circuits of Figures 6.55 and 6.56 can be used; Figure 6.55 is for high logic output activation and Figure 6.56 is for low. Both circuits are similar to those on Figures 6.53 and 6.54, but with the transistor polarity and power supplies reversed.

Figure 6.55 sinks current from the thyristor gate through a switched NPN transistor whose emitter is referenced to a negative supply. The logic circuit must also be referenced to this negative supply to ensure that transistor Q1 is turned off when required; thus, for TTL gates, V_{EE} would be −5 V.

In Figure 6.56, the logic-high bus, which is now ground, is the common ground for both the logic, and the thyristor and the load. As in the first example (Figure 6.53), the negative supply for the logic circuit ($-V_{EE}$) and the collector supply for the PNP transistor need not be the same supply. If, for power-supply current limitations, the collector supply is chosen to be another supply ($-V_{CC}$), it must be within the V_{CEO} ratings of the PNP transistor.

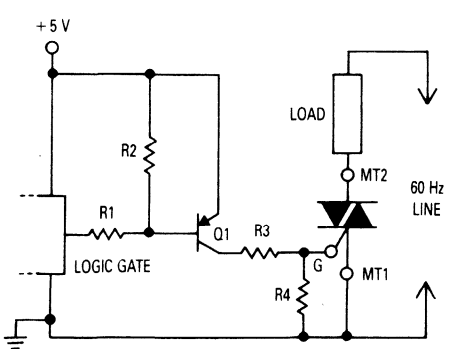


Figure 6.54. Low-Logic Activation with Interface Transistor

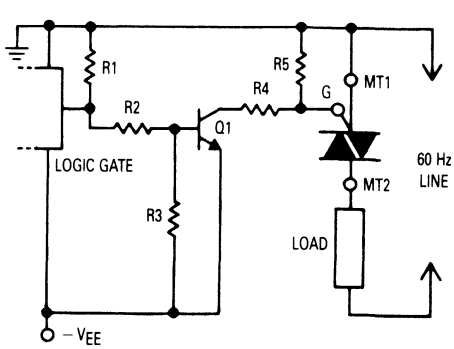


Figure 6.55. High-Logic Output Activation

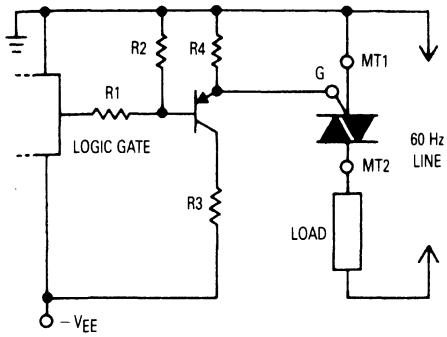


Figure 6.56. Low-Logic Output Activation

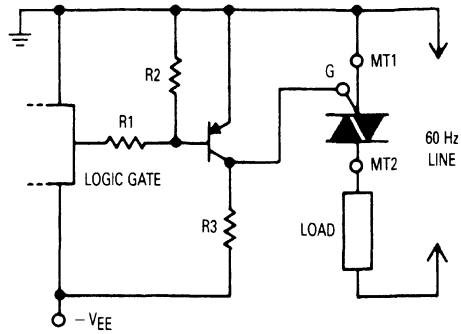


Figure 6.58. Shunt-Interface Circuit (Quadrants I and III Operation)

Also, the power dissipation of collector resistor, R3, is a function of $-V_{CC}$ — the lower $-V_{CC}$, the lower the power rating.

The four examples shown use gate-series switching to activate the thyristor and load (when the interface transistor is off, the load is off). Shunt-switching can also be used if the converse is required, as shown in Figures 6.57 and 6.58. In Figure 6.57, when the logic output is high, NPN transistor, Q1, is turned on, thus clamping the gate of the thyristor off. To activate the load, the logic output goes low, turning off Q1 and allowing positive gate current, as set by resistor R3, to turn on the thyristor.

In a similar manner, quadrant's II and III operation is derived from the shunt interface circuit of Figure 6.58.

OPTICAL ISOLATORS/COUPLERS

An Optoelectronic isolator combines a light-emitting device and a photo detector in the same opaque package that provides ambient light protection. Since there is no electrical connection between input and output, and the emitter and detector cannot reverse their roles, a signal can pass through the coupler in one direction only.

Since the opto-coupler provides input circuitry protection and isolation from output-circuit conditions, ground-loop prevention, dc level shifting, and logic control of high voltage power circuitry are typical areas where opto-couplers are useful.

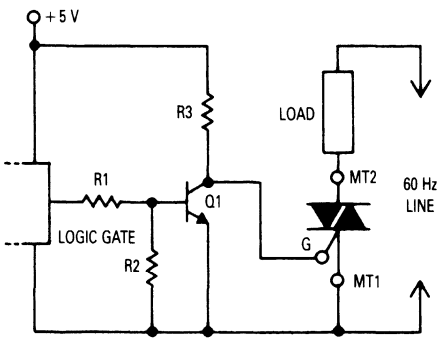


Figure 6.57. Shunt-Interface Circuit (High-Logic Output)

Figure 6.59 shows a photo-TRIAC used as a driver for a higher-power TRIAC. The photo-TRIAC is light sensitive and is turned on by a certain specified light density (H), which is a function of the LED current. With dark conditions (LED current = 0) the photo-TRIAC is not turned on, so that the only output current from the coupler is leakage current, called peak-blocking current (I_{DRM}). The coupler is bilateral and designed to switch ac signals.

The photo-TRIAC output current capability is, typically, 100 mA, continuous, or 1 A peak.

Any Motorola TRIAC can be used in the circuit of Figure 6.59 by using Table 6.VII. The value of R is based on the photo-TRIAC's current-handling capability. For example, when the MOC3011 operates with a 120 V line voltage (approximately 175 V peak), a peak I_{GT} current of 175 V/180 ohm (approximately 1 A) flows when the line voltage is at its maximum. If less than 1 A of I_{GT} is needed, R can be increased. Circuit operation is as follows:

Table 6.VII. Specifications for Typical Optically Coupled TRIAC Drivers

Device Type	Maximum Required LED Trigger Current (mA)	Peak Blocking Voltage	R(Ohms)
MOC3009	30	250	180
MOC3011	15	250	180
MOC3011	10	250	180
MOC3020	30	400	260
MOC3021	15	400	360
MOC3030	30	250	51
MOC3031	15	250	51

When an op-amp, logic gate, transistor or any other appropriate device turns on the LED, the emitted light triggers the photo-TRIAC. Since, at this time, the main TRIAC is not on, MT2-to-gate is an open circuit. The 60 Hz line can now cause a current flow via R, the photo-TRIAC, Gate-MT1 junction and load. This Gate-MT1 current triggers the main TRIAC, which then shorts and turns

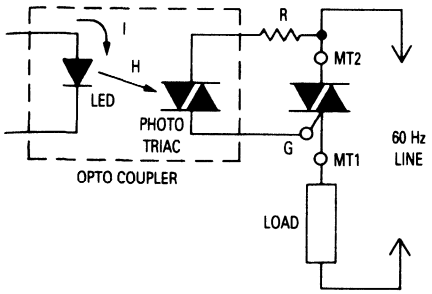


Figure 6.59. Optically-Coupled TRIAC Driver is Used to Drive a Higher-Power TRIAC

off the photo-TRIAC. The process repeats itself every half cycle until the LED is turned off.

Triggering the main TRIAC is thus accomplished by turning on the LED with the required LED-trigger current indicated in Table 6.VII.

MICROPROCESSORS

Microprocessor systems are also capable of controlling ac power loads when interfaced with thyristors. Commonly, the output of the MPU drives a PIA (peripheral interface adaptor) which then drives the next stage. The PIA Output Port generally has a TTL compatible output with significantly less current source and sink capability than standard TTL. (MPUs and PIAs are sometimes constructed together on the same chip and called microcontrolllers.)

When switching ac loads from microcomputers, it is good practice to optically isolate them from unexpected load or ac line phenomena to protect the computer system from possible damage. In addition, optical isolation will make UL recognition possible.

A typical TTL-compatible microcontroller, such as the MC3870P offers the following specifications:

I_{OH} = 300 μA (V_{OH} = 2.4 V)
I_{OL} = 1.8 mA (V_{OL} = 0.4 V)
V_{CC} = 5 V

Since this is not adequate for driving the optocoupler directly (10 mA for the MOC3011), an interface transistor is necessary.

The circuit of Figure 6.60 may be used for thyristor triggering from the 3870 logical "1."

The interface transistor, again, can be the 2N4401. With 10 mA of collector current (for the MOC3011) and a base current of 0.75 mA, the $V_{CE(sat)}$ will be approximately 0.1 V.

R_1 can be calculated as in a previous example. Specifically:

1.8 mA (maximum I_{OL} for the 3870)
$> 5\ V/R_1$; $R_1 > 2.77$ k

R_1 can be 3 k, 1/4 W

With a base current of 0.75 mA, R_1 will drop (0.75 mA) (3 k) or 2.25 V. This causes a V_{OH} of 2.75 V, which is within the logical "1" range.

$R_2 = [2.75\ V - V_{BE(on)}]/I_B = (2.75 - 0.75)/0.75 = 2.66$ k

R_2 can be a 2.7 k, 1/4 W resistor.

R_3 must limit I_C to 10 mA:

$$R_3 = [5\ V - V_{CE(sat)} - V_F(\text{diode})/10\ \text{mA}]$$
$$= (5 - 0.1 - 1.2)/10\ \text{mA} = 370\ \Omega$$

Since R_3 is relatively small, no base-emitter leakage resistor is required.

Figure 6.61 shows logical "0" activation. Resistor values are calculated in a similar way.

THE CMOS INTERFACE

Another popular logic family, CMOS, can also be used to drive thyristors.

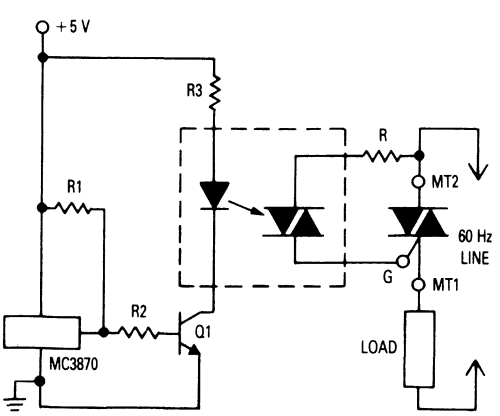


Figure 6.60. Logical "1" Activation from MC3870P Microcomputer

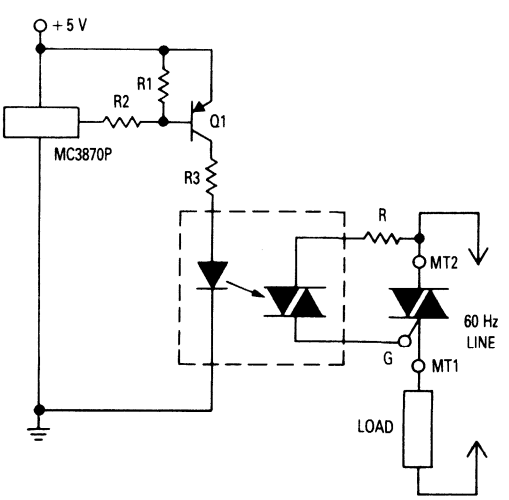


Figure 6.61. Logical "0" Activation

As shown in Figure 6.62(a), the output stage of a typical CMOS Gate consists of a P-channel MOS device connected in series with an N-channel device (drain-to-drain), with the gates tied together and driven from a common input signal. When the input signal goes high, logical 1, the P-channel device is essentially off and conducts only leakage current (I_{DSS}), on the order of picoamps. The N-channel unit is forward-biased and, although it has a relatively high on resistance ($r_{DS(on)}$), the drain-to-source voltage of the N-channel device (V_{DS}) is very low (essentially zero) because of the very low drain current (V_{DSS}) flowing through the device. Conversely, when the input goes low (zero), the P-channel device is turned fully on, the N-channel device is off and the output voltage will be very near V_{DD}.

When interfacing with transistors or thyristors, the CMOS Gate is current-limited mainly by its relatively high on resistance, the dc resistance between drain and source, when the device is turned on.

The equivalent circuits for sourcing and sinking current into an external load is shown in Figures 6.62(b) and 6.62(c). Normally, when interfacing CMOS to CMOS, the logic outputs will be very near their absolute maximum states (V_{DD} or 0 V) because of the extremely small load currents. With other types of loads (e.g. TRIACs), the current, and the resulting output voltage, is dictated by the simple voltage divider of $r_{DS(on)}$ and the load resistor R_L, where $r_{DS(on)}$ is the total series and/or parallel resistance of the devices comprising the NOR and NAND function.

Interfacing CMOS gates with thyristors requires a knowledge of the on resistance of the gate in the source and sink conditions. The on-resistance of CMOS devices is not normally specified on data sheets.

It can easily be calculated, however, from the output drive currents, which are specified. The drive (source/sink) currents of typical CMOS gates at various supply voltages are shown in Table 6.VIII. From this information,

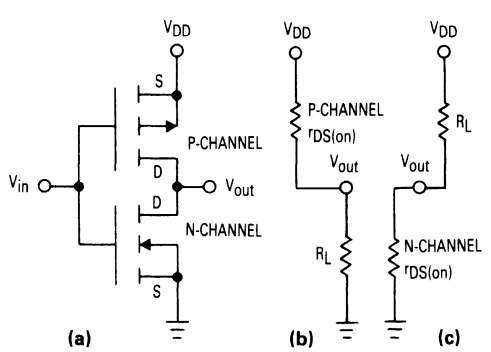


Figure 6.62. Output Section of a Typical CMOS Gate, (b) Equivalent Current-Sourcing Circuit is Activated when V_{in} goes Low, Turning the P-Channel Device Fully On, (c) Equivalent Current Sinking Circuit is Activated when the Input Goes High and Turns the N-Channel Device On

the on resistance for worst case design is calculated as follows:

For the source condition

$$r_{DS(on)(MAX)} = (V_{DD} - V_{OH})/I_{OH(MIN)}$$

Similarly, for the sink current condition

$$r_{DS(on)(MAX)} = V_{OL}/I_{OL(MIN)}$$

Values of $r_{DS(on)}$ for the various condition shown in Table 6.VIII are tabulated in Table 6.IX.

Table 6.VIII. CMOS Characteristics

Specified source/sink currents to maintain logical "1" and logical "0" levels for various power-supply (V_{DD}) voltages. The I_{OH} and I_{OL} values are used to calculate the "on" resistance of the CMOS output.

Output Drive Current	CMOS AL Series mA, dc		CMOSCL/CP Series mA, dc	
	Min	Typ	Min	Typ
$I_{(source)} - I_{OH}$				
V_{DD} = 5 V; V_{OH} = 2.5 V	−0.5	−1.7	−0.2	−1.7
V_{DD} = 10 V; V_{OH} = 9.5 V	−0.5	−0.9	−0.2	−0.9
V_{DD} = 15 V; V_{OH} = 13.5 V		−3.5		−3.5
$I_{(sink)} - I_{OL}$				
V_{DD} = 5 V; V_{OL} = 0.4 V	0.4	7.8	0.2	7.8
V_{DD} = 10 V; V_{OL} = 0.5 V	0.9	2	0.5	2
V_{DD} = 15 V; V_{OL} = 1.5 V		7.8		7.8

Table 6.IX
Calculated CMOS On Resistance Values For Current Sourcing and Sinking at Various V_{DD} Options

Operating Conditions	Output Resistance, $r_{DS(on)}$ Ohms	
	Typical	Maximum
Source Condition		
V_{DD} = 5 V	1.7 k	12.5 k
10 V	500	2.5 k
15 V	430	—
Sink Condition		
V_{DD} = 5 V	500	2 k
10 V	420	1 k
15 V	190	—

It is apparent from this table that the on resistance decreases with increasing supply voltage.

Although the minimum currents are now shown on the data sheet for the 15 V case, the maximum on resistance can be no greater than the 10 V example and, therefore, can be assumed for worst case approximation to be 1 and 2.5 kohms for sink-and-source current cases, respectively.

The sourcing on resistance is greater than the sinking case because the difference in carrier mobilities of the two channel types.

Since $r_{DS(on)}$ for both source and sink conditions var-

ies with supply voltage (V_{DD}), there are certain drive limitations. The relative high $r_{DS(on)}$ of the P-channel transistor could possibly limit the direct thyristor drive capability; and, in a like manner, the N-channel $r_{DS(on)}$ might limit its clamping capability. With a 10 or 15 V supply, the device may be capable of supplying more than 10 mA, but should be limited to that current, with an external limiting resistor, to avoid exceeding the reliable limits of the unit metalization.

DC MOTOR CONTROL WITH THYRISTORS

In order to control the speed of a dc series field motor at different required torque levels, it is necessary to adjust the voltage applied to the motor. For any particular applied voltage the motor speed is determined solely by the torque requirements and top speed is reached under minimum torque conditions. When a series motor is used as a traction drive for vehicles, it is desirable to control the voltage to the motor to fit the various torque requirements of grades, speed and load. The common method of varying the speed of the motor is by inserting resistance in series with the motor to reduce the supplied voltage. This type of motor speed control is very inefficient due to the I^2R loss, especially under high current and torque conditions.

A much more efficient method of controlling the voltage applied to the motor is the pulse width modulation method shown in Figure 6.63. In this method, a variable width pulse of voltage is applied to the motor at the same rate to proportionally vary the average voltage applied to the motor. A diode is placed in parallel with the inductive motor path to provide a circuit for the inductive motor current and prevent abrupt motor current change. Abrupt current changes would cause high induced voltage across the switching device.

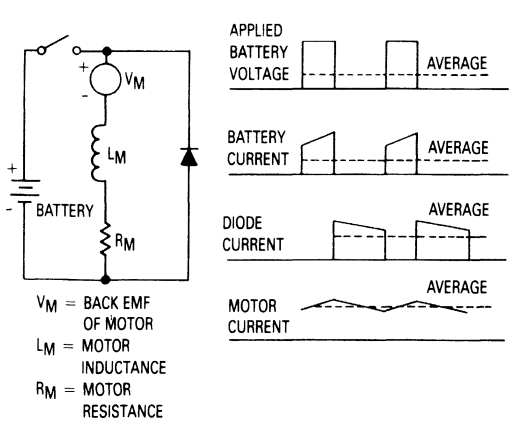


Figure 6.63. Basic Pulse Width Modulated Motor Speed Control

The circulating current through the diode decreases only in response to motor and diode loss. With reference to Figure 6.63, it can be seen that the circulating diode current causes more average current to flow through the motor than is taken from the battery. However, the power taken from the battery is approximately equal to the power delivered to the motor, indicating that energy is stored in the motor inductance at the battery voltage level and is delivered to the motor at the approximate current level when the battery is disconnected.

To provide smooth and quiet motor operation, the current variations through the motor should be kept to a minimum during the switching cycle. There are limitations on the amount of energy that can be stored in the motor inductance, which, in turn, limits the power delivered to the motor during the off time; thus the off time must be short. To operate the motor at low speeds, the on time must be approximately 10 percent of the off time and therefore, a rapid switching rate is required that is generally beyond the capabilities of mechanical switches. Practical solutions can be found by the use of semiconductor devices for fast, reliable and efficient switching operations.

SCR DC MOTOR CONTROL

SCRs offer several advantages over power transistors as semiconductor switches. They require less driver power, are less susceptible to damage by overload currents and can handle more voltage and current. Their disadvantages are that they have a higher power dissipation due to higher voltage drops and the difficulty in commutating to the off condition.

The SCR must be turned off by either interrupting the current through the anode-cathode circuit or by forcing current through the SCR in the reverse direction so that the net flow of forward current is below the holding current long enough for the SCR to recover blocking ability. Commutation of the SCR in high current motor control circuits is generally accomplished by discharging a capacitor through the SCR in the reverse direction. The value of this capacitor is determined approximately from the following equation:

$$C_c = \frac{T_q I_A}{V_c}$$

Where:

C_c = value of necessary commutating capacitance
T_q = turn-off time of the SCR
I_A = value of anode current before commutation
V_c = voltage of C_c before commutation

This relationship shows that to reduce the size of C_c, the capacitor should be charged to as high a voltage as possible and the SCR should be selected with as low a turn-off time as possible.

If a 20 microsecond turn-off time SCR is commutated by a capacitor charged to 36 volts, it would take over 110 μF to turn off 200 amperes in the RC commutating circuit of Figure 6.64. If a 50 cycle switching frequency is desired,

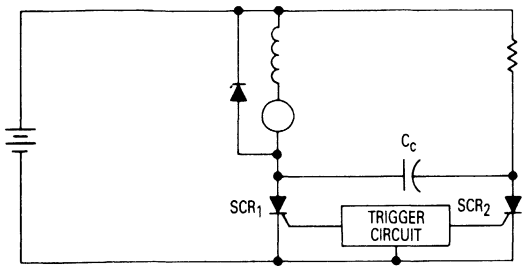


Figure 6.64. Speed Control with Resistive Charging

the value of R_1 would be approximately 5 ohms to allow charging time with an on duty cycle of 10 percent. The value of this resistor would give approximately 260 watts dissipation in the charging circuit with 90 percent off duty cycle.

If the resonant charging commutating circuitry of Figure 6.65 is used, the capacitor is reduced to approximately 55 μF. In this circuit, SCR_3 is gated on at the same time as SCR_1 and allows the resonant charging of C_C through L_C to twice the supply voltage. SCR_3 is then turned off by the reversal of voltage in the resonant circuit before SCR_2 is gated on. It is apparent that there is very little power loss in the charge circuit depending upon the voltage drop across SCR_3 and the resistance in L_C.

If the commutating capacitor is to be reduced further, it is necessary to use a transformer to charge the capacitor to more than twice the supply voltage. This type of circuit is illustrated by the transformer charge circuit shown in Figure 6.66. In this circuit the capacitor can be charged to several times the supply voltage by transformer action through diode D_1 before commutating SCR_1. The disadvantage of this circuit is in the high motor current that flows through the transformer primary winding.

HEAVY DUTY MOTOR CONTROL WITH SCRs

Another advantage of SCRs is their high surge current capabilities, demonstrated in the motor drive portion of the golf cart controller shown in Figure 6.67. Germanium power transistors were used because of the low saturation voltages and resulting low static power loss. However, since switching speeds are slow and leakage currents are high, additional circuit techniques are required to ensure reliable operation:

1) The faster turn-on time of the SCR (Q9) over that of the germanium transistors shapes the turn-on load line.
2) The parallelled output transistors (Q3–Q8) require a 6 V reverse bias.
3) The driver transistor Q2 obtains reverse bias by means of diode D4.

To obtain the 6 V bias, the 36 V string of 6 V batteries are tapped, as shown in the schematic. Thus, the motor is powered from 30 V and the collector supply for Q2 is 24 V, minimizing the dissipation in colllector load resistor R1.

Total switching loss in switchmode applications is the result of the static (on-state) loss, dynamic (switching) loss and leakage current (off-state) loss. The low saturation voltage of germanium transistors produces low static loss. However, switching speeds of the germanium transistors are low and leakage currents are high. Loss due to leakage current can be reduced with off bias, and load line shaping can minimize switching loss. The turn-off switching loss was reduced with a standard snubber network (D5, C1, R2) see Figure 6.67.

Turn-on loss was uniquely and substantially reduced by using a parallel connected SCR (across the germanium transistors) the MCR265-4 (55 A rms, 550 A surge). This faster switching device diverts the initial turn-on motor load current from the germanium output transistors, reducing both system turn-on loss and transistor SOA stress.

The main point of interest is the power switching portion of the PWM motor controller. Most of the readily available PWM ICs can be used (MC3420, MC34060, TL494, SG1525A, UA78S40, etc.), as they can source at

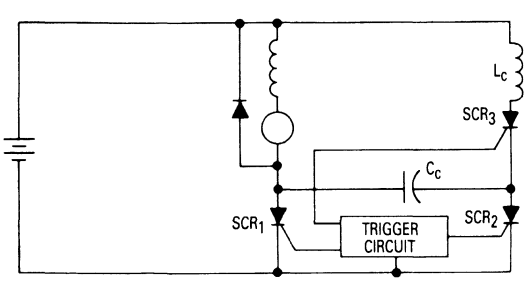


Figure 6.65. Speed Control with Inductive Charging

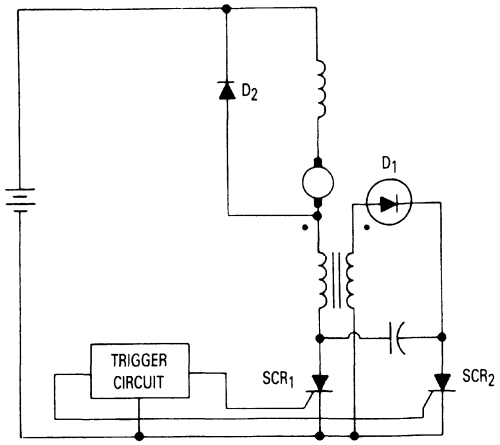


Figure 6.66. SCR Motor Control with Transformer Charging

least a 10 mA, +15 V pulse for driving the following power MOSFET.

Due to the extremely high input impedance of the power MOSFET, the PWM output can be directly connected to the FET gate, requiring no active interface circuitry. The positive going output of the PWM is power gained and inverted by the TMOS FET Q1 to supply the negative going base drive to PNP transistor Q2. Diode D1 provides off-bias to this paraphase amplifier, the negative going pulse from the emitter furnishing base drive to the six parallel connected output transistors and the positive going collector output pulse supplying the SCR gate trigger coupled through transformer T1.

Since the faster turn-on SCR is triggered on first, it will carry the high, initial turn-on motor current. Then the slower turn-on germanium transistors will conduct clamping off the SCR, and carry the full motor current. For the illustrated 2HP motor and semiconductors, a peak exponentially rising and falling SCR current pulse of 120 A lasting for about 60 μs was measured. This current is well within the rating of the SCR. Thus, the high turn-on stresses are removed from the transistors providing a much more reliable and efficient motor controller while using only a few additional components.

DIRECTION AND SPEED CONTROL FOR MOTORS

For a shunt motor, a constant voltage should be applied to the shunt field to maintain constant field flux so that the armature reaction has negligible effect. When constant voltage is applied to the shunt field, the speed is a direct function of the armature voltage and the armature current. If the field is weak, then the armature reaction may counterbalance the voltage drop due to the brushes, windings and armature resistances, with the net result of a rising speed-load characteristic.

The speed of a shunt-wound motor can be controlled with a variable resistance in series with the field or the armature. Varying the field current for small motor provides a wide range of speeds with good speed regulation. However, if the field becomes extremely weak, a rising speed-load characteristic results. This method cannot provide control below the design motor speed. Varying the resistance in series with the armature results in speeds less than the designed motor speed; however, this method yields poor speed regulation, especially at low speed settings. This method of control also increases power dissipation and reduces efficiency and the torque since the maximum armature current is reduced. Neither type of resistive speed control is very satisfactory. Thyristor drive controls, on the other hand, provide continuous control through the range of speed desired, do not have the power losses inherent in resistive circuits, and do not compromise the torque characteristics of motors.

Although a series-wound motor can be used with either dc or ac excitation, dc operation provides superior performance. A universal motor is a small series-wound mo-

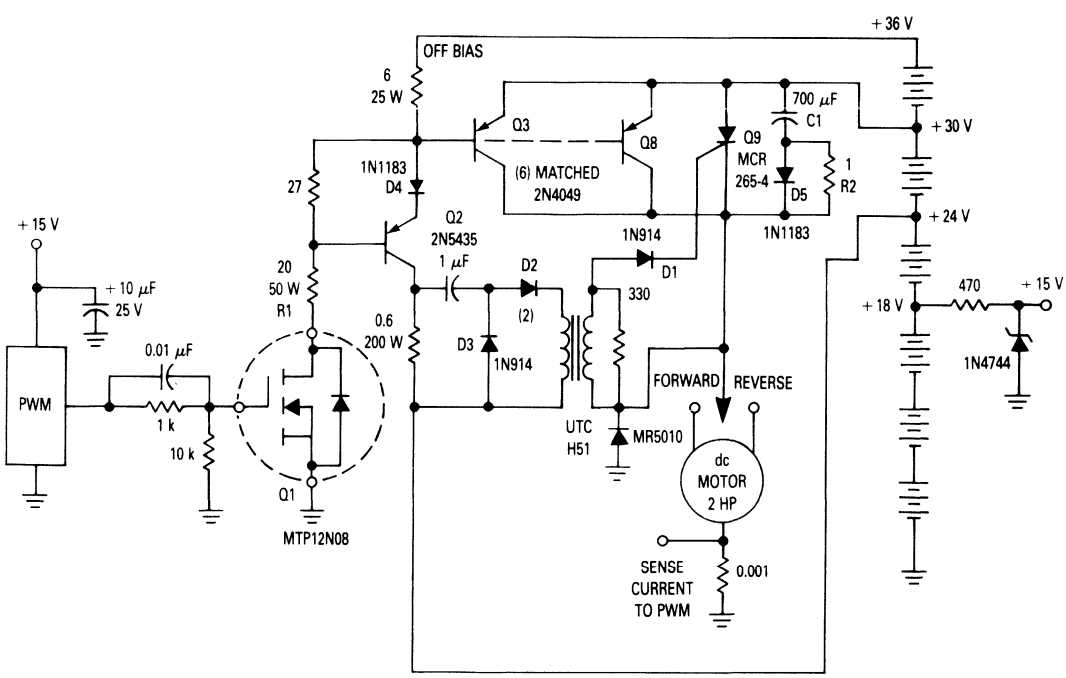


Figure 6.67. PWM DC Motor Controller Using SCR Turn-On Feature

tor designed to operate from either a dc or an ac supply of the same voltage. In the small motors used as universal motors, the winding inductance is not large enough to produce sufficient current through transformer action to create excessive commutation problems. Also, high-resistance brushes are used to aid commutation. The characteristics of a universal motor operated from alternating current closely approximate those obtained for a dc power source up to full load; however, above full load the ac and dc characteristics differ. For a series motor that was not designed as a universal motor, the speed-torque characteristic with ac rather than dc is not as good as that for the universal motor. At eight loads, the speed for ac operation may be greater than for dc since the effective ac field strength is smaller than that obtained on direct current. At any rate, a series motor should not be operated in a no-load condition unless precaution is are taken to limit the maximum speed.

1

SERIES-WOUND MOTORS

The circuit shown in Figure 6.68 can be used to control the speed and direction of rotation of a series-wound dc motor. Silicon controlled rectifiers Q1–Q4, which are connected in a bridge arrangement, are triggered in diagonal pairs. Which pair is turned on is controlled by switch S1 since it connects either coupling transformer T1 or coupling transformer T2 to a pulsing circuit. The current in the field can be reversed by selecting either SCRs Q2 and Q3 for conduction, or SCRs Q1 and Q4 for conduction. Since the armature current is always in the same direction, the field current reverses in relation to the armature current, thus reversing the direction of rotation of the motor.

A pulse circuit is used to drive the SCRs through either transformer T1 or T2. The pulse required to fire the SCR is obtained from the energy stored in capacitor C1. This capacitor charges to the breakdown voltage of zener diode D5 through potentiometer R1 and resistor R2. As the capacitor voltage exceeds the zener voltage, the zener conducts, delivering current to the gate of SCR Q5. This turns Q5 on, which discharges C1 through either T1 or T2 depending on the position of S1. This creates the desired triggering pulse. Once Q5 is on, it remains on for the duration of the half cycle. This clamps the voltage across C1 to the forward voltage drop of Q5. When the supply voltage drops to zero, Q5 turns off, permitting C1 to begin charging when the supply voltage begins to increase.

The speed of the motor can be controlled by potentiometer R1. The larger the resistance in the circuit, the longer required to charge C1 to the breakdown voltage of zener D5. This determines the conduction angle of either Q1 and Q4, or Q2 and Q3, thus setting the average motor voltage and thereby the speed.

SHUNT-WOUND MOTORS

If a shunt-wound motor is to be used, then the circuit in Figure 6.69 is required. This circuit operates like the one shown in Figure 6.68. The only differences are that the field is placed across the rectified supply and the armature is placed in the SCR bridge. Thus the field current is unidirectional but armature current is reversible; consequently the motor's direction of rotation is reversible. Potentiometer R1 controls the speed as explained previously.

RESULTS

Excellent results were obtained when these circuits were used to control 1/15 hp, 115 V, 5,000 r/min motors. This circuit will control larger, fractional-horsepower motors provided the motor current requirements are within the semiconductor ratings. Higher current devices will

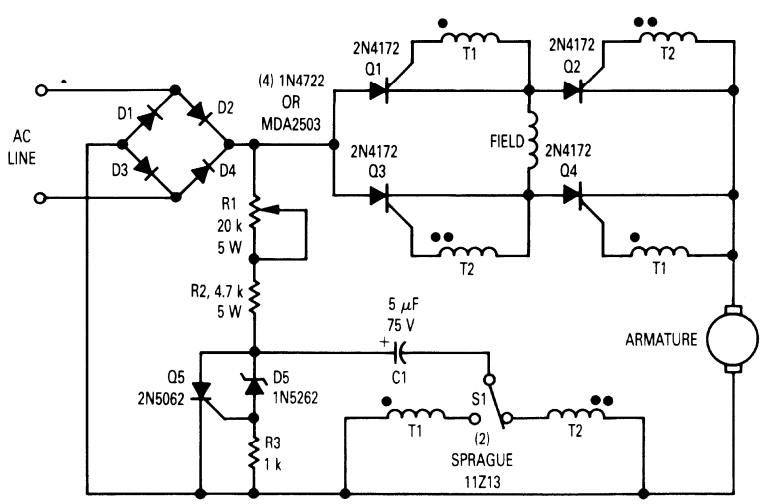


Figure 6.68. Direction and Speed Control for Series-Wound or Universal Motor

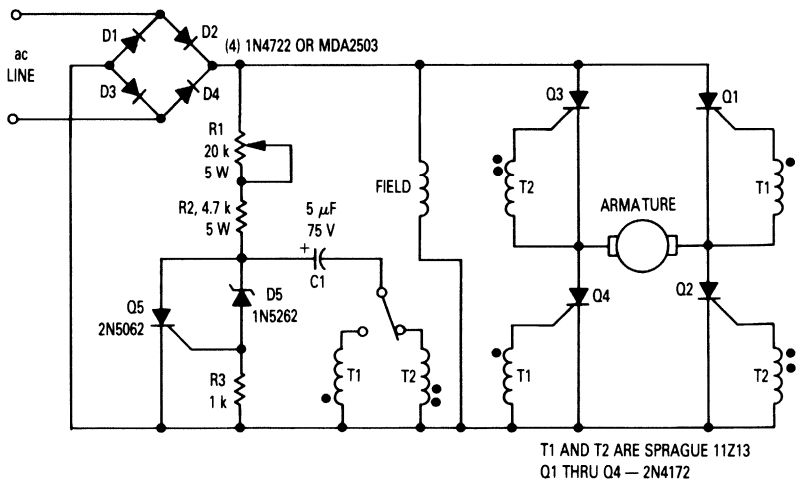


Figure 6.69. Direction and Speed Control for Shunt-Wound Motor

permit control of even larger motors, but the operation of the motor under worst case must not cause anode currents to exceed the ratings of the semiconductor.

UNIJUNCTION TRANSISTOR APPLICATIONS USING RELAXATION OSCILLATORS

Most UJT oscillator circuits employ the basic relaxation oscillator circuit in some way or another. As mentioned previously, either the output at base-one, base-two, or the emitter can be utilized in order to fulfill a specified requirement.

THE BASIC UJT RELAXATION OSCILLATOR CIRCUIT

The UJT relaxation oscillator, the basic building block in most UJT timer and oscillator circuits (Figure 6.70), operates as follows:

When power is applied, the capacitor C_E charges exponentially through the resistor R_E until the voltage on the capacitor equals the emitter firing voltage V_P. At this voltage, the emitter base-one junction becomes forward biased and the emitter characteristic goes into the negative resistance region. The capacitor C_E discharges through the emitter and a positive going pulse will be available at base-one. This pulse is shown in Figure 6.71(a) for a circuit having

R_E = 10 kΩ, C_E = 0.01 μF, R2 = 200 Ω, R1 = 47 Ω, and V1 = 20 V.

Prior to firing, a current I_{B2} is flowing from base-two to base-one. When emitter current starts to flow, this current will increase to $I_{B2(mod)}$ since the resistance from base-two to ground is decreasing. A negative going voltage pulse will therefore appear at base-two, and this waveform is shown in Figure 6.71(b).

When the voltage at the emitter has decreased to V_0, a voltage approximately equal to the valley voltage when R1 is purely resistive, the UJT will turn off if R_E meets certain conditions. C_E will start to charge up again, and the cycle repeats. The waveform that appears at the emitter is shown in Figure 6.71(c).

In order for the above sequence of events to take place, R_E has to meet certain conditions. What these conditions are can best be explained by means of the emitter characteristic curve in Figure 6.72. (This curve is not drawn to scale in order to show more detail.)

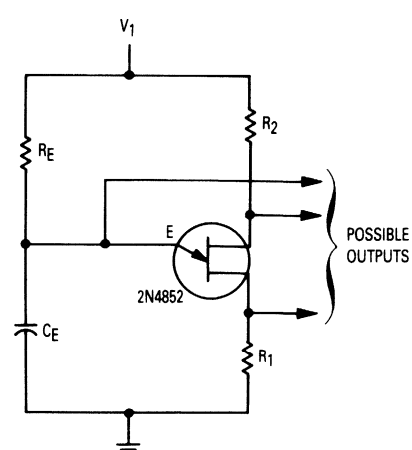
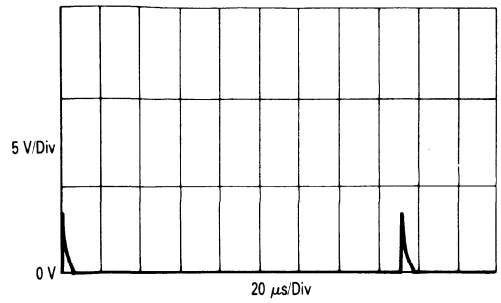
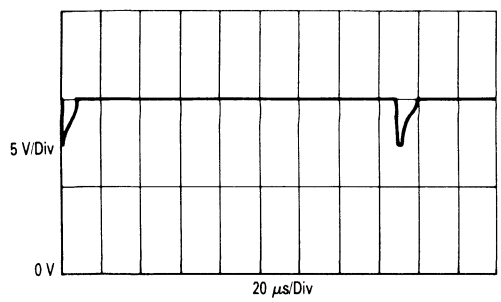


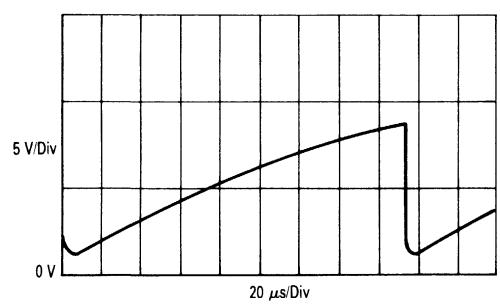
Figure 6.70. Basic UJT Relaxation Oscillator



(a). Base-One Waveform



(b). Base-Two Waveform



(c). Emitter Waveform

Figure 6.71. UJT Oscillator Waveforms

The emitter capacitor C_E, will charge until the emitter voltage is equal to V_p. At this point on the characteristic curve, peak point emitter current I_p will be flowing, and in order to fire the unijunction, the value of emitter resistor R_E must be small enough to allow a current somewhat larger than I_p to flow. R_E must, therefore, meet the following requirement:

$$R_E < \frac{V_1 - V_p}{I_p} = R_{E(max)} \qquad (1)$$

where V1 is the applied bias voltage.

Referring to Figure 6.72, this means that a load line intersecting the characteristic curve in the cutoff region, as illustrated by load line one, would keep the UJT from ever firing.

Having selected $R_E < R_{E(max)}$, the UJT will turn on, and C_E will discharge through the emitter. If R_E is too small, however, and allows an emitter current larger than the valley current I_V to flow, the UJT will not turn off. A stable state in the saturation region will result, and the load line will intersect the emitter characteristic curve somewhere to the right of the valley point. Load line 2 in Figure 6.76 intersecting the characteristic curve at P2 illustrates this condition.

The minimum R_E that can be used in order to assure oscillation can be defined by this formula:

$$R_E > \frac{V_1 - V_V}{I_V} = R_{E(min)}^{**} \qquad (2)$$

where V_V is the valley voltage.

An emitter resistance selected to meet the requirements in equations (1) and (2) will result in a load line which intersects the characteristic curve somewhere in the negative resistance region. An example is given by load line 3, intersecting the curve at P3. The theory explaining the turn-off will be given in the appendix.

The time required for a complete period can be calculated. The voltage on C_E at any time is given by the equation:

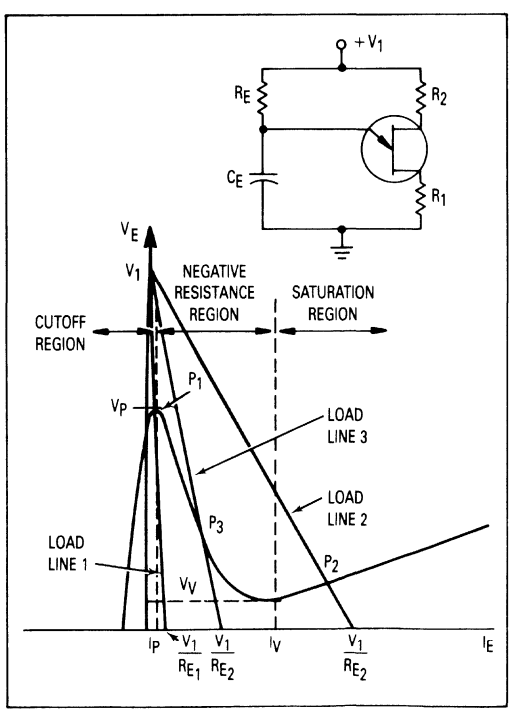


Figure 6.72. UJT Emitter Characteristic Load Lines

$$V_{CE} = V_V + (V_1 - V_V)(1 - e^{-t/R_E C_E}) \quad (3)$$

Substituting $V_{CE} = V_p = V_D + \eta V_{B2B1}$ *

$$V_D + \eta V_{B2B1} = V_V + (V_1 - V_V)(1 - e^{-t/R_E C_E}) \quad (4)$$

Solving this equation for t will give the time to charge C_E from V_V to V_p.

$$t = R_E C_E \ln \frac{V_1 - V_V}{V_1 - V_D - \eta V_{B2B1}} \quad (5)$$

A complete period T also includes the switching time of the UJT and the formula for T becomes:

$$T = R_E C_E \ln \frac{V_1 - V_V}{V_1 - V_D - \eta V_{B2B1}} + t_{on} + t_{off} \quad (6)$$

The following simplifications can be made in this formula:

The turn-on time is generally much smaller than t_{off} and can be omitted. V1 is also usually an order of magnitude larger than V_D or V_V, and when R1 and R2 are small, $V_{B2B1} \approx V1$. Equation (6) can therefore be written:

$$T \approx R_E C_E \ln \frac{1}{1 - \eta} + t_{off} \quad (7)$$

To summarize: The condition for stable operation of the relaxation oscillator is that R_E must be chosen such that the load line intersects the emitter characteristic in the negative resistance region. The approximate period can be found from Equation (7).

A SIMPLE TIME DELAY

The basic building block can be used without modification in simple time delay circuits. One such circuit is shown in Figure 6.70. The circuit operation is as follows:

The circuit values are determined by means of the equations developed previously. The value of the emitter resistor R_E is chosen by means of Equations (1) and (2) to meet the requirements.

$$R_{E(min)} < R_E < R_{E(max)}$$

When $R_E = 10\ M\Omega$, $C_E = 10\ \mu F$, and $\eta = 0.8$, the time required for one complete period can be found from Equation (7):

$$T \approx R_E C_E \ln \frac{1}{1 - \eta} = 10 \cdot 10^6 x 10 \cdot 10^{-6} x \ln \frac{1}{1 - 0.8}$$

$T \approx 160$ seconds

R2 is selected as 1 kΩ to provide maximum temperature compensation with the UJT used. The theory of temperature compensation is given in the appendix.

After the first cycle, the relay will normally be energized. When push-button S1, being normally closed is activated, the SCR turns off, the relay is de-energized, and power is applied to the relaxation oscillator and the load. After a time delay varying from less than a second to approximately 2.5 minutes, as determined by the setting of the 10 MΩ pot, the unijunction will fire and turn on the SCR. The relay will energize and power is removed from the oscillator and the load. The relay K1 will stay energized until the push button S1 is pushed again.

As shown in the example, the UJT trigger output from Base 1 directly drives the gate of the SCR. However, where isolation between the UJT trigger, or any other type of trigger, and the thyristor power circuit is required, then a simple pulse transformer interfacing the two elements will suffice.

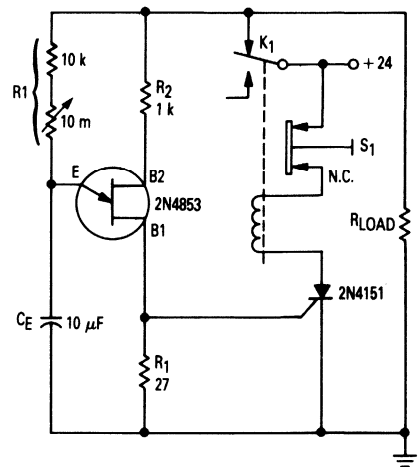


Figure 6.73. A Simple Time Delay Circuit

TEMPERATURE STABILIZATION OF THE PEAK POINT VOLTAGE

Practically all UJT characteristics are temperature dependent. The interbase resistance r_{BB} and emitter reverse current I_{EO} increase, while the peak, valley voltage, current, intrinsic standoff ratio η, and the junction diode drop decrease with increasing temperature.

The peak point voltage is given by the equation:

$$V_p = V_D + \eta V_{B2B1} \quad (10)$$

Since both V_D and η decrease with temperature, V_p will also decrease. This is, of course, a very undesirable condition in many applications, and particularly in timers and oscillator circuits. It has been found, however, that the change in V_p can be compensated for by adding a resistor R2 in series with the base two terminal.

If this resistor is selected properly, V_p can be made to vary less than 1% over a 50°C temperature variation. An equivalent circuit for the UJT in the cutoff region, including the external resistor R2, is shown in Figure 6.74. The peak point voltage is now given by:

*In practice, the variation of the emitter voltage in the neighborhood of the valley point is so small that in order to assure turn-off, R_E should be selected two to three times larger than $R_{E(min)}$.

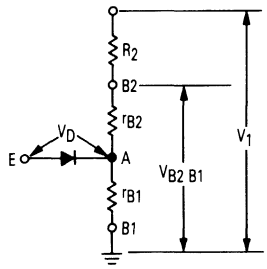


Figure 6.74. Electrical Equivalent Circuit for the UJT with the External Compensating Resistor R2. The Equivalent Circuit is Valid in the Cutoff Region Only.

$$V_p = V_D + \frac{\eta V_1 r_{BB}}{(r_{BB} + R2)} \qquad (11)$$

When temperature is increased, V_D decreases, and for V_p to remain unchanged, the second term in Equation (6), representing the voltage at point A, must increase. Since r_{BB} will increase and R2 will remain unchanged, the second term in the equation will indeed increase.

It would seem like a relatively simple task to calculate R2 from Equation (11) by taking the derivative of V_p with respect to temperature, setting $\frac{dv}{dt}$ p equal to zero, and solve for R2. This procedure would result in the following equation for R2.

$$R2 = 1/2 \left[-(2\, r_{BB} + V_1\, \eta \frac{K_2}{K_1} + V_1\, r_{BB} \frac{K_3}{K_1}) \pm (2\, r_{BB} + V_1\, \eta \frac{K_2}{K_1} + V_1\, r_{BB} \frac{K_3}{K_1} - 4\, r_{BB} (1 + V1 \frac{K_3}{K_1}) \right] \qquad (12)$$

$$\text{where } K_1 = \frac{dv_D}{dt} = -2.7 \text{ mV/°C}$$

$$K_2 = \frac{d\, r_{BB}}{dt} = \frac{r_{BBN} \cdot 0.77}{100} \text{ /°C}$$

$$K_3 = \frac{d\eta}{dt} = \frac{\eta N \cdot 0.06}{100} \text{ /°C}$$

and the subscript N denotes the value at 25°C.

When solving this equation, it would also have to be taken into account that r_{BB} is voltage dependent and when V_{B2B1} is increased by one volt, r_{BB} increases 1.2% (based on the value of r_{BB} at V_{B2B1} = 3 V). Furthermore, the temperature dependency of r_{BB} affects not only terms containing K2 but also terms containing r_{BB} itself.

In equation (12), r_{BB}, K1, K2, and η are voltage dependent and V_{B2B1} is dependent on R2. This interdependency results in a very complex equation that is difficult to solve, which in turn greatly reduces the usefulness of Equation (12).

In most applications, the variation predominates and can be compensated for by choosing R2 as follows:

$$R_2 = 15\%\ r_{BB} \qquad (13)$$

If a high degree of accuracy is required, however, a final adjustment of R2 should be made in the actual operating circuit.

Frequency variation as a function of temperature for a typical annular UJT is shown in Figure 6.75. Temperature curves for several values of R2 ranging from 250 ohms to 3 kohms are shown, and an R2 of approximately 1.5 kohms can be seen to compensate very well from −5°C to +85°C. A smaller resistor should be used for operation below −5°C.

DYNAMIC OPERATING PATHS

In order to determine the dynamic operating path of the relaxation oscillator, the circuit in Figure 6.76 can be used. Figure 6.80(b) shows the emitter characteristic curve for V_{B2B1} = 20 volts with the dynamic operating path of the oscillator shown with dotted lines. (V_1 is adjusted for V_{B2B1} = 20 volts.)

At the beginning of a cycle, C_E will start to charge from point A on the characteristic curve. At point B, where the voltage of C_E equals V_p, the UJT will fire and the characteristic curve goes into the negative resistance region. The voltage on the capacitor cannot change instantaneously, however, and the dynamic operating path will move from point B to point C. The time required to move from B to C is approximately 1 μs. From point C, the operating path follows an essentially straight line to point D, which is approximately equal to the valley point. This straight line has a slope of approximately 32 volts/ampere or 32 ohms, and is composed of R1 and the UJT emitter base one saturation resistance. There is not enough emitter current available to sustain operation at point D, and the operating path tries to follow the characteristic curve to the point where it is intersected by the load line determined by R_E. If the emitter circuit of the UJT were purely resistive (i.e. no capacitor C_E), this intersection point would be a stable operating point. To reach this point, however, the emitter voltage must increase. The resistance from emitter to base-one will also increase, and the emitter current will decrease somewhat. When the emitter voltage increases, however, current starts to

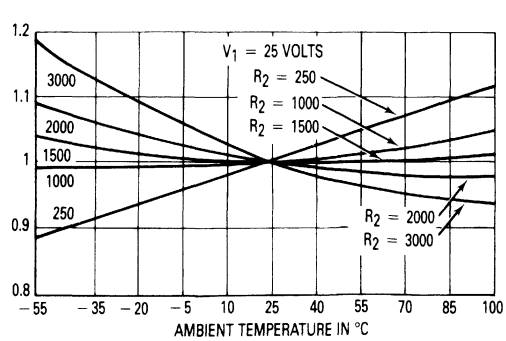
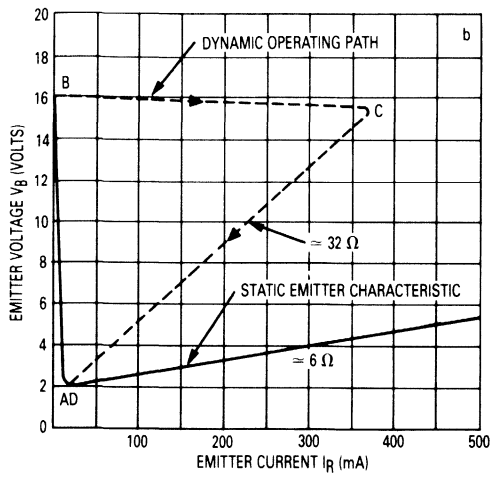
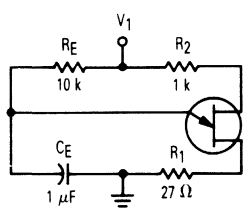


Figure 6.75. Frequency versus Temperature for a UJT Relaxation Oscillator Circuit. (Frequency is Normalized to 25°C and R2 is a Variable Parameter)



(a)



(b)

Figure 6.76. Determining the Dynamic Operating Path

flow into the capacitor and the emitter current is reduced more than that required by the characteristic curve. So, with a capacitor C_E in the emitter circuit, there are no stable operating points in the negative resistance region, and from point D, therefore, the operating path goes to point A again and the cycle repeats. It takes about 180 μs to traverse the path from point C to point A in the circuit shown.

The shape of the dynamic operating path is determined by the capacitor C_E, the bias voltage, and the resistor R1. Figure 6.77 shows operating paths for different values of C_E while 6.77(b) shows operating paths for fixed C_E but varying interbase voltage.

When an inductive load, like a relay coil, for example, is substituted for R1, the dynamic operating path will be somewhat different. Figure 6.78(a) shows a relaxation oscillator having a pulse transformer instead of R1, and Figure 6.78(b) shows the resulting dynamic operating path. An important difference here is that the emitter no longer ceases to conduct when valley voltage is reached but goes down to less than 0.5 volts before turning off. Figure 6.78(c) shows how the turn-off voltage is dependent on the bias voltage.

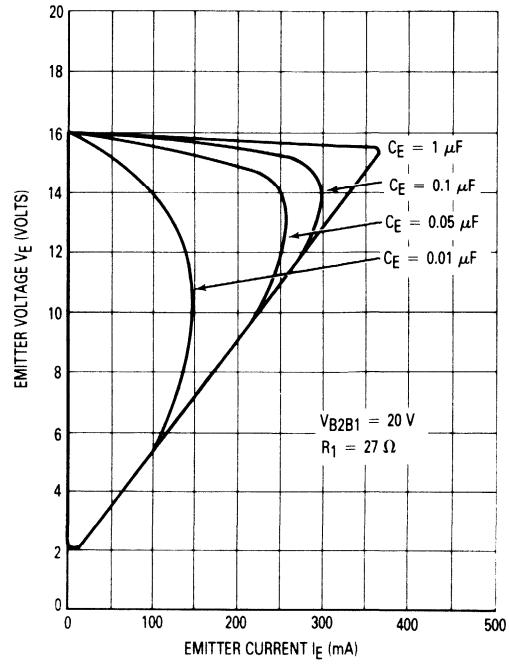


Figure 6.77(a). Dynamic Operating Path versus Emitter Capacitance (Circuit Figure 6.80)

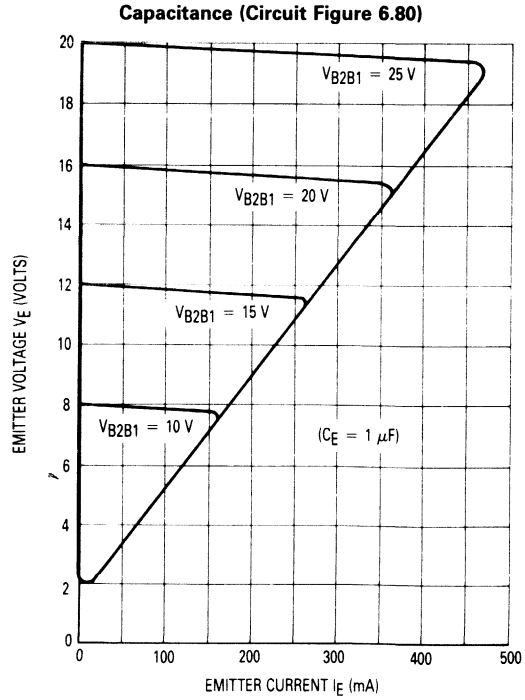


Figure 6.77(b). Dynamic Operation Path versus Interbase Voltage (Circuit Figure 6.80)

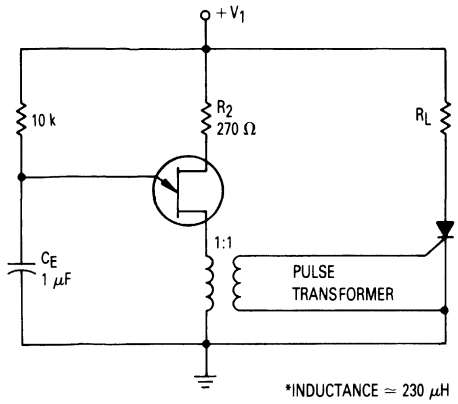
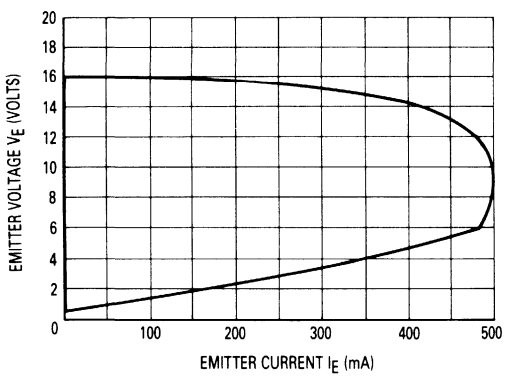
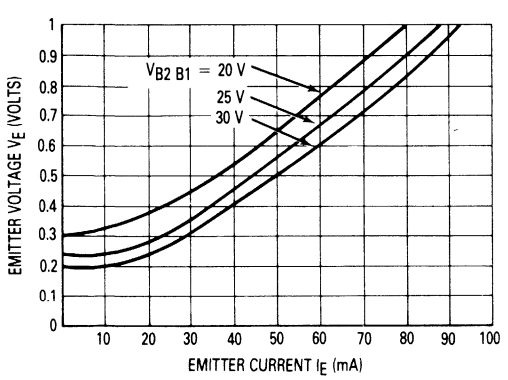


Figure 6.78(a). A Relaxation Oscillator with Inductive* Load



(b)



(c)

BATTERY CHARGER USING A UJT

The battery charger circuit shown in Figure 6.79(a) is a very simple circuit utilizing the relaxation oscillator.

The circuit will not work unless the battery to be charged is connected with proper polarity. The battery voltage controls the charger and when the battery is fully charged, the charger will not supply current to the battery.

The circuit operation is as follows: The battery charging current is obtained through the SCR when it is triggered into the conducting state by the UJT relaxation oscillator. The oscillator is only activated when the battery voltage is low. V_{B2B1} of the UJT is derived from the voltage of the battery to be charged, and since $V_p = V_D + \eta V_{B2B1}$, the higher V_{B2B1}, the higher V_p. When V_p exceeds the breakdown voltage of the zener diode Z1, the UJT will cease to fire and the SCR will not conduct. This indicates that the battery has attained its desired charge as set by R2.

The relaxation oscillator itself and the waveforms associated with the operation is shown in Figure 6.79(b). (The voltage increase will tend to change the pulse repetition rate, but this is not important, since the battery will tend to average the output.)

FEEDBACK CIRCUITS

The circuits described so far have been manual control circuits; i.e., the power output is controlled by a potentiometer turned by hand. Simple feedback circuits may be constructed by replacing R_T with heat or light-dependent sensing resistors; however, these circuits have no means of adjusting the operating levels. The addition of a transistor to the circuits allows complete control.

Figure 6.81 shows a feedback control using a sensing resistor for feedback. The sensing resistor may respond

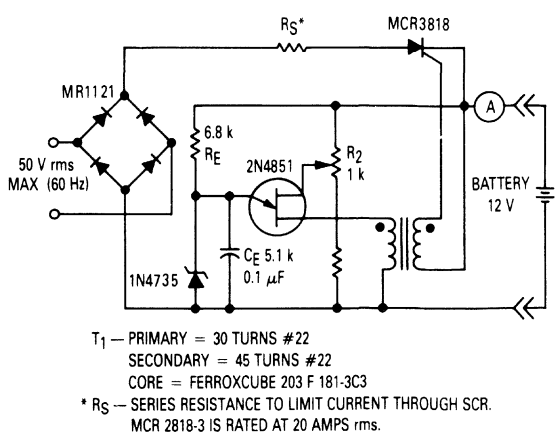


Figure 6.79(a). A 12 Volt Battery Charger Control (20 Amps rms Max)

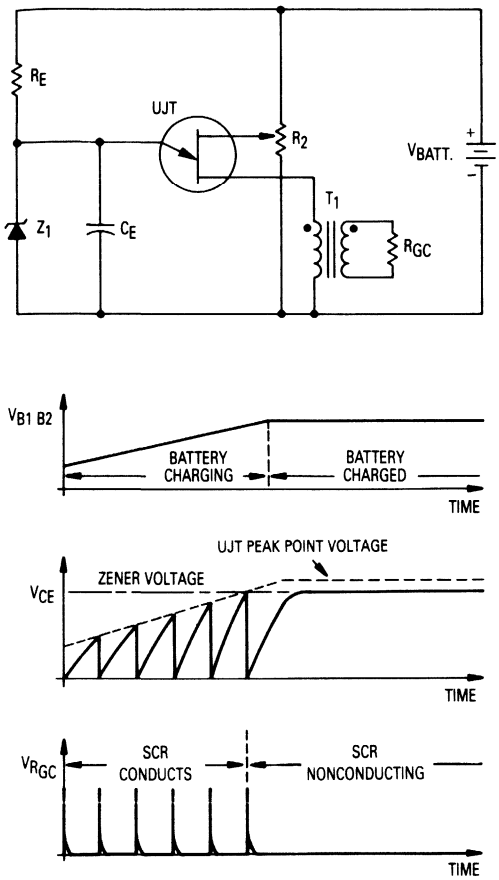


Figure 6.79(b). Waveforms Associated with Battery Charger Operation

to any one of many stimuli such as heat, light, moisture, pressure, or magnetic field. R_S is the sensing resistor and R_C is the control resistor that establishes the desired operating point. Transistor Q_1 is connected as an emitter follower such that an increase in the resistance of R_S decreases the voltage on the base of Q_1, causing more current to flow. Current through Q_1 causes voltage to charge C_T, triggering the UJT at some phase angle. As R_S becomes larger, more current flows into the capacitor, the voltage builds up faster, causing the UJT to trigger at a smaller phase angle and more power is applied to the load. When R_S decreases, less power is applied to the load. Thus, this circuit is for a sensing resistor which decreases in response to too much power in the load. If the sensing resistor increases with load power, then R_S and R_C should be interchanged.

If the quantity to be sensed can be fed back to the circuit in the form of an isolated, varying dc voltage such as the output of a tachometer, it may be inserted between the voltage divider and the base of Q1 with the proper polarity. In this case, the voltage divider would be a potentiometer to adjust the operating point. Such a circuit is shown in Figure 6.82.

In some cases, average load voltage is the desired feedback variable. In a half wave circuit this type of feedback usually requires the addition of a pulse transformer, shown in Figure 6.83. The RC network, R_1, R_2, C_1 averages load voltage so that it may be compared with the set point on R_S by Q_1. Full wave operation of this type of circuit requires dc in the load as well as the control circuit. Figure 6.84 is one method of obtaining this full wave control.

There are, of course, many more sophisticated circuits which can be derived from the basic circuits discussed here. If, for example, very close temperature control is desired, the circuit of Figure 6.81 might not have sufficient gain. To solve this problem a dc amplifier could be inserted between the voltage divider and the control transistor gate to provide as close a control as desired. Other modifications to add multiple inputs, switched gains, ramp and pedestal control, etc., are all simple additions to add sophistication. Basically, however, it is the UJT itself which provides the fast rising, high current pulse,

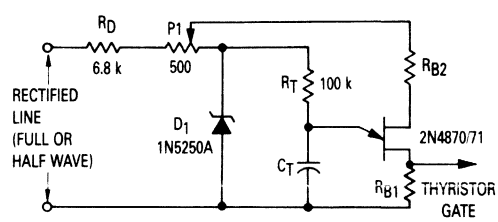


Figure 6.80. Circuit for Line Voltage Compensation

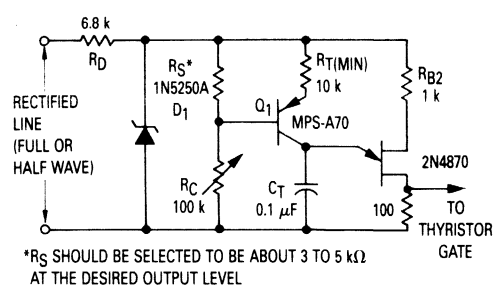


Figure 6.81. Feedback Control Circuit

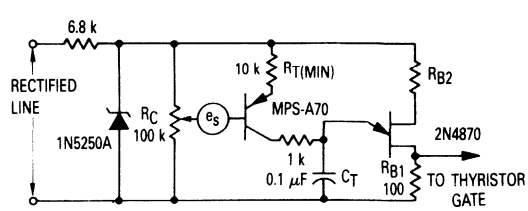


Figure 6.82. Voltage Feedback Circuit

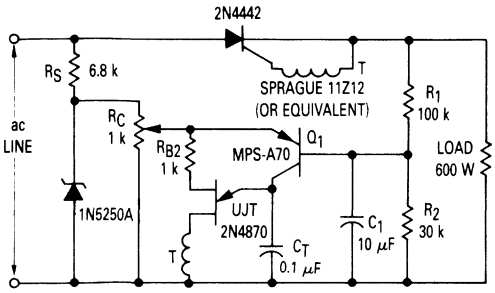


Figure 6.83. Half Wave, Average Voltage Feedback

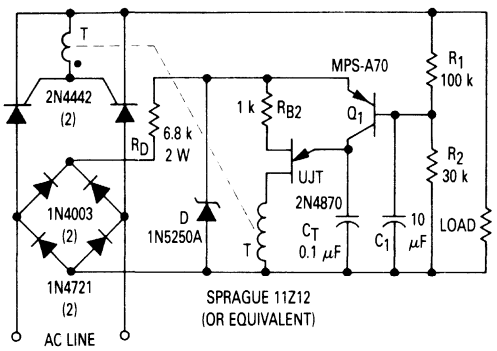


Figure 6.84. Full Wave, Average Voltage Feedback Control

which is desirable for reliable thyristor operation. The ease of adding feedback and relative insensitivity to line voltage changes are additional benefits gained from using this trigger device.

TEMPERATURE-SENSITIVE HEATER CONTROL

Figure 6.85 shows a heater circuit which is controlled by the room temperature. This circuit eliminates several of the disadvantages of the mechanical control: large size, high price, unreliability, and poor power regulation. The mechanical control is an on-off control and is not capable of regulating the power. By using phase control, the circuit shown in Figure 6.85 is able to reduce the power to the load as the desired temperature is reached, thus eliminating much of the overshoot inherent in mechanical controls.

The line voltage is full-wave rectified by the bridge consisting of D1 through D4. The output of the bridge is applied to the control circuit through resistor R1 and clamped to 20 volts by zener diode D5. The thermistor R_T and variable resistor R2 control the base current for transistor Q1. R2 is adjusted so Q1 is off at the desired temperature. When Q1 is off, no current can flow to capacitor C1, and C1 cannot charge to the firing voltage of unijunction transistor Q2. Therefore, Q2 cannot fire the TRIAC. If the temperature decreases, the resistance of R_T increases, Q1 is turned on and current flows to C1. C1 charges to the firing voltage of Q2, Q2 fires and turns the TRIAC on through pulse transformer T1. If the temperature continues to decrease, the resistance of R_T increases more and Q1 is turned on more. C1 charges faster and the TRIAC is triggered earlier, delivering more power to the load. As the temperature increases, the resistance of R_T decreases and Q1 will conduct less. C1 takes longer to charge and the TRIAC is triggered later in the cycle. When the desired temperature is reached, Q1 is off and the TRIAC is off.

The circuit shown is for a heater load, but the circuit could also be used to control a motor with a constant load such as a blower motor, as indicated by the dotted portion of Figure 6.85. The circuit is shown for a heating application but can be used for cooling by interchanging R_T and R2.

800 W LIGHT-DIMMER CIRCUITS

Figure 6.86 shows a wide-range light-dimmer circuit using a unijunction transistor and a pulse transformer to provide phase control for the TRIAC. The circuit operates from a 115 volt, 60 Hz source and can control up to 800 watts of power to incandescent lights. The power to the lights is controlled by varying the conduction angle of the TRIAC from 0° to about 170°. The power available at 170° conduction is better than 97% of that at the full 180°.

Operation begins when ac voltage is applied to the diode bridge consisting of diodes D1 through D4. The bridge rectifies the input voltage and applies a dc voltage to resistor R1 and zener diode D5. The zener applies a constant voltage of 22 volts to unijunction transistor Q1 except at the end of each alternation when the line voltage drops to zero. During each half cycle, capacitor C1 charges through variable resistor R2 until the capacitor voltage equals the emitter firing voltage V_P of Q1. When V_P is reached, Q1 fires and C1 discharges through the emitter of Q1 and a pulse is applied to the TRIAC through pulse transformer T1. Once the TRIAC turns on, voltage to the timing circuit is removed and no further pulses can occur during that half cycle. Since the line voltage is full-wave rectified and applied to the phase control circuit, the operation is the same for both positive and negative half cycles. Variable resistor R2 varies the time constant of the timing circuit thus providing phase control of the TRIAC.

800 W SOFT-START LIGHT DIMMER

The circuit shown in Figure 6.87 is a light dimmer with soft-start operation. Soft starting is desirable because of the very low resistance of a cold filament compared to its hot resistance. This low resistance causes very high inrush currents when a lamp is first turned on, and this leads to short lamp life. Soft starting also allows the use of TRIACs with lower current ratings. Failures caused by high inrush currents are eliminated by the soft-start feature, which applies current to the bulb slowly enough to eliminate high surges. Accidental turn on, which could nullify this advantage, is prevented by a special dv/dt network (R6, C3) across the TRIAC.

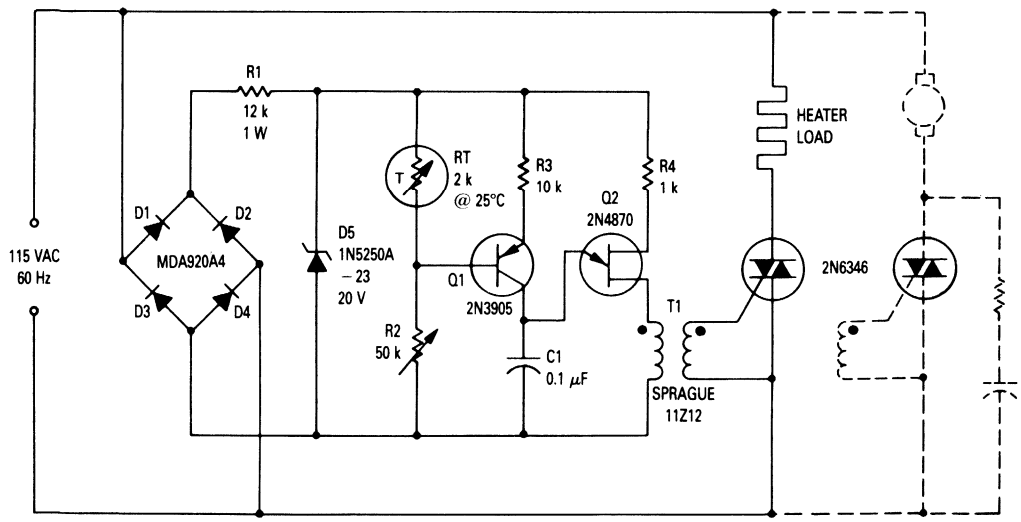


Figure 6.85. Temperature-Sensitive Heater Control

Operation of this circuit begins when 115 Vac input voltage is applied to the diode bridge consisting of D1 through D4. The bridge rectifies the input and applies a dc voltage to resistor R1 and zener diode D5. The zener provides a constant voltage of 20 volts to unijunction transistor Q1, except at the end of each half-cycle of the input when the line voltage drops to zero. Initially the voltage across capacitor C1 is zero and capacitor C2 cannot charge to trigger Q1. C1 will begin to charge, but because the voltage is low, C2 will be charged to a voltage adequate to trigger C1 only near the end of the half cycle. Although the lamp resistance is low at this time, the voltage applied to the lamp is low and the inrush current is small. Then the voltage on C1 rises, allowing C2 to trigger Q1 earlier in the cycle. At the same time the lamp is being heated by the slowly increasing applied voltage, and by the time the peak voltage applied to the lamp has reached its maximum value, the bulb has been heated sufficiently so that the peak inrush current is kept to a reasonable value. Resistor R4 controls the charging rate of C2 and provides the means to dim the lamp. Diode D6 and resistor R7 improve operation at low conduction angles.

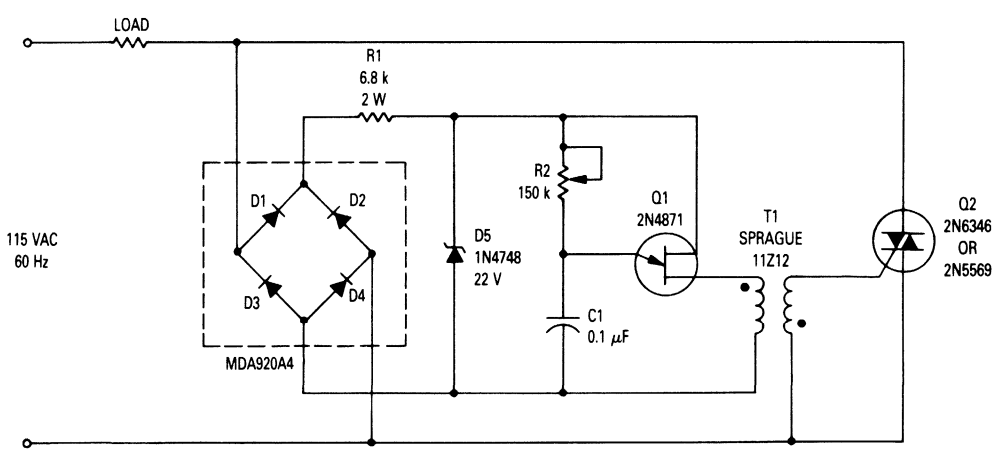


Figure 6.86. 800 W TRIAC Light Dimmer

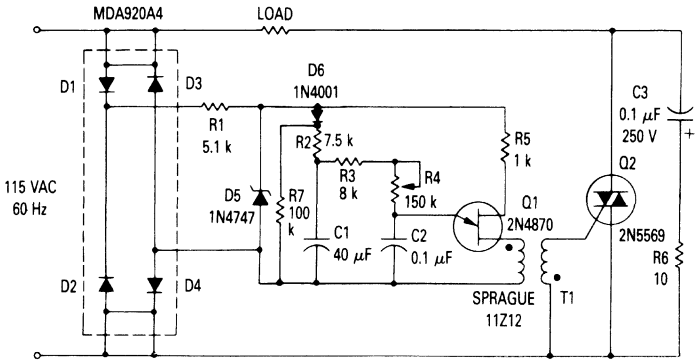


Figure 6.87. 800 W Soft-Start Light Dimmer

VOLTAGE REGULATOR FOR A PROJECTION LAMP

The circuit shown in Figure 6.88 will regulate the rms output voltage across the load (a projection lamp) to 100 volts ±2% for an input voltage between 105 and 250 volts ac. This is accomplished by indirectly sensing the light output of lamp L1 and applying this feedback signal to the firing circuit (Q1 and Q2) which controls the conduction angle of TRIAC Q3. The load is a 150-watt projection lamp which has a reflector mirror included inside the glass envelope. If the light output of the lamp were sensed directly by the photocell, it would respond to the 60 Hz variations of the supply voltage unless additional filter components were used. Therefore, another approach was used to generate the feedback signal. The reflector inside the lamp's envelope glows red due to the heat of the filament. Since the reflector has a relatively large mass it cannot respond to the supply frequency, and its light output provides a form of integration. This light is then used as a feedback signal. To eliminate 60 Hz modulation of the photocell, it is mounted at one end of a black tube with the other end of the tube directed at the back side of the reflector in the lamp. The lamp voltage is provided by TRIAC Q3, whose conduction angle is set by the firing circuit for unijunction transistor Q2. The circuit is synchronized with the line through the full-wave bridge rectifier. The voltage to the firing circuit is limited by zener diode D5. Phase control of the supply voltage is set by the charging rate of capacitor C1. Q2 will fire when the voltage on C1 reaches approximately 0.65 times the zener voltage. The charging rate of C1 is set by the conduction of Q1, which is controlled by the resistance of photocell R2. Potentiometers R3 and R4 are used to set the lamp voltage to 100 volts when the line voltage is 105 volts and 250 volts, respectively. This assures that

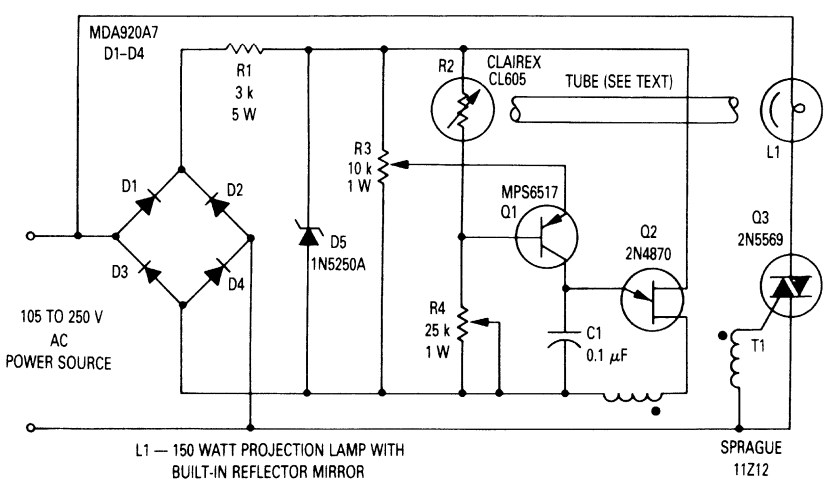
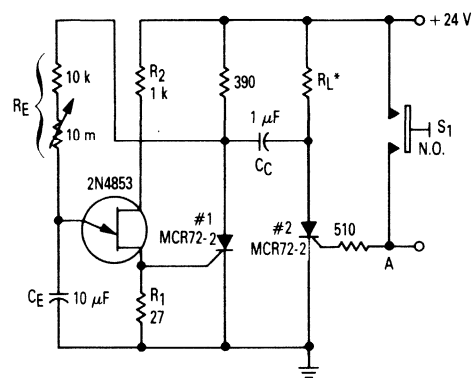


Figure 6.88. Voltage Regulator for a Projection Lamp

the lamp voltage will be within the desired tolerance over the operating range of input voltage. Some interaction will occur between R3 and R4 and the adjustment of each potentiometer may have to be made several times. Since this is an rms voltage regulator, a true rms meter must be used to adjust the load voltage.

TIMER CIRCUITS

A variation of the UJT-relay time delay circuit is shown in Figure 6.89. Here the relay is replaced by an SCR which generally reduces circuit cost. After one cycle of operation, SCR #1 will be on, and a low value of voltage is applied to the UJT emitter circuit, thus interrupting the timing function. When push button S1 is pushed, or a positive going pulse is applied at point A, SCR #2 will turn on, and SCR #1 will be turned off by commutating capacitor C_C. With SCR #1 off, the supply voltage will be applied to R_E and the circuit will begin timing again. After a period of time determined by the setting of R_E, the UJT will fire and turn SCR #1 on and commutate SCR #2 off.



*VALUE OF R_L MUST BE LOW ENOUGH TO ALLOW HOLD CURRENT TO FLOW IN THE SCR.

Figure 6.89. A Simple Time Delay Circuit Using Two SCRs

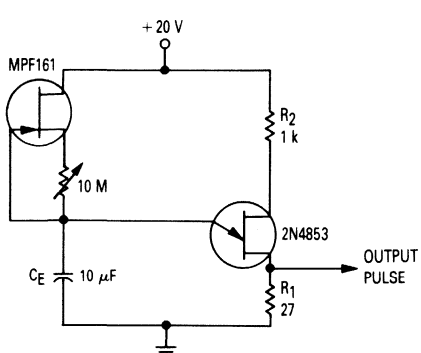


Figure 6.90. A Time Delay Circuit Featuring Constant Current Charging

The time delay is determined by the charge time of the capacitor. In order to achieve long time delays, R_E, C_E, or both will have to be large. For good accuracy and repeatability, the capacitor must have a leakage current that is much smaller than the charge current. A Mylar type capacitor has been found to be good for this purpose, but since this type of capacitor is fairly expensive for large values of capacitance, it is preferable to increase R_E in order to obtain long time delays. Large values of R_E, however, creates a problem due to the UJT peak point emitter current I_p. When the capacitor is charged almost to the peak point, only a small voltage will appear across R_E, and if R_E is very large, only a small current will be flowing. If the peak current of the UJT is appreciable, the device will never fire if the current through R_E is not sufficient to supply I_p. The annular device, having a typical I_p of 0.2 μA @ V_{B2B1} = 25 Vdc, offers an advantage in this area and large values of R_E can be used. However, when charging through a resistor, the charge current will initially be relatively large while the charge current when the voltage on the capacitor is close to V_p will be small. It would, for this reason, be advantageous to charge with a constant small current. This can be accomplished by simply replacing R_E by a junction field effect transistor as shown in Figure 6.90. Since the JFET is fully on when there is no voltage from gate to source, the 10 MΩ resistor will determine the amount of off bias applied to the FET. A constant current of less than 1 μA can easily be obtained which results in time delays up to 10 minutes.

When the capacitor is charged with a linear current, the charge time can be found from the equation:

$$t_{charge} = \frac{(V_p - V_V) \cdot C_E}{I_{charge}}$$

When C_E is in microfarads and I_{charge} is in microamperes, t will be in seconds.

However, even an emitter peak current as low as 0.2 μA is objectionable if longer time delays are desired. In the circuit shown in Figure 6.91 the peak current is supplied separately from the charging current and extremely long time delays are possible. Transistor Q1 and resistors R1, R2, and R3 form a constant current source and the charge current might be adjusted to be as low as a few nanoamperes. This current would, of course, not be sufficient to fire the UJT where I_p = 0.2 μA unless the peak current was supplied from another source. Field effect transistor Q2, acting as a source follower, supplies the current flowing into the emitter lead prior to firing and diode D1 provides a low impedance discharge path for C_E. D1 must be selected to have a leakage much lower than the charge current.

The charge current to C_E is given by the formula:

$$I_{charge} = \frac{E - V_{BE}}{R3} - I_B$$

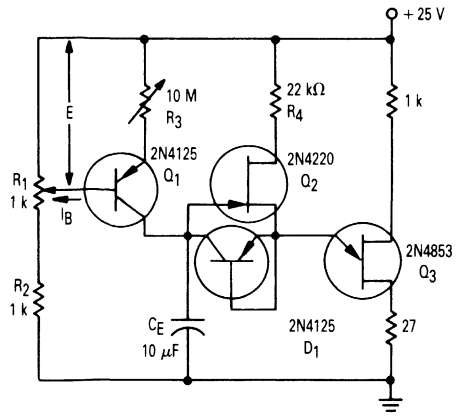


Figure 6.91. Long Duration Time Delay

Since I_B is small, the delay time will vary linearly with R3. The voltage E, applied across R3 and the base emitter junction of Q1, is set by the variable resistor R1. Time delays up to 10 hours are possible with this circuit. Resistor R4 in series with the FET drain terminal must be large enough not to allow currents in excess of I_V to flow when the UJT is on, otherwise the UJT will not turn off and the circuit will latch up.

PUT APPLICATIONS

PUTs are negative resistance devices and are often used in relaxation oscillator applications and as triggers for controlling thyristors. Due to their low leakage current, they are useful for high-impedance circuits such as long-duration timers and comparators.

TYPICAL CIRCUITS

The following circuits show a few of the many ways in which the PUT can be used. The circuits are not optimized even though performance data is shown.

In several of the circuit examples, the versatility of the PUT has been hidden in the design. By this it is meant that in designing the circuit, the circuit designer was able to select a particular intrinsic standoff ratio or he could select a particular R_G (gate resistance) that would provide a maximum or minimum valley and peak current. This makes the PUT very versatile and very easy to design with.

LOW VOLTAGE LAMP FLASHER

One advantage of the PUT over a conventional unijucntion transistor is that the PUT operates very well for low supply voltages. This is due to the low forward voltage drop of the PUT, 1.5 volts maximum for the MPU131-33, compared to the emitter saturation voltage of the UJT of 3 volts maximum for the 2N5431.

A circuit using the PUT in a low voltage application is shown in Figure 6.92 where a supply voltage of 3 volts is used. The circuit is a low voltage lamp flasher composed of a relaxation oscillator formed by Q1 and an SCR flip flop formed by Q2 and Q3.

With the supply voltage applied to the circuit, the timing capacitor C1 charges to the firing point of the PUT, 2 volts plus a diode drop. The output of the PUT is coupled through two 0.01 μF capacitors to the gate of Q2 and Q3. To clarify operation, assume that Q3 is on and capacitor C4 is charged plus to minus as shown in the figure. The next pulse from the PUT oscillator turns Q2 on. This places the voltage on C4 across Q3 which momentarily reverse biases Q3. This reverse voltage turns Q3 off. After discharging, C4 then charges with its polarity reversed to that shown. The next pulse from Q1 turns Q3 on and Q2 off. Note that C4 is a non-polarized capacitor.

For the component values shown, the lamp is on for about 1/2 second and off the same amount of time.

VOLTAGE CONTROLLED RAMP GENERATOR

The PUT provides a simple approach to a voltage controlled ramp generator, VCRG, as shown in Figure 6.93(a).

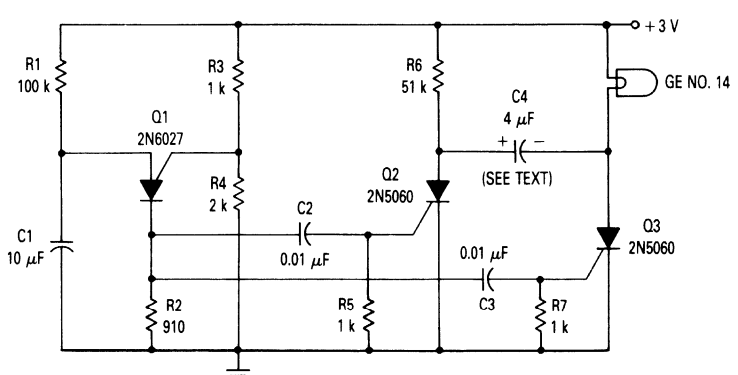


Figure 6.92. Low Voltage Lamp Flasher

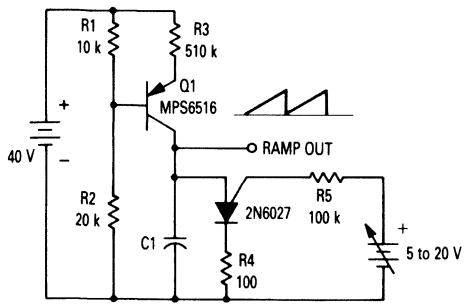
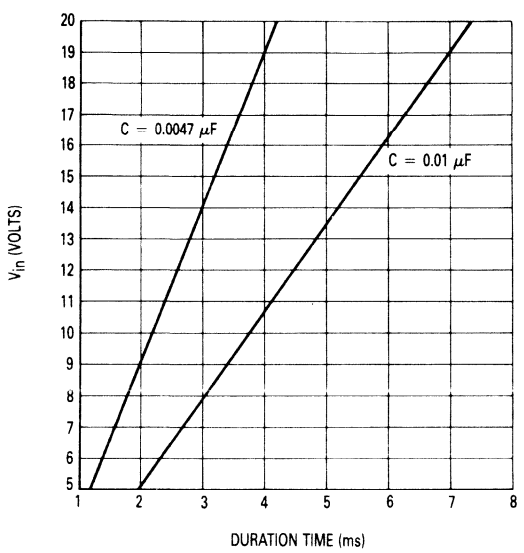


Figure 6.93(a). Voltage Controlled Ramp Generator (VCRG)



(b). Voltage versus Ramp Duration Time of VCRG

The current source formed by Q1 in conjuction with capacitor C1 set the duration time of the ramp. As the positive dc voltage at the gate is changed, the peak point firing voltage of the PUT is changed which changes the duration time, i.e., increasing the supply voltage increases the peak point firing voltage causing the duration time to increase.

Figure 6.93(b) shows a plot of voltage-versus-ramp duration time for a 0.0047 μF and a 0.01 μF timing capacitor. The figure indicates that it is possible to have a change in frequency of 3 ms and 5.4 ms for the 0.0047 μF and the 0.01 μF capacitor respectively as the control voltage is varied from 5 to 20 volts.

LOW FREQUENCY DIVIDER

The circuit shown in Figure 6.94 is a frequency divider with the ratio of capacitors C1 and C2 determining division. With a positive pulse applied to the base of Q1, assume that C1 = C2 and that C1 and C2 are discharged. When Q1 turns off, both C1 and C2 charge to 10 volts each through R3. On the next pulse to the base of Q1, C1 is again discharged but C2 remains charged to 10 volts. As Q1 turns off this time, C1 and C2 again charge. This time C2 charges to the peak point firing voltage of the PUT causing it to fire. This discharges capacitor C2 and allows capacitor C1 to charge to the line voltage. As soon as C2 discharges and C1 charges, the PUT turns off. The next cycle begins with another positive pulse on the base of Q1 which again discharges C1.

The input and output frequency can be approximated by the equation

$$f_{in} \approx \frac{(C1 + C2)}{C1} f_{out}$$

For a 10 kHz input frequency with an amplitude of 3 volts, Table 6.X shows the values for C1 and C2 needed to divide by 2 to 11.

This division range can be changed by utilizing the programmable aspect of the PUT and changing the voltage on the gate by changing the ratio R6/(R6 + R5). Decreasing the ratio with a given C1 and C2 decreases the division range and increasing the ratio increases the division range.

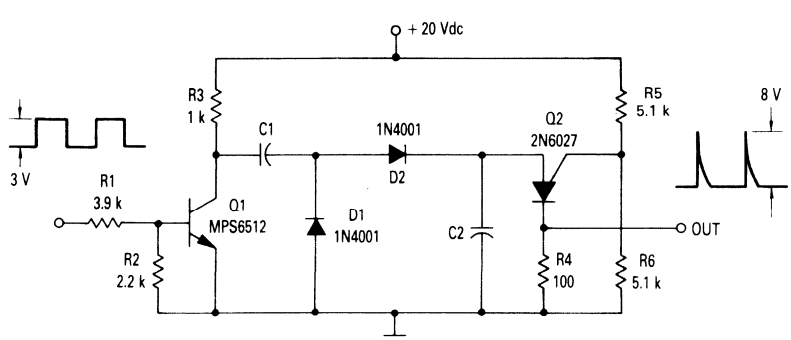


TABLE 6.X

C_1	C_2	Division
0.01 μF	0.01 μF	2
0.01 μF	0.02 μF	3
0.01 μF	0.03 μF	4
0.01 μF	0.04 μF	5
0.01 μF	0.05 μF	6
0.01 μF	0.06 μF	7
0.01 μF	0.07 μF	8
0.01 μF	0.08 μF	9
0.01 μF	0.09 μF	10
0.01 μF	0.1 μF	11

Figure 6.94. Low Frequency Divider

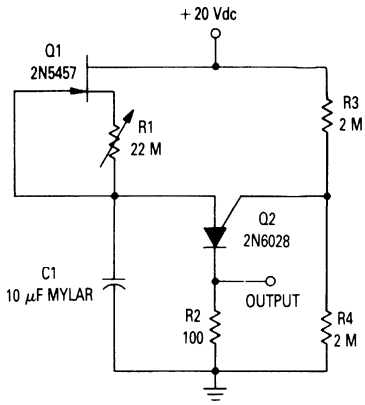


Figure 6.95. 20-Minute, Long Duration Timer

The circuit works very well and is fairly insensitive to the amplitude, pulse width, rise and fall times of the incoming pulses.

PUT LONG DURATION TIMER

A long duration timer circuit that can provide a time delay of up to 20 minutes is shown in Figure 6.95. The circuit is a standard relaxation oscillator with a FET current source in which resistor R1 is used to provide reverse bias on the gate-to-source of the JFET. This turns the JFET off and increases the charging time of C1. C1 should be a low leakage capacitor such as a mylar type.

The source resistor of the current source can be computed using the following equation:

$$V_{GS} = V_P\,(1 - \sqrt{I_O/I_{DSS}})$$

$$\therefore R1 = \frac{V_{GS}}{I_O}$$

where I_O is the current out of the current source.
V_P is the pinch off voltage,
V_{GS} is the voltage gate-to-source and,
I_{DSS} is the current, drain-to-source, with the gate shorted to the source.

The time needed to charge C1 to the peak point firing voltage of Q2 can be approximated by the following equation:

$$t = \frac{C\Delta V}{I},$$

where t is time in seconds
C is capacitance in μF,
ΔV is the change in voltage across capacitor C1, and
I is the constant current used to charge C1.

Maximum time delay of the circuit is limited by the peak point firing current, I_P, needed to fire Q2. For charging currents below I_P, there is not enough current available from the current source to fire Q2, causing the circuit to lock up. Thus a PUT works better than a unijunction in a long duration timer because it has a lower peak point firing current. Also, because of the programmable aspect of the PUT, I_P can be made very small by making R_G (the equivalent parallel resistance of R3 and R4) large, (1 MΩ) as shown in Figure 6.95.

PHASE CONTROL

Figure 6.96 shows a circuit using a PUT for phase control of an SCR. The relaxation oscillator formed by Q2 provides conduction control of Q1 from 1 to 7.8 milliseconds or 21.6° to 168.5°. This constitutes control of over 97% of the power available to the load.

Only one SCR is needed to provide phase control of both the positive and negative portion of the sine wave by putting the SCR across the bridge composed of diodes D1 through D4.

BATTERY CHARGER USING A PUT

A short circuit proof battery charger is shown in Figure 6.97 which will provide an average charging current of about 8 amperes to a 12 volt lead acid storage battery. The charger circuit has an additional advantage in that it will not function nor will it be damaged by improperly connecting the battery to the circuit.

With 115 volts at the input, the circuit commences to function when the battery is properly attached. The battery provides the current to charge the timing capacitor C1 used in the PUT relaxation oscillator. When C1 charges

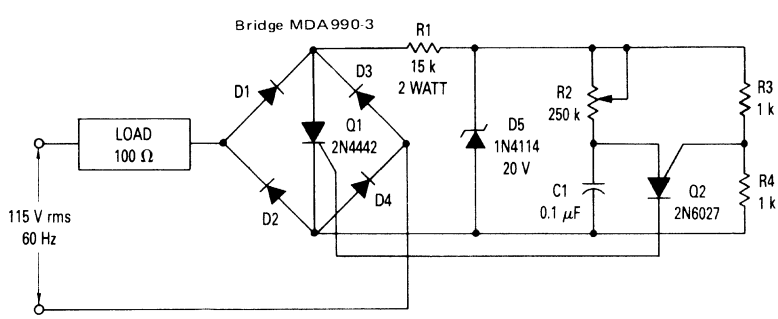


Figure 6.96. SCR Phase Control

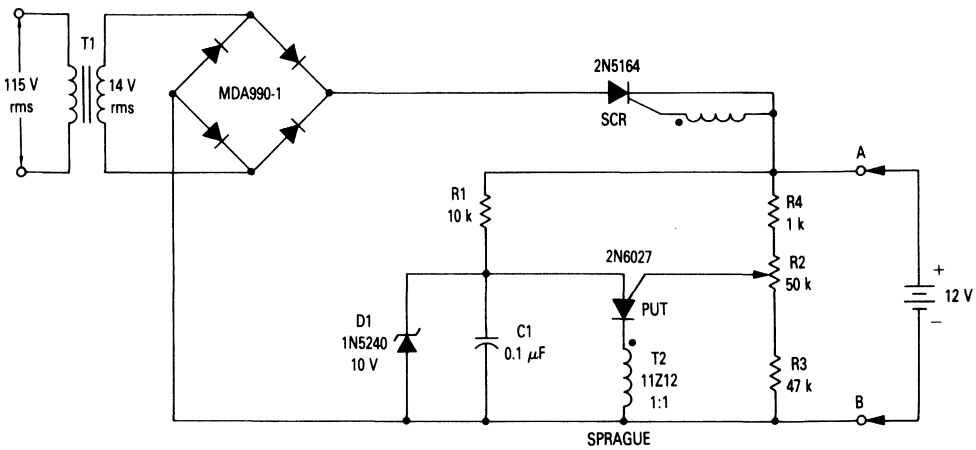


Figure 6.97(a). 12-Volt Battery Charger

to the peak point voltage of the PUT, the PUT fires turning the SCR on, which in turn applies charging current to the battery. As the battery charges, the battery voltage increases slightly which increases the peak point voltage of the PUT. This means that C1 has to charge to a slightly higher voltage to fire the PUT. The voltage on C1 increases until the zener voltage of D1 is reached which clamps the voltage on C1 and thus prevents the PUT oscillator from oscillating and charging ceases. The maximum battery voltage is set by potentiometer R2 which sets the peak point firing voltage of the PUT.

In the circuit shown, the charging voltage can be set from 10 V to 14 V, the lower limit being set by D1 and the upper limit by T1. Lower charging voltages can be obtained by reducing the reference voltage (reducing the value of zener diode D1) and limiting the charging current (using either a lower voltage transformer, T1, or adding resistance in series with the SCR).

Resistor R4 is used to prevent the PUT from being destroyed if R2 were turned all the way up.

Figure 6.97(b) shows a plot of the charging characteristics of the battery charger.

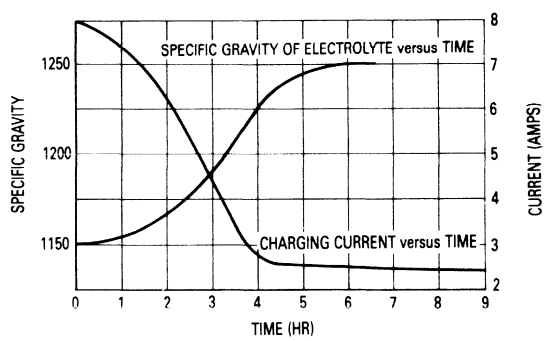


Figure 6.97(b). Charging Characteristics of Battery Charger

90 V rms VOLTAGE REGULATOR USING A PUT

The circuit of Figure 6.98 is an open loop rms voltage regulator that will provide 500 watts of power at 90 V rms with good regulation for an input voltage range of 110–130 V rms.

With the input voltage applied, capacitor C1 charges until the firing point of Q3 is reached causing it to fire. This turns Q5 on which allows current to flow through the load. As the input voltage increases, the voltage across R10 increases which increases the firing point of Q3. This delays the firing of Q3 because C1 now has to charge to a higher voltage before the peak-point voltage is reached. Thus the output voltage is held fairly constant by delaying the firing of Q5 as the input voltage increases. For a decrease in the input voltage, the reverse occurs.

Another means of providing compensation for increased input voltage is achieved by Q2 and the resistive divider formed by R6 and R7. As input voltage increases, the voltage at the base of Q2 increases causing Q2 to turn on harder which decreases the charging rate of C1 and further delays the firing of Q5.

To prevent the circuit from latching up at the beginning of each charging cycle, a delay network consisting of Q1 and its associated circuitry is used to prevent the current source from turning on until the trigger voltage has reached a sufficiently high level. This is achieved in the following way: Prior to the conduction of D2, the voltage on the base of Q1 is set by the voltage divider (R4 + R5)/(R1 + R3 + R4 + R5). This causes the base of Q1 to be more positive than the emitter and thus prevents Q1 from conducting until the voltage across R3 is sufficient to forward bias the base-emitter junction of Q1. This occurs when the line voltage has increased to about 15 volts.

The circuit can be operated over a different voltage range by changing resistors R6 and/or R4 which change the charging rate of C1.

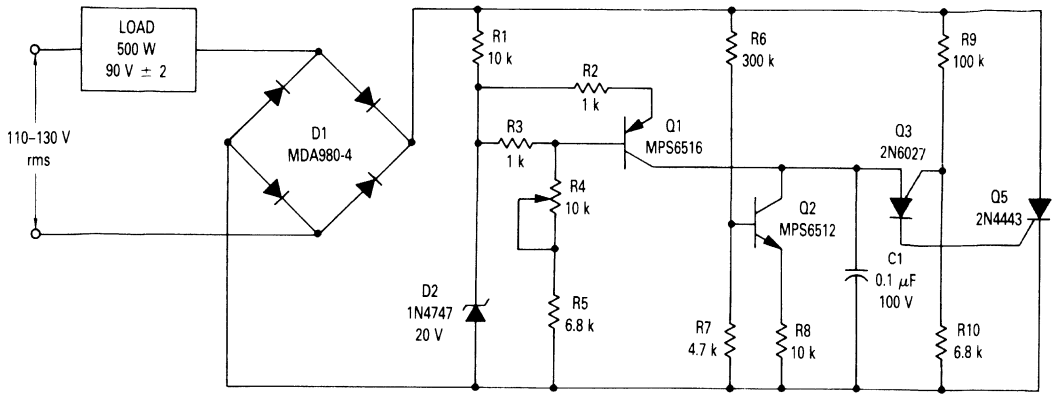
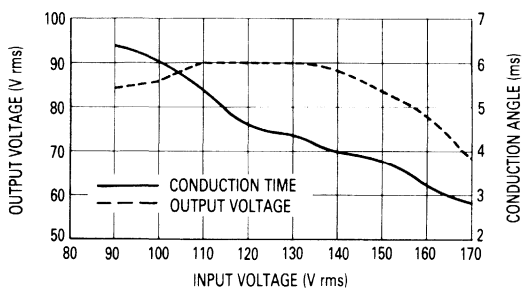


Figure 6.98(a). rms Voltage Regulator



(b). Output Voltage and Conduction Angle versus Input Voltage

Figure 6.98(b) provides a plot of output voltage and conduction angle versus input voltage for the regulator. As the figure indicates, good regulation can be obtained between the input voltage range of 110 to 130 volts.

SILICON BILATERAL SWITCH (SBS) APPLICATIONS

It is important that thyristor trigger circuitry be capable of supplying a fast rising, high current gate pulse to the power thyristors in order to prevent di/dt failure, especially when they are subjected to high inrush load currents. Because of the regenerative switching action and low dynamic on resistance of the SBS, it is ideally suited for this use.

These circuits indicate the uses for the SBS. In some applications the device switches on at V_S while in others it is turned on by drawing a small current out of the gate lead.

LAMP DIMMER

Figure 6.99 is the schematic diagram of a low cost full range lamp dimmer. Shunting the SBS with two 20 kΩ resistors minimizes the "flash-on" or hysteresis effect. V_S of the SBS is reduced to about 4 volts, and since this is below the operating voltage of the internal zener diodes, the temperature sensitivity of the device is increased.

An improved full range power controller suitable for lamp dimming and similar applications is shown in Figure 6.100.

It operates from a 120 volt, 60 Hz ac source and can control up to 1000 watts of power to incandescent bulbs. The power to the bulbs is varied by controlling the conduction angle of TRIAC Q1. Many circuits can be used for phase control, but the single RC circuit used is the simplest by far and was consequently chosen for this particular application. For settings such that no power is delivered to the load, the timing capacitor would never discharge through the SBS. The result is an abnormal amount of apparent phase shift caused by the capacitor starting to charge toward a source of voltage with a residual charge of the opposite sign. This is the cause of the hysteresis effect and is eliminated in this circuit by the addition of the two diodes and 5.1 kΩ resistor connected to the SBS gate. At the end of each positive half

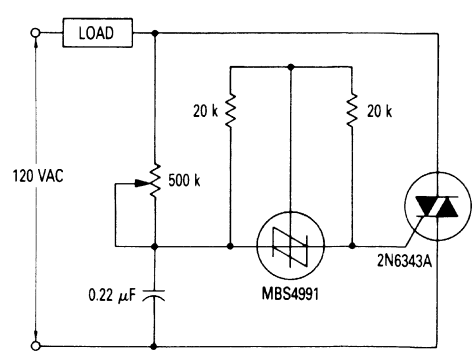


Figure 6.99. Low Cost Lamp Dimmer

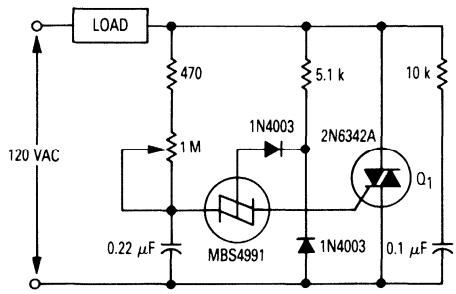


Figure 6.100. 1000 W TRIAC Light Dimmer

cycle when the applied voltage drops below that of the capacitor, gate current flows out of the SBS and it switches on, discharging the capacitor to near zero volts.

The RC network shown across the TRIAC represents a typical snubber circuit that is normally adequate to prevent line transients from accidentally firing the TRIAC.

ELECTRONIC CROWBAR

Occasionally the need arises for positive protection of expensive electrical or electronic equipment against excessive supply voltage. Such overvoltage conditions can occur due to improper switching, wiring, short circuits or failure of regulators. Where it is economically desirable to shut down equipment rather than allow it to operate on excessive supply voltage, an electronic "crowbar" circuit such as the one shown in Figure 6.101 can be employed to quickly place a short-circuit across the power lines, thereby dropping the voltage across the protected device to near zero and blowing a fuse. Since the TRIAC and SBS are both bilateral devices, the circuit is equally useful on ac or dc supply lines. With the values shown for R1, R2 and R3, the crowbar operating point can be adjusted over the range of 60 to 120 volts dc or 42 to 84 volts ac. The resistor values can be changed to cover a different range of supply voltages. The voltage rating of the TRIAC must be greater than the highest operating point as set by R2. I_1 is a low power incandescent lamp with a voltage rating equal to the supply voltage. It may be used to check the set point and operation of the unit by opening the test switch and adjusting the input or set point to fire the SBS. An alarm unit such as the Mallory Sonalert may be connected across the fuse to provide an audible indication of crowbar action. Note that this circuit may not act on short, infrequent power line transients.

SBS APPLICATIONS IN POWER CONTROL

The incandescent-lamp dimmer was one of the first circuits to use thyristors after their invention and has remained one of the most important applications of these devices. Triggering circuits for the lamp dimmer have taken many forms, from the relatively complex unijunction transistor oscillator with an RC slaving network to simpler circuits, which use a SBS trigger.

Figure 6.102 shows the basic control circuit. In the positive half-cycle, the 0.1 μF capacitor charges through the dual-section phase-shift circuit until its voltage reaches the break-over potential of the MBS4991 SBS. The MBS4991 potential then drops to about 1 volt, forcing charge from the 0.1 μF capacitor through the gate of the MAC210-4 TRIAC. This current turns the TRIAC on. When the TRIAC turns on, it removes the voltage from the timing circuit. C1 then discharges through the latched on TRIAC and the SBS if it also holds. What happens depends on the setting of R1, and the switching current, switching voltage, latching current and holding current of the SBS. Analysis of the circuit behavior is difficult and cannot be treated on a half-cycle basis because the previous half-cycle must be considered to establish the initial conditions, and because large residual voltages remain on C1. Several cycles of the ac line are needed to establish steady state conduction angles.

Hysteresis in the single RC phase controller is a result of the initial voltage on the capacitor before triggering. If the control is set to completely turn-off the lamp, triggering does not occur, and the capacitor voltage alternates up and down to some value less than V_S. If the control is advanced, the SBS fires and latches, causing the capacitor to charge from the previous polarity on-

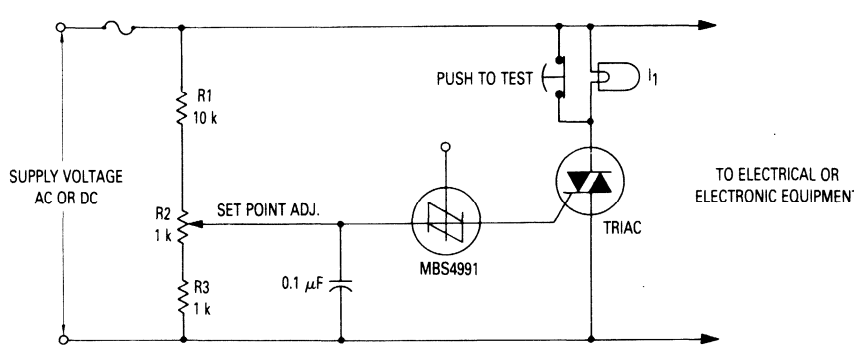


Figure 6.101. Electronic Crowbar

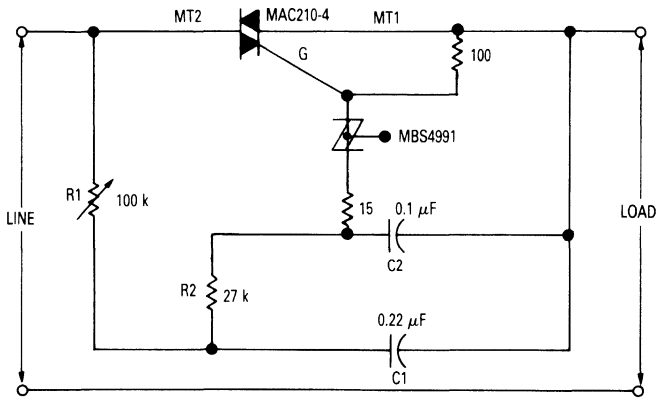


Figure 6.102. Basic Control Circuit for TRIAC Using a SBS Trigger

state voltage of about 1 V. Consequently, the control settings for dim illumination depend on whether the potentiometer is being advanced from an off state or retarded from a state with the lamp on, because the timing capacitor must charge through a different voltage gradient in the two cases.

The dual-section phase-shift network prevents hysteresis and allows reliable and stable triggering at all conduction angles. The 100 kΩ variable resistor R1 and the 0.22 μF capacitor C1 perform the basic phase shifting and serve as a charging supply for the 0.1 μF charge-storage capacitor C2. The 27 kΩ resistor isolates the trigger circuit from the phase shifter so that the voltage on C1 is only minimally affected by the triggering action. It is this isolation that reduces the hysteresis, prevalent in single-section phase-shift systems, to an unnoticeable level.

Although the same timing circuit is used for both halves of the cycle, the MBS4991 trigger is not exactly symmetrical. Therefore, the conduction angles of the MAC210-4 are not identical in the two half-cycles. As a result, a small dc component is introduced in the load.

In cases where high power must be handled or rapidly rising voltages may be encountered (high dv/dt), it is preferable to use two SCRs instead of a TRIAC for full-wave power control. Figure 6.103 illustrates a variation of the basic circuit to allow this. In the positive half-cycle, SCR-1 is triggered, through the primary of the pulse transformer (T), in exactly the same manner as in the basic circuit. In the negative half-cycle, the 0.1 μF triggering capacitor discharges through the shunt G-K diode of SCR-1 and the primary of the pulse transformer, inducing a pulse in the secondary, which triggers SCR-2.

The circuits described above were designed for incandescent-lamp dimmers and are ideally suited for this purpose. However, they may have many other uses, which are perhaps not immediately obvious. For example, uni-

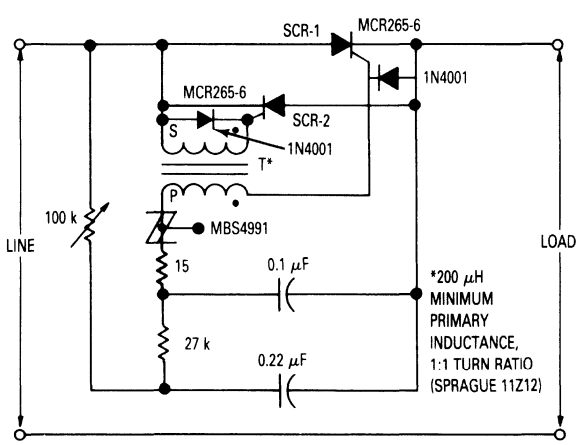


Figure 6.103. Basic Full-Wave Control Circuit for SCRs

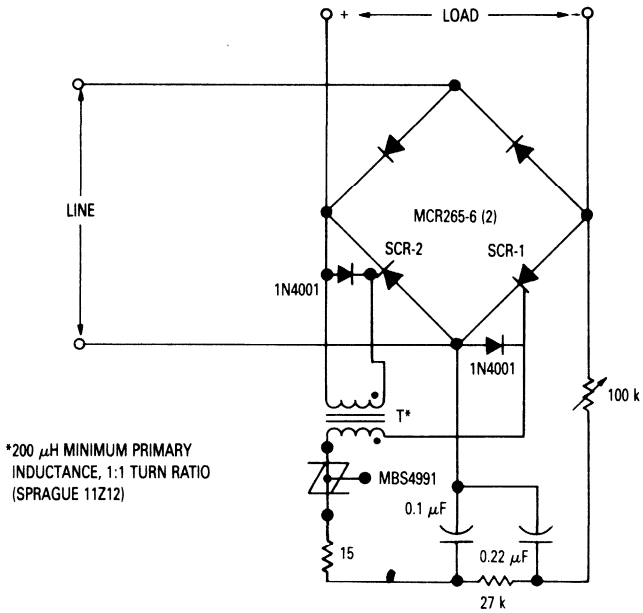


Figure 6.104. Variation of Basic Control Circuit to Provide Controlled DC Output

versal and shaded-pole motors are easily and conveniently controlled with these circuits. These motors have higher torque at low speeds when open-loop controlled in this manner rather than with rheostats or variable transformers, owing to the higher voltage pulses applied. In another application, a slight modification of the basic control circuit allows control of the dc output of a full-wave rectifier bridge using pulse-transformer coupling (Figure 6.104).

The power rating of these circuits is limited only by the thyristors employed. The control circuit will give sufficient drive for any thyristor that can be triggered with 50 mA or less gate current. For example, with MCR3818-4 controlled rectifiers mounted on a suitable heat sink, these circuits will control up to 3 kW power from a 120 V line.

TRIAC ZERO-POINT SWITCH APPLICATIONS

BASIC TRIAC ZERO-POINT SWITCH

Figure 6.105 shows a manually controlled zero-point switch useful in power control for resistive loads. Operation of the circuit is as follows. On the initial part of the positive half cycle, the voltage is changing rapidly from

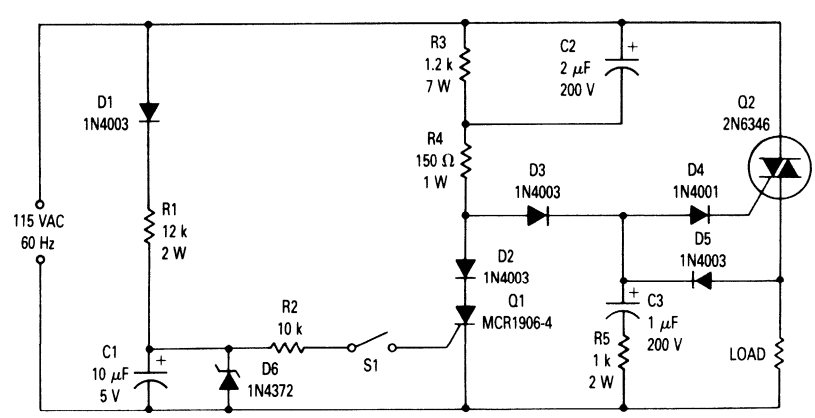


Figure 6.105. Zero-Point Switch

zero causing a large current flow into capacitor C2. The current through C2 flows through R4, D3, and D4 into the gate of the TRIAC Q2 causing it to turn on very close to zero voltage. Once Q2 turns on, capacitor C3 charges to the peak of the line voltage through D5. When the line voltage passes through the peak, D5 becomes reverse-biased and C3 begins to discharge through D4 and the gate of Q2. At this time the voltage on C3 lags the line voltage. When the line voltage goes through zero there is still some charge on C3 so that when the line voltage starts negative C3 is still discharging into the gate of Q2. Thus Q2 is also turned on near zero on the negative half cycle. This operation continues for each cycle until switch S1 is closed, at which time SCR Q1 is turned on. Q1 shunts the gate current away from Q2 during each positive half cycle keeping Q2 from turning on. Q2 cannot turn on during the negative cycle because C3 cannot charge unless Q2 is on during the positive half cycle.

If S1 is initially closed during a positive half cycle, SCR Q1 turns on but circuit operation continues for the rest of the complete cycle and then turns off. If S1 is closed during a negative half cycle, Q1 does not turn on because it is reverse biased. Q1 then turns on at the beginning of the positive half cycle and Q2 turns off.

Zero-point switching when S1 is opened is ensured by the characteristic of SCR Q1. If S1 is opened during the positive half cycle, Q1 continues to conduct for the entire half cycle and TRIAC Q2 cannot turn on in the middle of the positive half cycle. Q2 does not turn on during the negative half cycle because C3 was unable to charge during the positive half cycle. Q2 starts to conduct at the first complete positive half cycle. If S1 is opened during the negative half cycle, Q2 again cannot turn on until the beginning of the positive half cycle because C3 is uncharged.

A 3-volt gate signal for SCR Q1 is obtained from D1, R1, C1, and D6.

TEMPERATURE CONTROL WITH ZERO-POINT SWITCHING

Figure 6.106 shows a modulated TRIAC zero-point switching circuit designed to control heater loads operating from 115 Vac.

Circuit operation is best described by splitting the circuit into two parts. The circuit at the right is the zero-point switch (previously described in the section on zero-point switching) and its operation is unchanged. The circuit to the left is the proportional control for the zero-point switch.

The operation of the control circuit is as follows: diode D1, resistor R1, capacitor C1 and the load on C1 establish the dc supply voltage for the control circuit. Temperature

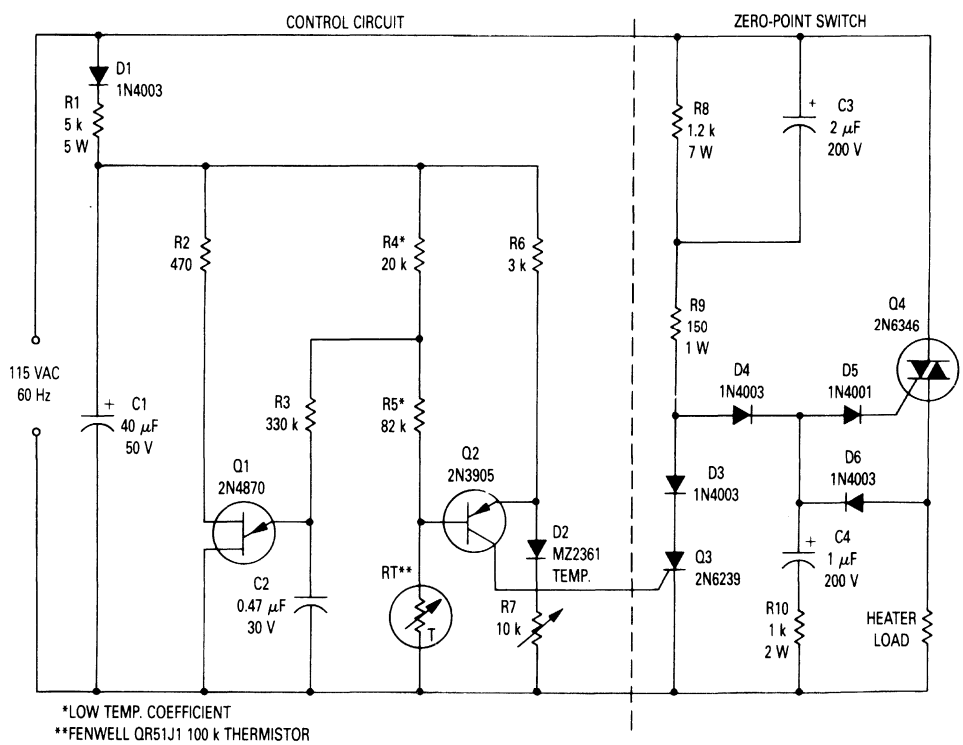


Figure 6.106. Temperature Controller Using Zero-Point Switching

is sensed by thermistor R_T, which is part of the bridge circuit consisting of R4, R5, R6, R7, D2 and R_T. The detector for the bridge is transistor Q2. R7 is set so the bridge is in balance at the desired temperature. As the temperature increases, R_T decreases, Q2 turns on and provides gate drive to SCR Q3. Q3 turns on and shunts the gate signal away from the TRIAC Q4. Q4 shuts off and removes power to the load. Now, as the temperature drops, R_T increases and Q2 turns off, SCR Q3 turns off, and full-wave power is applied to the load. Normally, the circuit would continue to cycle randomly, providing groups of full power to the heater load. However, modulation is applied to proportion the load power in response to small changes in R_T. The modulation is achieved by superimposing a sawtooth voltage on one arm of the bridge through R3. The period of the sawtooth is set to equal 12 cycles of the line frequency. From one to all 12 cycles can be applied to the load, thus allowing the load power to modulate in 8% steps from 0% to 100% duty cycle. The sawtooth voltage is generated by the unijunction transistor relaxation oscillator consisting of R2, R3, R4, C2 and Q1. The sawtooth wave modulates the bridge voltage so that over a portion of the twelve-cycle group the bridge voltage will be above the null point, and over the other portion it will be below the null point. This action divides each twelve-cycle group into an on portion and an off portion, the proportioning depending upon the amount R_T has varied from the nominal value. This circuit provides excellent control of a resistance heater as it will tend to stabilize and apply the correct amount of power on a continuous basis at a steady-state duty cycle depending on the load requirements. The temperature is therefore controlled over a very narrow range and no EMI is generated.

TRIAC RELAY-CONTACT PROTECTION

A common problem in contact switching high current is arcing which causes erosion of the contacts. A solution to this problem is illustrated in Figure 6.107. This circuit can be used to prevent relay contact arcing for loads up to 50 amperes.

There is some delay between the time a relay coil is energized and the time the contacts close. There is also a delay between the time the coil is de-energized and the time the contacts open. For the relay used in this circuit both times are about 15 ms. The TRIAC across the relay contacts will turn on as soon as sufficient gate current is present to fire it. This occurs after switch S1 is closed but before the relay contacts close. When the contacts close, the load current passes through them, rather than through the TRIAC, even though the TRIAC is receiving gate current. If S1 should be closed during the negative half cycle of the ac line, the TRIAC will not turn on immediately but will wait until the voltage begins to go positive, at which time diode D1 conducts providing gate

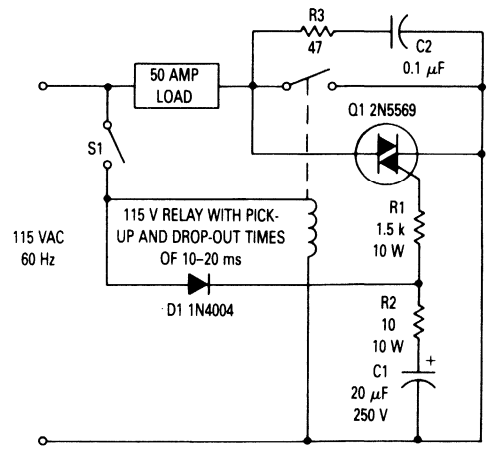


Figure 6.107. TRIAC Prevents Relay Contact Arcing

current through R1. The maximum time that could elapse before the TRIAC turns on is 8-1/3 ms for the 60 Hz supply. This is adequate to ensure that the TRIAC will be on before the relay contact closes. During the positive half cycle, capacitor C1 is charged through D1 and R2. This stores energy in the capacitor so that it can be used to keep the TRIAC on after switch S1 has been opened. The time constant of R1 plus R2 and C1 is set so that sufficient gate current is present at the time of relay drop-out after the opening of S1, to assure that the TRIAC will still be on. For the relay used, this time is 15 ms. The TRIAC therefore limits the maximum voltage, across the relay contacts upon dropout to the TRIAC's voltage drop of about 1 volt. The TRIAC will conduct until its gate current falls below the threshold level, after which it will turn off when the anode current goes to zero. The TRIAC will conduct for several cycles after the relay contacts open.

This circuit not only reduces contact bounce and arcing but also reduces the physical size of the relay. Since the relay is not required to interrupt the load current, its rating can be based on two factors: the first is the rms rating of the current-carrying metal, and the second is the contact area. This means that many well-designed 5 ampere relays can be used in a 50 ampere load circuit. Because the size of the relay has been reduced, so will the noise on closing. Another advantage of this circuit is that the life of the relay will be increased since it will not be subjected to contact burning, welding, etc.

The RC circuit shown across the contact and TRIAC (R3 and C2) is to reduce dv/dt if any other switching element is used in the line.

CHAPTER 7
MOUNTING TECHNIQUES FOR THYRISTORS

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, semiconductor-industry field history indicates that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.*

Many failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature resulting in reduced component life. In addition, mechanical damage can occur from mounting securely to a warped surface. With the widespread use of plastic-packaged semiconductors, mechanical damage becomes very significant.

Figure 7.1 shows an example of doing nearly everything wrong. In this instance, the victimized device is in a TO-220 package. The leads are bent to fit into a socket — an operation which, if not properly done, can crack the package, break the bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4"-hole containing a fiber-insulating sleeve. The force used to tighten the screw pulls the package into the hole, causing enough distortion to crack the die. Even if the die were not cracked, the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If the heat sink surface is rough and some burrs are present around the hole, many — but unfortunately not all — poor mounting practices are covered.

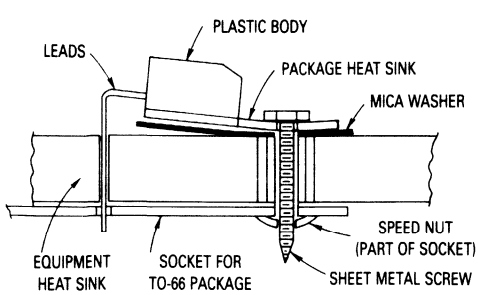


Figure 7.1. Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)

*See MIL Handbook 217B, Section 2.2.

In many situations, the semiconductor case must be isolated electrically from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, there is the possibility of arc-over problems if high voltages are being handled. Thus, electrical isolation places additional demands upon the mounting procedure.

Proper mounting procedures necessitate attention to the following areas:

1) Mounting surface preparation,
2) Application of thermal compounds,
3) Installation of the insulator,
4) Fastening of the assembly, and
5) Lead bending and soldering.

In this chapter, the procedures are discussed in general terms. Specific details for each class of packages are given in the figures and in Table 7.I. Appendix VII contains a brief review of thermal resistance concepts, and Appendix VIII lists sources of supply for accessories. Motorola-supplied hardware for all power packages is detailed on separate data sheets for each package type.

MOUNTING SURFACE PREPARATION

In general, the heat sink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heat sink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required.

SURFACE FLATNESS

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 7.2. Flatness is normally specified as a fraction of the Total Indicator

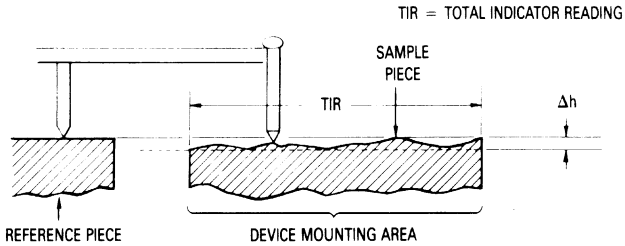


Figure 7.2. Surface Flatness

1

Reading (TIR). The mounting surface flatness, i.e., Δh/TIR, is satisfactory in most cases if less than 4 mils per inch, which is normal for extruded aluminum — although disc type devices usually require 1 mil per inch.

SURFACE FINISH

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory,* a finer finish is costly to achieve and does not significantly lower contact resistance. Most commercially available cast or extruded heat sinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger packages having mounting holes removed from the semiconductor die location, such as a TO-204AA (TO-3), may successfully be used with larger holes to accommodate an insulating bushing, but this doesn't work well with Thermopad plastic packages. For these packages, a smaller screw size must be used so that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because, if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heat sink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as it attempts to conform it to the shape of the heat sink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heat sink. The first effect may often be detected immediately by looking for cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and the problem is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heat sinks, several manufacturers are capable of properly utilizing the capabilities inherent of fine-edge blanking or sheared-through holes when applied to stamped heat sinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. The edges should be broken to remove burrs which cause poor contact between device and heat sink and which may puncture isolation material.

Many aluminum heat sinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heat sinks. For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heat sink, anodized or painted surfaces may be more effective than other insulating materials which tend to creep (i.e., they flow), thereby reducing contact pressure.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Unless used immediately after machining, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse. Thermal grease should be immediately applied thereafter and the semiconductor attached as the grease readily collects dust and metal particles.

THERMAL COMPOUNDS

To improve contacts, thermal joint compounds or greases are used to fill air voids between all mating surfaces. Values of thermal resistivity vary from 0.10 degrees

*Tests run by Thermalloy (Catalog #74-INS-3, page 14) using a copper TO-3 package with a typical 32-microinch finish, showed that finishes between 16 and 64 μ-in caused less than ±2.5% difference in interface thermal resistance.

Celsius-inches per watt for copper film to 1200°C-in/W for air, whereas satisfactory joint compounds will have a resistivity of approximately 60°C-in/W. Therefore, the voids, scratches, and imperfections which are filled with a joint compound, will have a thermal resistance of about 1/20th of the original value which makes a significant reduction in the overall interface thermal resistance.

Joint compounds are a formulation of fine zinc particles in a silicon oil which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Experience will indicate whether the quantity is sufficient, as excess will appear around the edges of the contact area. To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the assembly.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 7.I. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator and is therefore highly desirable despite the handling problems created by its affinity for foreign matter. Some sources of supply for joint compounds are shown in Appendix VIII.

Some users and heat sink manufacturers prefer not to use compounds. This necessitates use of a heat sink with lower thermal resistance which imposes additional cost, but which may be inconsequential when low power is being handled. Others design on the basis of not using grease, but apply it as an added safety factor, so that if improperly applied, operating temperatures will not exceed the design values.

MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semi, a thermocouple on the heat sink, and a means of applying and measuring dc power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are in poor agreement.

Consider the TO-220 package shown in Figure 7.3. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface

Table 7.I
Approximate Values for Interface Thermal Resistance and Other Package Data
(See Table 7.II for Case Number to JEDEC Outline Cross-Reference)

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heat sink.

Package Type and Data					Interface Thermal Resistance (°C/W)					
JEDEC Outline	Description	Recommended Mounting Hole and Drill Size	Machine Screw Size[1]	Torque In-Lb	Metal-to-Metal		With Insulator			See Note
					Dry	Lubed	Dry	Lubed	Type	
DO-4	10-32 Stud 7/16" Hex	0.188, #12	10-32	20	0.3	0.2	1.6	0.8	3 mil Mica	
DO-5	1/4-28 Stud 11/16" Hex	0.250, #1	1/4-28	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-21	Pressfit, 1/2"	See Figure 7.7	—	—	0.15	0.10	—	—	—	
TO-204 (TO-3)	Diamond Flange	0.140, #28	6-32	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-126	Thermopad 1/4" x 3/8"	0.133, #33	4-40	6	2	1.3	4.3	3.3	2 mil Mica	
TO-127	Thermopad 1/2" x 5/8"	0.140, #26	6-32	8	1.6	0.8	2.6	1.8	2 mil Mica	
TO-220AB	Thermowatt	0.140, #28	6-32	8	1.2	1	3.4	1.6	2 mil Mica	1, 2

NOTE 1. See Figures 7.8 and 7.11 for additional data on TO-204 and TO-220 packages.
NOTE 2. Screw not insulated.

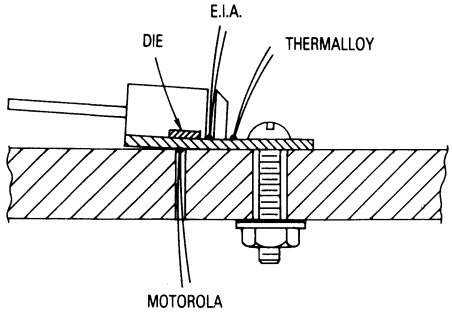


Figure 7.3. JEDEC TO-220 Package Mounted to Heat Sink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

slightly. To improve contact, Motorola TO-220 packages are slightly concave and use of a spreader bar under the screw lessens the lifting, but some is inevitable with a single-ended package.

The thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heat sink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The EIA location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the EIA location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance is constant for a given setup, junction-to-case values decrease and case-to-sink values increase as the case thermocouple readings become warmer.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semi package and the heat sink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heat sink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location could be close to the temperature at the EIA location as the lateral heat flow is generally small.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the semi is making contact to the heat sink, since heat sinks are measured from the point of semi contact to the ambient. Once the special heat sink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heat sink without thermal grease and no insulator. This error is small when compared to the heat dissipators often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant, and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heat sink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface

Table 7.II
Cross Reference Chart

Motorola Case Number to JEDEC Outline Number and Table 7.I Reference

Motorola Number	JEDEC Number		Reference In Table 7.I
	Old	New	
54-05	TO-3[2]	TO-204AE	TO-3
61-03	TO-3[2]	TO-204AE	TO-3
63-02	DO-4[2]	TO-203AE	DO-4
77-05	TO-126[1,2]	TO-225AA	TO-126
86-01	DO-4[1,2]	TO-203AA	DO-4
90-05	TO-127[1,2]	TO-225AB	TO-127
174-04	DO-21[1,2]	TO-208AA	DO-21
175-03	DO-5[1,2]	TO-203AB	DO-5
221A-04	TO-220AB	TO-220AB	TO-220AB
235-03	DO-5[1,2]	TO-203AB	DO-5
263-04	DO-5[1,2]	TO-203AB	DO-5
310-02	DO-21[1,2]	TO-208AA	DO-21
311-02	DO-5[1,2]	TO-203AB	DO-5
326-01	TO-3[2]	TO-204AA	TO-3

NOTE 1. Would fit within this family outline if registered with JEDEC.

NOTE 2. Not within all JEDEC outline dimensions. The data in Table 7.I and suggested mounting hardware and procedures generally apply.

resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use and yields reproducible results. At this printing, however, sufficient data to compare results to other methods is not available.

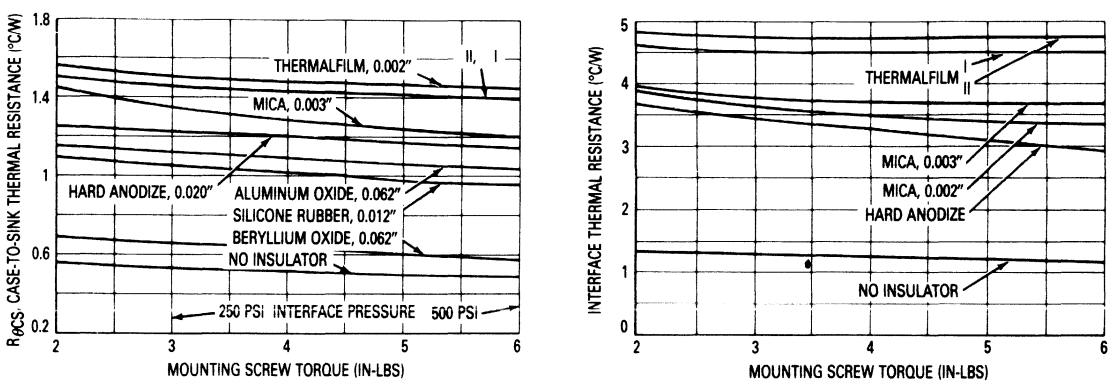
The only way to get accurate measurements of the interface resitance is to also test for junction-to-case thermal resistance at the same time. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

INSULATION CONSIDERATIONS

Since it is most expedient to manufacture power semiconductors with collectors or anodes electrically common to the case, the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, it is best to isolate the entire heat sink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heat sink. Where heat sink isolation is not possible, because of safety reasons or in instances where a chassis serves as a heat sink or where a heat sink is common to several devices, insulators are used to isolate the individual components from the heat sink.

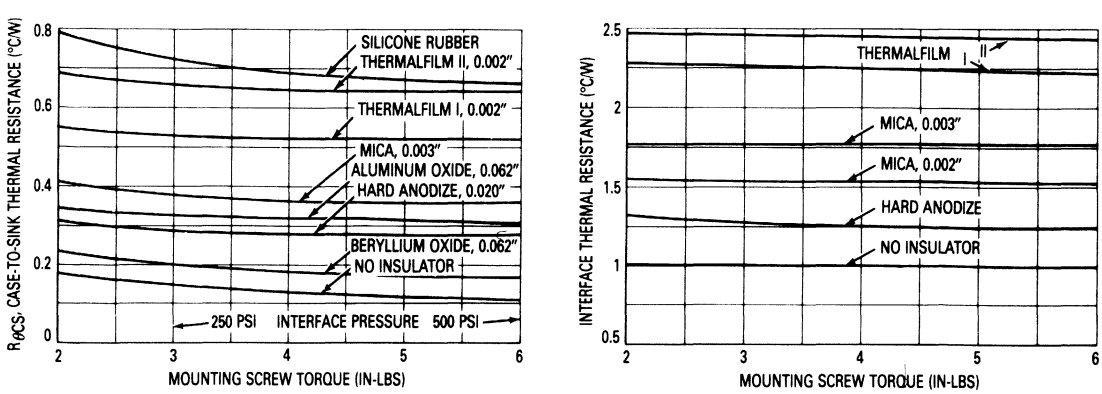
When an insulator is used, thermal grease assumes greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a markedly uneven surface. Reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torque applied to TO-3 and TO-220 packages, are shown in Figure 7.4 for bare surfaces and Figure 7.5 for greased surfaces. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case). When high power is handled, beryllium oxide is



(a). TO-3 (b). TO-220AB

Figure 7.4. Interface Thermal Resistance Without Thermal Grease as a Function of Mounting Screw Torque Using Various Insulating Materials



(a). TO-3 (b). TO-220AB

Figure 7.5. Interface Thermal Resistance Using Thermal Grease as a Function of Mounting Screw Torque Using Various Insulating Materials

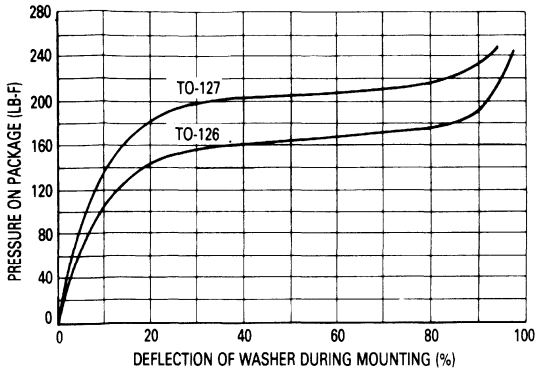


Figure 7.6. Characteristics of the Bell Compression Washers Designed for Use with Thermopad Semiconductors

unquestionably the best choice. Thermafilm is Thermalloy's tradename for a polyimide material which is also commonly known as Kapton*; this material is fairly popular for low power applications because it is low cost, withstands high temperatures and is easily handled, in contrast to mica which chips and flakes easily.

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly so that having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the breakdown voltage of the insulation system. Because of these factors, which are not amenable to analysis, high potential testing should be done on prototypes and a large margin of safety employed. In some situations, it may be necessary to substitute "empty" packages for the semiconductors to avoid shorting them or to prevent the semiconductors from limiting the voltage applied during the high potential test.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, let us look at the basic characteristics of several types of hardware.

COMPRESSION WASHERS

A very useful piece of hardware is the bell-type compression washer. As shown in Figure 7.6, it has the ability to maintain a fairly constant pressure over a wide range of physical deflection — generally 20% to 80% — thereby maintaining an optimum force on the package. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package or insulating washer caused by temperature changes. Bell type washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme.

Motorola washers designed for use with the Thermopad package maintain the proper force when properly secured. They are used with the large face contacting the packages.

MACHINE SCREWS

Machine screws and nuts form a trouble-free fastener system for all types of packages which have mounting holes. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of any of the Thermopad plastic package types as the screw heads are not sufficiently flat to provide properly distributed force.

SELF-TAPPING SCREWS

Under some conditions, sheet-metal screws are acceptable. However, during the tapping process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; a very unsatisfactory surface results. When used, a speed-nut must be used to secure a standard screw, or the type of screw must be used which roll-forms machine screw threads.

EYELETS

Successful mounting can also be accomplished with hollow eyelets provided an adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

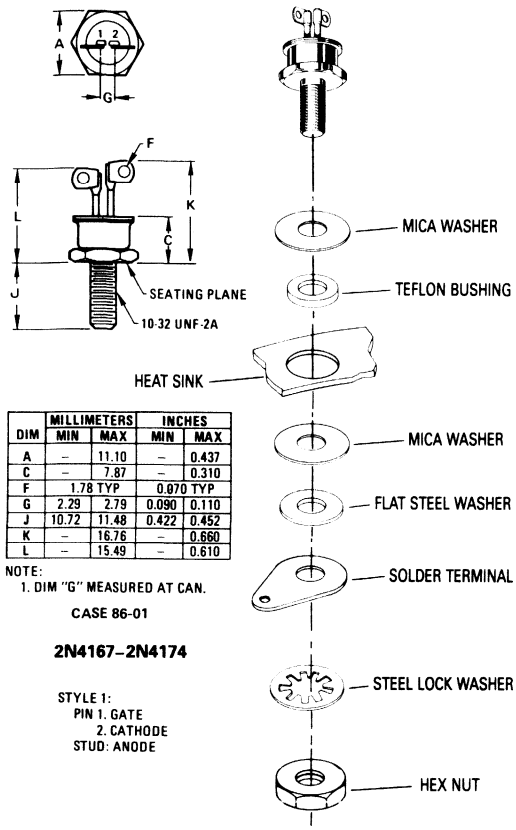
RIVETS

When a metal flange-mount package is being mounted directly to a heat sink, rivets can be used. Rivets are not a recommended fastener for any of the plastic packages except for the tab-mount type. Aluminum rivets are preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

INSULATORS AND PLASTIC HARDWARE

Because of its relatively low cost and low thermal resistance, mica is still widely used to insulate semiconductor packages from heat sinks despite its tendency to chip and flake. It has a further advantage in that it does not creep or flow so that the mounting pressure will not reduce with time in use. Plastic materials, particularly

*®DuPont



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	11.10	–	0.437
C	–	7.87	–	0.310
F	1.78 TYP		0.070 TYP	
G	2.29	2.79	0.090	0.110
J	10.72	11.48	0.422	0.452
K	–	16.76	–	0.660
L	–	15.49	–	0.610

NOTE:
1. DIM "G" MEASURED AT CAN.

CASE 86-01

2N4167–2N4174

STYLE 1:
PIN 1. GATE
2. CATHODE
STUD: ANODE

Figure 7.7. Mounting Details for Stud-Mounted Semiconductors

Teflon*, will flow. When plastic materials form part of the fastening system, a compression washer is a valuable addition which assures that the assembly will not loosen with time.

FASTENING TECHNIQUES

Each of the various types of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heat sinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Manufacturers which provide heat sinks for general use and other associated hardware are listed in Appendix VIII. Manufacturer's catalogs should be consulted to obtain more detailed information. Motorola also has mounting hardware available for a number of different packages. Consult the Hardware Data Sheet for dimensions of the components and part numbers.

Specific fastening techniques are discussed in the remainder of this chapter for the following categories of semiconductor package.

1) Stud mount: 10-32 UNF-24
   1/4-28 UNF-24
2) Flange mount: TO-3
3) Pressfit: DO-21
4) Thermopad®: TO-225AA/225AB or 225 Family
5) Thermowatt®: TO-220 Family

STUD MOUNT

Mounting errors with stud-mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heat sink hole. Both these practices may cause the hex base to warp, which may crack the semiconductor die. The best fastening method is to use a nut and washer; the details are shown in Figure 7.7.

FLANGE MOUNT

Few known mounting difficulties exist with this type of package. The rugged base and distance between die and mounting holes combine to make it extremely difficult to warp, unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. A typical mounting installation is shown in Figure 7.8. Machine screws, self-tapping

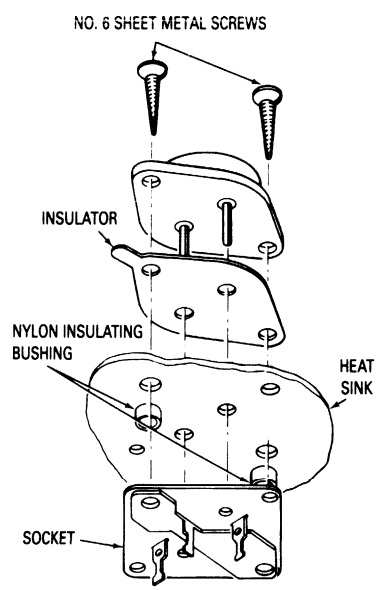
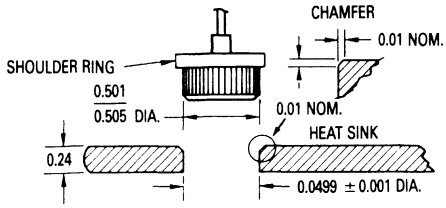
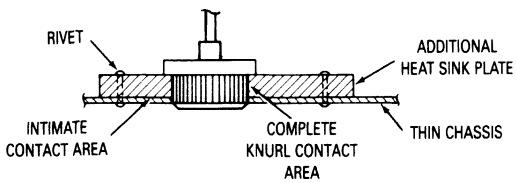


Figure 7.8. Mounting Details for Flat-Base Mounted Semiconductors (TO-204AE Shown)

*Trademark E.I. DuPont



Heat Sink Mounting



Thin-Chassis Mounting

The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heat sink material. Recommended hardnesses are: copper—less than 50 on the Rockwell F scale; aluminum—less than 65 on the Brinell scale. A heat sink as thin as 1/8" may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

Figure 7.9. Mounting Details for Press-Fit Semiconductors

screws, eyelets, or rivets may be used to secure the package.

PRESS FIT

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 7.9. A special fixture meeting the necessary requirements is a must.

THERMOPAD

The Motorola Thermopad plastic power packages have been designed to feature minimum size with no compromise in thermal resistance. This is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting, i.e., plastic is molded enveloping the chip but leaving the mounting hole open. The benefits of this construction are obtained at the expense of paying strict attention to the mounting procedure. Success in mounting Thermopad devices depends largely upon using a compression washer which provides a controllable pressure across a large bearing surface. Having a small hole with no chamber and a flat, burr-free, well-finished heat sink are also important requirements.

Several types of fasteners may be used to secure the Thermopad package; machine screws, eyelets, or clips are preferred. With screws or eyelets, a bell compression washer should be used which applies the proper force to the package over a fairly wide range of deflection. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of the recommended washers are shown in Figure 7.6

Figure 7.10 shows details of mounting TO-225AA or TO-225AB devices. Use of the clip requires caution to insure that adequate mounting force is applied. When electrical isolation is required, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

THERMOWATT

The popular TO-220 Thermowatt package also requires attention to mounting details. Figure 7.11 shows suggested mounting arrangements and hardware. The rectangular washer shown in Figure 7.11(a) is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

In situations where the Thermowatt package is making direct contact with the heat sink, an eyelet may be used, provided sharp blows or impact shock is avoided.

FREE AIR AND SOCKET MOUNTING

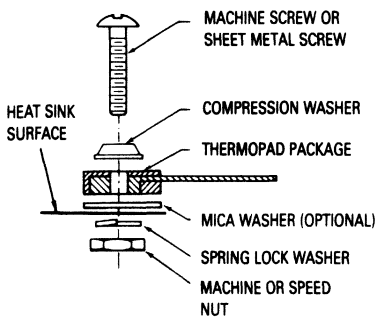
In applications where average power dissipation is of the order of a watt or so, power semiconductors may be

mounted with little or no heat-sinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked glass-to-metal seals around the leads. The plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heat sink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance.

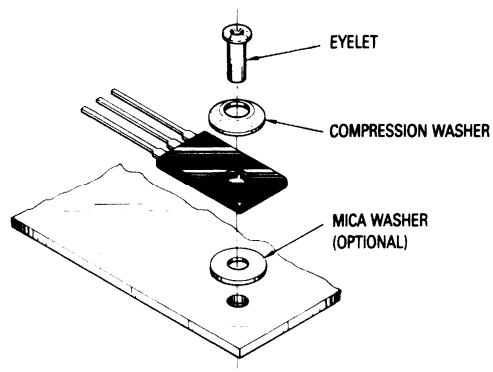
In many situations, because its leads are fairly heavy, the TO-225AB package has supported a small heat sink; however, no definitive data is available. When using a small heat sink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 7.12. The arrangement in Figure 7.12(a) could be used with any plastic package, but the scheme of part Figure 7.12(b) is more practical with Case 77 or Case 90 Thermopad devices. With the other package types, mounting the transistor on top of the heat sink is more practical.

In certain situations, in particular where semiconductor testing is required, sockets are desirable. Manufacturers

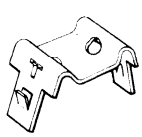
1



(a). Machine Screw Mounting

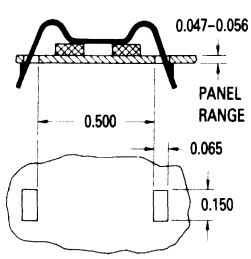


(b). Eyelet Mounting

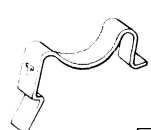


PART C52825-011

MATERIAL: HEAT-TREATED SPRING
STEEL 0.011 THICKNESS



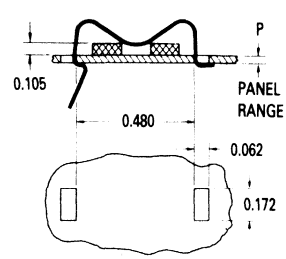
TO-225AB Clip



PARTS C50272-011 AND C51451-011

MATERIAL: HEAT-TREATED SPRING
STEEL 0.011 THICKNESS

Part	P
C50272-011	0.046–0.055
C51451-011	0.030–0.034



TO-225AA Clip

(c). Tinnerman Clips (Eaton Corp.)

Figure 7.10. Recommended Mounting Arrangements for TO-225AA and TO-225AB Thermopad Packages

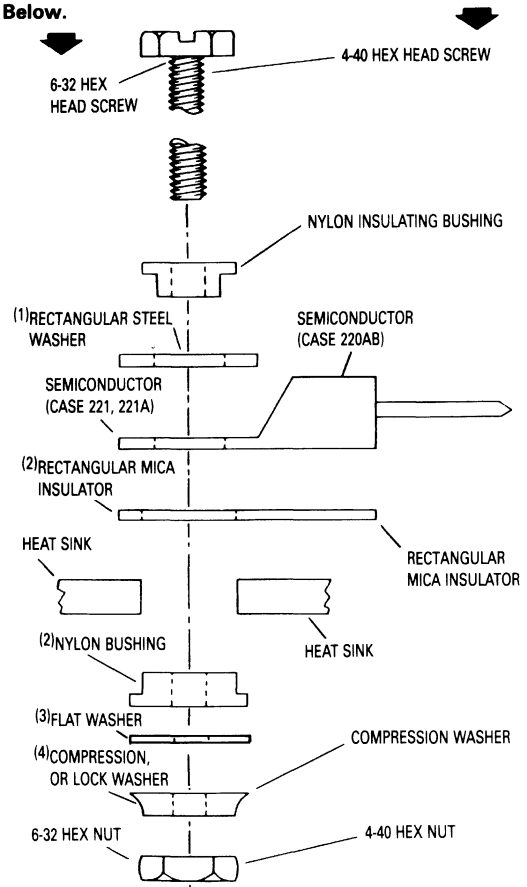
have provided sockets for all the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details.

(a). Preferred Arrangement for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Use Parts Listed Below.

(b). Alternate Arrangement for Isolated Mounting when Screw must be at Heat Sink Potential. 4-40 Hardware is Used.

Use Parts Listed Below.



(1) USED WITH THIN CHASSIS AND/OR LARGE HOLE
(2) USED WHEN ISOLATION IS REQUIRED
(3) REQUIRED WHEN NYLON BUSHING AND LOCK WASHER ARE USED
(4) COMPRESSION WASHER PREFERRED WHEN PLASTIC INSULATING MATERIAL IS USED

TORQUE REQUIREMENTS
INSULATED 0.68 N-M (6 IN-LBS) MAX
NONINSULATED 0.9 N-M (8 IN-LBS) MAX

Figure 7.11. Mounting Arrangements for Thermowatt Packages

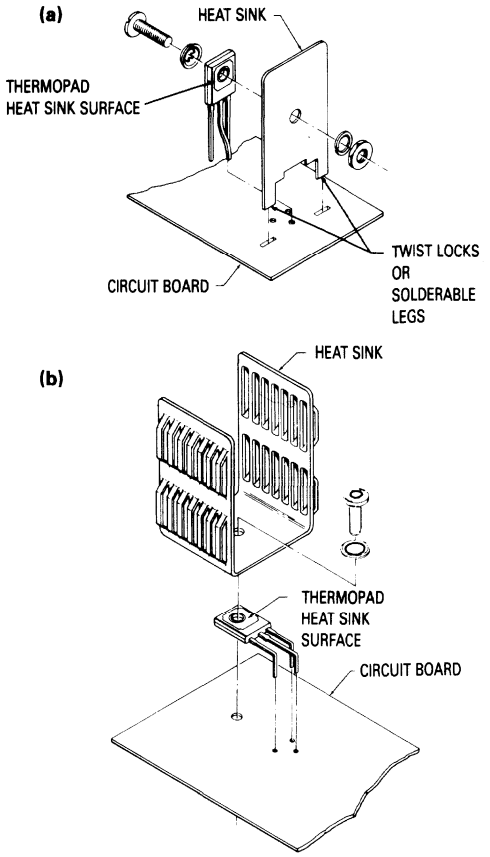


Figure 7.12. Methods of Using Small Heat Sinks with Plastic Semiconductor Packages

HANDLING PINS, LEADS, AND TABS

The pins and lugs of metal-packaged devices are not designed for any bending or stress. If abused, the glass-to-metal seals could crack. Wires may be attached using sockets, crimp connectors, or solder, provided the data-sheet ratings are observed.

The leads and tabs of the plastic packages are more flexible and can be reshaped, although this is not a recommended procedure for users to do. In some cases, a heat sink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola. Preformed leads remove the risk of device damage caused by bending from the users.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, it must be supported between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case while bending with the fingers or another pair

of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A lead-bend radius greater than 1/16 inch is advisable for TO-225AA, 1/10 inch for TO-225AB and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. An acceptable lead-forming method that provides this relief is to incorporate an S-bend into the lead. Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices.

Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline may cause the encapsulant to swell, possibly damaging the transistor die. Likewise, chlorinated Freon solvents are unsuitable, since they may cause the outer package to dissolve and swell.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if the packages are free-standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area or thyristor di/dt limits, as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix VII). A fine wire thermocouple should be used, such as #32AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

GRAPHICAL INTEGRATION

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation.

SUBSTITUTION

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

CHAPTER 8
RELIABILITY AND QUALITY

As the price of semiconductor devices decreases, reliability and quality have become increasingly important in selecting a vendor. In many cases these considerations even outweigh price, delivery and service.

The reason is that the cost of device fallout and warranty repairs can easily equal or exceed the original cost of the devices. Consider the example shown in Figure 8.1. Although the case is simplistic, the prices and costs are realistic by today's standards. In this case, the cost of failures raised the device cost from 15 cents to 21 cents, an increase of 40%. Clearly, then, investing in quality and reliability can pay big dividends.

With nearly three decades of experience as a major semiconductor supplier, Motorola is the largest manufacturer of discrete semiconductors in the world today. Since semiconductor prices are strongly influenced by manufacturing volume, this leadership has permitted Motorola to be strongly competitive in the marketplace while making massive investments in equipment, processes and procedures to guarantee that the company's after-purchase costs will be among the lowest in the industry. As a result of the procedures, Motorola is projecting an outgoing quality level of less than 3 PPM by 1992.

Given:
Purchase = 100,000 components @ 15¢ each
Assumptions: Line Fallout = 0.1%
Warranty Failures = 0.01%

Components Cost =	100,000 x 15¢ =	$15,000
Line Fallout Cost = @ $40 per repair	100 x $40 =	4,000
Warranty Cost = @ $200 per repair	10 x $200 =	2,000
		$21,000

Adjusted Cost
Per Component = $21,000 ÷ 100,000 = 21¢

Definitions:
Line Fallout = Module or subassembly failure requiring troubleshooting, parts replacement and retesting
Warranty Failure = System field failure requiring in warranty repair

Figure 8.1. Component Costs to the User (including line fallout and warranty costs)

Quality and reliability are two essential elements in order for a semiconductor company to be successful in the marketplace today. Quality and reliability are interrelated because reliability is quality extended over the expected life of the product.

Quality is the assurance that a product will fulfill customers' expectations.

Reliability is the probability that a product will perform its intended function satisfactorily for a prescribed life under certain stated conditions.

The quality and reliability of Motorola thyristors are achieved with a four step program:

1) Thoroughly tested designs and materials
2) Stringent in-process controls and inspections
3) Process average testing along with 100% quality assurance redundant testing
4) Reliability verifications through audits and reliability studies

ESSENTIALS OF RELIABILITY

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of trouble free service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. Reliability can be redefined as the probability of failure free performance, under a given manufacturer's specifications, for a given period of time. The failure rate of semiconductors in general, when plotted versus a long period of time, exhibit what has been called the "bath tub curve" (Figure 8.2).

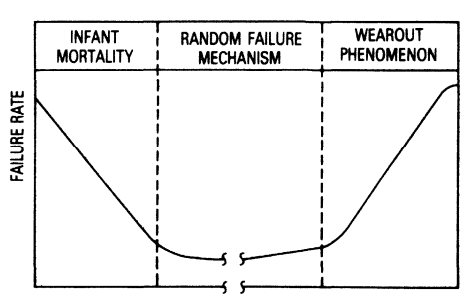


Figure 8.2. Failure Rate of Semiconductor

RELIABILITY MECHANICS

Since reliability evaluations usually involve only samples of an entire population of devices, the concept of the central limit theorem applies and a failure rate is calculated using the λ^2 distribution through the equation:

$$\lambda \leq \frac{\lambda^2 (\alpha, 2r + 2)}{2\ nt}$$

λ^2 = chi squared distribution

where $\alpha = \frac{100 - cl}{100}$

λ = Failure rate

cl = Confidence limit in percent

r = Number of rejects

n = Number of devices

t = Duration of tests

The confidence limit is the degree of conservatism desired in the calculation. The central limit theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate, and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 8.3).

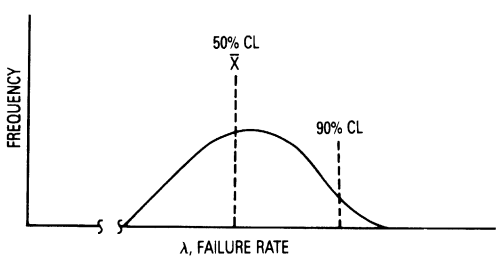


Figure 8.3. Confidence Limits and the Distribution of Sample Failure Rates

The term (2r + 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to λ^2 tables. The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the λ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing have shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_o(t)e^{-o/KT}$$

Where R(t) = reaction rate as a function of time and temperature

R_o = A constant

t = Time

T = Absolute temperature, °Kelvin (°C + 273°)

o = Activation energy in electron volts (ev)

K = Boltzman's constant = 8.62×10^{-5} ev/°K

This equation can also be put in the form:

AF = Acceleration factor

T2 = User temperature

T1 = Actual test temperature

The Arrhenius equation states that reaction rate increases exponentially with the temperature. This produces a straight line when plotted on log-linear paper with a slope expressed by o. o may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The overall activation energy exhibited by Motorola thyristors is 1 ev.

RELIABILITY QUALIFICATIONS/EVALUATIONS OUTLINE:

Some of the functions of Motorola Reliability and Quality Assurance Engineering are to evaluate new products for introduction, process changes (whether minor or major), and product line updates to verify the integrity and reliability of conformance, thereby ensuring satisfactory performance in the field. The reliability evaluations may be subjected to a series of extensive reliability testing, such as in the tests performed section, or special tests, depending on the nature of the qualification requirement.

AVERAGE OUTGOING QUALITY (AOQ)

With the industry trend to average outgoing qualities (AOQ) of less than 100 PPM, the role of device final test, and final outgoing quality assurance have become a key ingredient to success. At Motorola, all parts are 100% tested to process average limits then the yields are monitored closely by product engineers, and abnormal areas of fallout are held for engineering investigation. Motorola also 100% redundant tests all dc parameters again after marking the device to further reduce any mixing problems associated with the first test. Prior to shipping, the parts are again sampled, tested to a tight sampling plan by our Quality Assurance department, and finally our outgoing final inspection checks for correct paperwork, mixed product, visual and mechanical inspections prior to packaging to the customers.

AVERAGE OUTGOING QUALITY (AOQ)

$$AOQ = \text{Process Average} \times \text{Probability of Acceptance} \times 10^6 \text{ (PPM)}$$

$$\text{Process Average} = \frac{\text{No. of Reject Devices}}{\text{No. of Devices Tested}}$$

$$\text{Probability of Acceptance} = \left(1 - \frac{\text{No. of Lots Rejected}}{\text{No. of Lots Tested}}\right)$$

$$10^6 = \text{To Convert to Parts Per Million}$$

$$AOQ = \frac{\text{No. of Reject Devices}}{\text{No. of Devices Tested}} \times \left(1 - \frac{\text{No. of Lots Rejected}}{\text{No. of Lots Tested}}\right) \times 10^6 \text{(PPM)}$$

Current AOQ levels (1988) are less than 50 PPM. The projected goal, by 1992, is less than 3 PPM, a defect rate so low that it becomes virtually invisible to the user. Figure 8.4 shows AOQ of Motorola Thyristors.

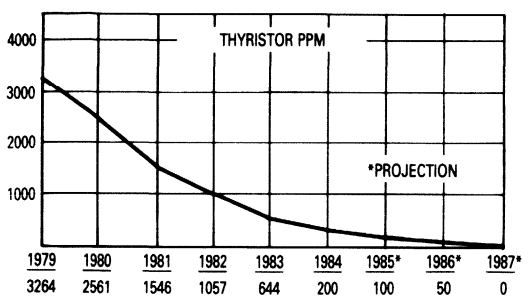
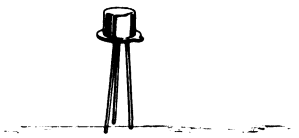


Figure 8.4. Average Outgoing Quality (AOQ) of Motorola Thyristors

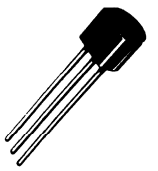
THYRISTOR RELIABILITY

The reliability data described herein applies to Motorola's extensive offering of thyristor products for low and medium current applications. The line includes not only the pervasive Silicon Controlled Rectifiers (SCRs) and TRIACs, but also a variety of Unijunction Transistors (UJTs), Programmable Unijunction Transistors (PUTs), Silicon Bidirectional Switches (SBSs), SIDACs and other associated devices used for SCR and TRIAC triggering purposes. Moreover, these devices are available in different package styles with overlapping current ranges to provide an integral chip-and-package structure that yields lowest cost, consistent with the overriding consideration of high reliability.

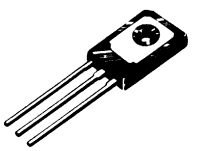
The various packages and the range of electrical specifications associated with the resultant products are shown in Figure 8.5.



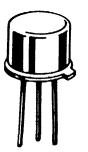
Case 22-03/TO-206AA (TO-18)
Devices Available:
SCRs, UJTs, PUTs
Current Range: to 0.5 A
Voltage Range: 25 to 200 V



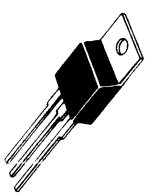
Case 29-04/TO-226AA (TO-92)
Devices Available:
SCRs, TRIACs, UJTs, PUTs, SBSs
Current Range: to 0.8 A
Voltage Range: 25 to 600 V



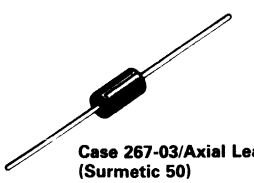
Case 77-05/TO-225AA (TO-126)
Devices Available:
SCRs, TRIACs
Current Range: to 4 A
Voltage Range: 25 to 600 V



Case 79-04/TO-205AD (TO-39)
Devices Available:
SCRs
Current Range: to 1.6 A
Voltage Range: 25 to 600 V



Case 221A-04/TO-220AB
Devices Available:
SCRs, TRIACs
Current Range: to 40 A
Voltage Range: 50 to 1000 V



Case 267-03/Axial Lead (Surmetic 50)
Devices Available:
SIDAC
Voltage Range: 104 to 240 V

Case 311-02/ Press Fit/Stud
Devices Available:
SCRs, TRIACs
Current Range: to 55 A
Voltage Range: 25 to 800 V

Figure 8.5. Motorola Thyristor Packages

To evaluate the reliability of these structures, production line samples from each type of package are being subjected to a battery of accelerated reliability tests deliberately designed to induce long-term failure. Though the tests are being conducted on a continuing basis, the results so far are both meaningful and impressive. They are detailed on the following pages in the hope that they will provide for the readers a greater awareness of the potential for thyristors in their individual application.

THYRISTOR CONSTRUCTION THROUGH A TIME TESTED DESIGN AND ADVANCED PROCESSING METHODS

A pioneer in discrete semiconductor components and the world's largest supplier thereof, Motorola has pyramided continual process and material improvements into thyristor products whose inherent reliability meets the most critical requirements of the market.

These improvements are directed towards long-term reliability in the most strenuous applications and the most adverse environments.

1

DIE GLASSIVATION

All Motorola thyristor die are glass-sealed with a Motorola patented passivation process making the sensitive junctions impervious to moisture and impurity penetration. This imparts to low-cost plastic devices the same freedom from external contamination formerly associated only with hermetically sealed metal packages. Thus, metal encapsulation is required primarily for higher current devices that would normally exceed the power-dissipation capabilities of plastic packages — or for applications that specify the hermetic package.

HIGHLY MECHANIZED ASSEMBLY

Motorola uses many techniques to ensure quality manufacturing of its thyristor products. A few of the newest techniques are (1) all diffusion steps are performed by microprocessor-controlled diffusion tubes, (2) four point probes are used to verify resistivity at each step during wafer processing, (3) all chips are individually probed to their electrical specifications, (4) wafer preparation for assembly includes laser scribing to separate the die while in wafer form, (5) assembly furnaces are automated to perform automatic insertion and removal of assembly fixtures.

VOID-FREE PLASTIC ENCAPSULATION

A fifth generation plastic package material, combined with improved copper piece-part designs, maximize package integrity during thermal stresses. The void-free encapsulation process imparts to the plastic package a mechanical reliability (ability to withstand shock and vibration) even beyond that of metal packaged devices.

IN-PROCESS CONTROLS AND INSPECTIONS

INCOMING INSPECTIONS

Apparently routine procedures, inspection of incoming parts and materials, are actually among the most critical segments of the quality and reliability assurance program. That's because small deviations from materials specifications can traverse the entire production cycle before being detected by outgoing Quality Control, and, if undetected, could affect long-term reliability. At Motorola, piece-part control involves the services of three separate laboratories . . . Radiology, Electron Optics and Product Analysis. All three are utilized to insure product integrity:

Raw Wafer Quality, in terms of defects, orientation, flatness and resistivity;

Physical Dimensions, to tightly specified tolerances;
Metal Hardness, to highly controlled limits;
Gaseous Purity and Doping Level;
Mold Compounds, for void-free plastic encapsulation.

IN-PROCESS INSPECTIONS

As illustrated in Figure 8.6, every major manufacturing step is followed by an appropriate in-process QA inspection. Quality control in wafer processing, assembly and final test impart to Motorola standard thyristors a reliability level that easily exceeds most industrial, consumer and military requirements . . . built-in quality assurance aimed at insuring failure-free shipments of Motorola products.

RELIABILITY AUDITS

Reliability audits are performed following assembly. Reliability audits are used to detect process shifts which can have an adverse effect on long-term reliability. Extreme stress testing on a real-time basis, for each product run, uncovers process abnormalities that may have escaped the stringent in-process controls. Typical tests include HTRB/FB (high-temperature reverse bias and forward bias) storage life and temperature cycling. When abnormalities are detected, steps are taken to correct the process.

OUTGOING QC

The most stringent in-process controls do not guarantee strict adherence to tight electrical specifications. Motorola's 100% electrical parametric test does — by eliminating all devices that do not conform to the specified characteristics. Additional parametric tests, on a sampling basis, provide data for continued improvement of product quality. And to help insure safe arrival after shipment, antistatic handling and packaging methods are employed to assure that the product quality that has been built in stays that way.

From rigid incoming inspection of piece parts and materials to stringent outgoing quality verification, assembly and process controls encompass an elaborate system of test and inspection stations that ensure step-by-step adherence to a prescribed procedure designed to yield a high standard of quality.

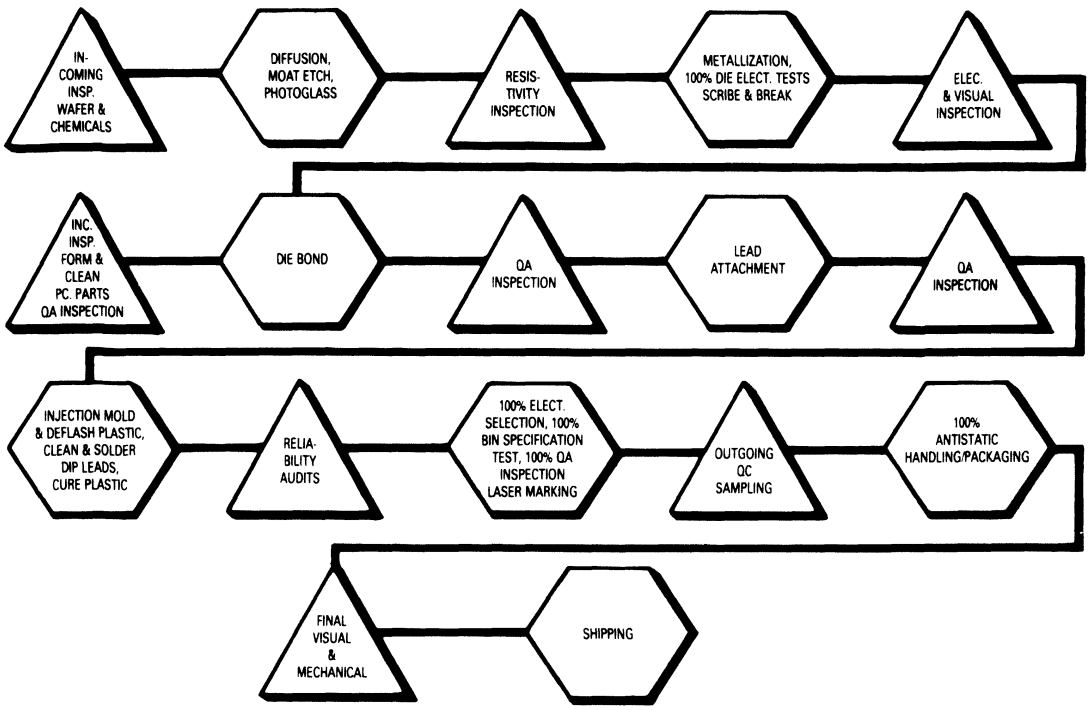


Figure 8.6. In-Process Quality Assurance Inspection Points for Thyristors

RELIABILITY TESTS

Only actual use of millions of devices, under a thousand different operating conditions, can conclusively establish the reliability of devices under the extremes of time, temperature, humidity, shock, vibration and the myriads of other adverse variables likely to be encountered in practice. But thorough testing, in conjunction with rigorous statistical analysis, is the next-best thing. The series of torture tests described in this document instills a high confidence level regarding thyristor reliability. The tests are conducted at maximum device ratings and are designed to deliberately stress the devices in their most susceptible failure modes. The severity of the tests compresses into a relatively short test cycle the equivalent of the stresses encountered during years of operation under more normal conditions. The results not only indicate the degree of reliability in terms of anticipated failures; they trigger subsequent investigations into failure modes and failure mechanisms that serve as the basis of continual improvements. And they represent a clear-cut endorsement that, for Motorola thyristors, low-cost and high quality are compatible attributes.

BLOCKING LIFE TEST

This test is used as an indicator of long-term operating reliability and overall junction stability (quality). All semiconductor junctions exhibit some leakage current under reverse-bias conditions. Thyristors, in addition, exhibit leakage current under forward-bias conditions in the off state. As a normal property of semiconductors, this junction leakage current increases proportionally with temperature in a very predictable fashion.

Leakage current can also change as a function of time — particularly under high-temperature operation. Moreover, this undesirable "drift" can produce catastrophic failures when devices are operated at, or in excess of, rated temperature limits for prolonged periods.

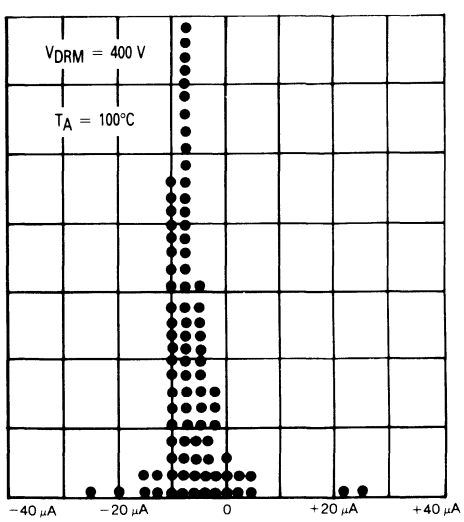
The blocking life test operates representative numbers of devices at rated (high) temperature and reverse-bias voltage limits to define device quality (as measured by leakage drifts) and reliability (as indicated by the number of catastrophic failures*). The results of these tests are shown in Table 8.I. Table 8.II shows leakage-current drift after 1000 hours HTRB.

Table 8.I. Blocking Life Test High Temperature Reverse Bias (HTRB) and High Temperature Forward Bias (HTFB)

Case	Test Conditions T_A @ Rated Voltage	Sample Size	Duration (Hours)	Total Device Hours	Catastrophic Failures*
29-04/TO-226AA (TO-92)	100°C	1000	1000	1,000,000	1
77-05/TO-225AA (TO-126)	110°C	1000	1000	1,000,000	0
221A-04/TO-220AB	100°C	1000	1000	1,000,000	0
311-02/Press Fit/Stud	100°C	200	1000	200,000	0
22-03/TO-206AA (TO-18)	110°C	200	1000	200,000	0
79-04/TO-205AD (TO-39)	110°C	150	1000	150,000	0
267-03/Axial Lead (Surmetic 50)	125°C	150	1000	150,000	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

Table 8.II. Leakage-Current Drift after 1000 Hours HTRB



Leakage Shift from Initial Value

The favorable blocking-life-test drift results shown here are attributed to Motorola's unique "glassivated junction" process which imparts a high degree of stability to the devices.

HIGH TEMPERATURE STORAGE LIFE TEST

This test consists of placing devices in a high-temperature chamber. Devices are tested electrically prior to exposure to the high temperature, at various time intervals during the test, and at the completion of testing. Electrical readout results indicate the stability of the devices, their potential to withstand high temperatures, and the internal manufacturing integrity of the package. Readouts at the various intervals offer information as to the time period in which failures occur. Although devices are not exposed to such extreme high temperatures in the field, the purpose of this test is to accelerate any failure mechanisms that could occur during long periods at actual storage temperatures. Results of this test are shown in Table 8.III.

Table 8.III. High Temperature Storage Life

Case	Test Conditions	Sample Size	Duration (Hours)	Total Device Hours	Catastrophic Failures*
29-04/TO-226AA (TO-92)	T_A 150°C	1000–2000	400	1,500,000	0
77-05/TO-225AA (TO-126)	**	1000–2000	350	550,000	0
221A-04/TO-220		1000	300	300,000	0
311-02/Press Fit/Stud		1000	125	125,000	0
22-03/TO-206AA (TO-18)		1000–2000	400	600,000	0
79-04/TO-205AD (TO-39)		1000–2000	100	150,000	0
267-03/Axial Lead (Surmetic 50)		1000	100	100,000	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

**Same for all.

STRESS TESTING — POWER CYCLING AND THERMAL SHOCK

POWER CYCLING TEST

How do the devices hold up when they are repeatedly cycled from the off state to the on state and back to the off state under conditions that force them to maximum rated junction temperature during each cycle? The Power Cycling Test was devised to provide the answers.

In this test, devices are subjected to full-rated, on-state power until rated junction temperature (T_J) has been reached. The devices are then turned off and T_J decreases to near ambient, at which time the cycle is repeated.

This test is important to determine the integrity of the chip and lead frame assembly since it repeatedly stresses the devices to their maximum ratings. It is unlikely that these worst-case conditions would be continuously encountered in actual use. Any reduction in T_J results in an exponential increase in operating longevity. Table 8.IV shows the results of power cycling.

Table 8.IV. Power Cycling

Case	Test Conditions	Sample Size	Duration (Cycles)	Total Device Cycles	Catastrophic Failures*
29-04/TO-226AA (TO-92)	$I_{T(rms)}$ = Maximum Rating ΔT_J = 70°C (30°C to 100°C) or ΔT_J = 95°C (30°C to 125°C) Depending on Maximum T_J Rating Force Air Cooling **t_{off} = Adjust per device type	100 200 100	5,000 10,000 20,000	500,000 3,000,000 2,000,000	0 1 0
77-05/TO-225AA (TO-126)		622	10,000	6,220,000	0
221A-04/TO-220		200 200 100	5,000 10,000 20,000	1,000,000 2,000,000 2,000,000	0 0 0
311-02/Press Fit/Stud 22-03/TO-206AA (TO-18) 79-04/TO-205AD (TO-39)		50 75	10,000 10,000	500,000 750,000	0 0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.
**Typical 4 seconds OFF.

THERMAL SHOCK CONDITIONS BEYOND THE NORM

Excesses in temperature not only cause variations in electrical characteristics, they can raise havoc with the mechanical system. Under temperature extremes, contraction and expansion of the chip and package can cause physical dislocations of mechanical interfaces and induce catastrophic failure.

To evaluate the integrity of Motorola thyristors under the most adverse temperature conditions, they are subjected to two different thermal shock tests: liquid-to-liquid and air-to-air.

LIQUID-TO-LIQUID (GLASS STRAIN)

This thermal shock test is performed for the same reasons as the temperature cycling test, however, the extreme changes in temperature are more sudden. This is an especially useful tool for evaluating the metal to nonmetal interface. Results of this test are shown in Table 8.V.

AIR-TO-AIR (TEMPERATURE CYCLING)

This thermal shock test is conducted to determine the ability of the devices to withstand exposure to extreme high and low temperature environments and to the shock of alternate exposures to the temperature extremes. Results of this test are shown in Table 8.VI.

Table 8.V. Liquid-to-Liquid

Case	Test Conditions	Sample Size	Number of Cycles	Catastrophic Failures*
29-04/TO-226AA (TO-92)	Mil Std 750, Method 1056-1 0°C to +100°C Dwell Time — 15 seconds Immediate Transfer	950	300	0
77-05/TO-225AA		200	300	0
221A-04/TO-220 (TO-126)		300	300	◀0
22-03/TO-206AA (TO-18)		75	300	0
79-04/TO-205AD (TO-39)		75	100	0
311-02/Press Fit/Stud		75	100	0
267-03/Axial Lead (Surmetic 50)		75	300	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

Table 8.VI. Air-to-Air

Case	Test Conditions	Sample Size	Number of Cycles	Total Device Cycles	Catastrophic Failures*
29-04/TO-226AA (TO-92)	−40°C or −65°C to +150°C Dwell — 15 minutes at each extreme Immediate Transfer	900	400	360,000	0
77-05/TO-225AA (TO-126)		500	400	200,000	0
221A-04/TO-220		400	400	160,000	0
311-02/Press Fit/Stud		150	400	60,000	0
22-03/TO-206AA (TO-18)		300	400	120,000	0
79-04/TO-205AD (TO-39)		75	50	3,750	0
267-03/Axial Lead (Surmetic 50)		100	400	40,000	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

1

ENVIRONMENTAL TESTING

MOISTURE TESTS

Humidity has been a traditional enemy of semiconductors, particularly plastic packaged devices. Most moisture-related degradations result, directly or indirectly, from penetration of moisture vapor through passivating materials, and from surface corrosion. At Motorola, this erstwhile problem has been effectively controlled through the use of a unique junction "glassivation" process and selection of package materials. The resistance to moisture-related failures is indicated by the tests described here.

BIASED HUMIDITY TEST

This test was devised to determine the resistance of component parts and constituent materials to the combined deteriorative effects of prolonged operation in a high-temperature/high-humidity environment. H^3TRB test results are shown in Table 8.VII.

MOISTURE RESISTANCE TEST

This test evaluates the deteriorative effects of temperature cycling and high humidity under accelerated conditions simulating tropical environments. During this test, devices are subjected to alternate periods of condensation and drying, which "breathe" moisture into nonhermetic packages and accelerate the development of corrosion. Increased effectiveness is further obtained by use of high temperatures which intensify the effects of humidity. Test results are shown in Table 8.VIII.

Table 8.VII. Biased Humidity Test
High humidity, high Temperature, reverse bias (H^3TRB)

Case	Test Conditions	Sample Size	Duration Hours	Total Device Hours	Catastrophic Failures*
29-04/TO-226AA (TO-82)	Relative Humidity 85% T_A = 85°C Reverse Voltage-Rated or 200 V Maximum	400	500–1000	300,000	0
77-05/TO-225AA		200	500–1000	150,000	0
221A-04/TO-220		100	500–1000	75,000	0
22-03/TO-206AA		100	500–100	75,000	0
267-03/Axial Lead (Surmetic 50)		30	1000	30,000	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

Table 8.VIII. Moisture Resistance Test

Case	Test Conditions	Sample Size	Duration Hours	Catastrophic Failures*
29-04/TO-226AA (TO-92)	Mil. Std. 750 Method 1021 Relative Humidity 92–98% Temperature Cycle — Cycle Time 24 Hours	100	960	0
77-05/TO-225AA (TO-126)		100	960	0
221A-04/TO-220		50	720	0
267-03/Axial Lead (Surmetic 50)		40	960	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

MECHANICAL TESTING

VIBRATION TEST (VARIABLE FREQUENCY)

Vibration, by causing loosening of parts or relative motion between parts in the sample, can produce objectionable operating characteristics, noise, wear and physical distortion, and often results in fatigue and failure of mechanical parts.

This test determines the effects of vibration within the predominate frequency ranges and magnitudes that may be encountered by thyristors during field service. Most vibration encountered in field service is not of a simple harmonic nature. Nevertheless, tests based on vibrations of this type have proved satisfactory for determining critical frequencies, modes of vibration and other data necessary for planning protective steps against the effects of undue vibration. Test results are shown in Table 8.IX.

Table 8.IX

Test Conditions Mil-S-750, Method 2056	Case	Duration (Minutes)	Sample Size	Catastrophic Failures*
20 G's in X_1 Y_1 Z_1 Axis	77-05	48	100	0
	221A-04	48	150	0
	29-04	48	340	0
	22-03	48	75	0
	79-04	48	—	—
	311-02		25	0
	267-03	48	84	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

SOLVENTS TEST

Almost invariably, in actual practice, plastic thyristors are subjected to a cleaning solution to remove residue flux or solvents utilized during circuit manufacturing. Frequently, the cleaning solution is highly chlorinated and the devices are completely immersed in an elevated temperature bath. Motorola plastic thyristors subjected to hot chlorinated baths have proved highly resistant to the potentially damaging effects of this chemical.

Alcohols, water baths, freon, etc., produce no known latent failure mechanisms. Tests have indicated that Motorola plastic packages will withstand all cleaning agents commonly used. Solvents' test results are shown in Table 8.X.

Table 8.X.

Test Conditions	Case	Number of Minutes	Sample Size	Catastrophic Failures*
Chlorothene Immersion at T_A = 50°C	221A-04	30	100	0
	77-05	30	50	0
	29-04	30	50	0
	267-03	30	50	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

CONSTANT ACCELERATION TEST

The Constant Acceleration test is used to determine the effects of a centrifugal force on semiconductor devices. This test is designed to indicate types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests. The results of this test are shown in Table 8.XI.

Table 8.XI

Test conditions Mil-S 750, Method 2006	Case	Duration (Minutes)	Sample Size	Catastrophic Failures*
10,000 G's in Y_1 Y_2 Axis	77-05	1	100	0
	29-04	1	340	0
	221A-04	1	150	0
	22-03	1	75	0
	267-03	1	84	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

DROP SHOCK TEST

Drop shock testing simulates the stress encountered by a device during rough handling, transportation or field operation. Shocks of this type may disturb operating characteristics or may cause catastrophic failures. Motorola plastic thyristors exhibited extremely good resistance to mechanical shock. Results are shown in Table 8.XII.

Table 8.XII

Test Conditions Mil-STD-202, Method 202	Case	Sample Size	Catastrophic Failures*
X_1, Y_1 Axis 15 G's, 10 Blows	77-05	100	1
	221A-04	150	0
	29-04	340	0
	311-02	25	0
	22-03	75	0
	267-03	84	0

*Failures are at maximum rated values. The severe nature of these tests is normally not seen under actual conditions.

CHAPTER 9
USING THYRISTOR DIE FOR HYBRID ASSEMBLY

1

Substantial savings in weight and volume can be achieved by hybrid packaging techniques. Most Motorola thyristor packaged devices are in die form for custom hybrid assembly. The same advanced thyristor processing techniques available in packaged form is available in die form.

DIE CHARACTERISTICS

Currently 12 die sizes are available. Seven in the low current range (< 8 amps) and 5 in the medium current range (> 8 amps). Table 9.I lists all low current devices and their die sizes while Table 9.II lists all medium current devices (for die layout and bond pad dimensions consult the factory).

Table 9.I. Low Current (< 8 Amps)

Die Metallization: Al (front), Au (back)

Part Number	*Die Size (Mil^2)
2C5060 thru 5064	32
MCRC100-4 thru -8	42
MCRC22-2 thru -8	48
2C1595 thru 2C1599	70
MCR106-2 thru -8	70
CC106F thru M	48
MAC97-4 thru -8	42
2C6071 thru 6075	84
2C4870 thru 2C4871	15 x 20
2C2646 thru 2C2647	15 x 20
2C6027 thru 2C6028	20
1C5758 thru 5761A	20
MBSC4991 thru 4992	20
2C6116 thru 6118	20

*All Thyristor Die are square unless indicated.

Table 9.II. Medium Current (> 8 Amps)

Die metallization: Solderable TiNiAg (Front and Back)

Part Number	*Die Size (Mil^2)
MCRC218-2 thru -10	92
CC122F1 thru N1	92
MCRC72-2 thru -8	92
MCRC67-2 thru -6	92
2C6394 thru 6399	92
MCRC68-2 thru -6	92
2C6400 thru 6405	150
MCR69-2 thru -6	150
2C682 thru 692	150
CC230F thru 230M	150
MCRC70-2 thru 70-6	150
MCRC264-2 thru -10	180
CC228A thru CC228M	150
MCRC265-2 thru -10	210
TC2500B thru N	120
MACC218A4 thru A10	120
2C6342 thru 6349	120
MACC228A4 thru A10	120
2C6342A thru 6349A	150
MACC15A4 thru A10	150
MACC223A4 thru A10	180
TC6421B thru N	210
MACC224A4 thru A10	210

*All Thyristor Die are square unless indicated.

ELECTRICAL CHARACTERISTICS

All die are individually probed at room temperature. However due to limitations when probing in wafer form some of the specifications of the equivalent packaged device cannot be tested and guaranteed in wafer form. These parameters include $R_{\theta JC}$, V_{TM} at high current, and switching times. The above parameters depend upon the

assembly techniques of the individual user. Each die is 100% tested by state-of-the-art computer test equipment and visually inspected per MIL-STD 19500 and MIL-STD 750 prior to shipment. Electrical specifications for most devices listed in Tables 9.I and 9.II can be found by consulting the corresponding data sheet for the packaged part.

Example:	MCRC218-2 thru 10	See MCR218 Data Sheet
	2C5060	See 2N5060 Data Sheet
	CC228A thru M	See C228 Data Sheet

1

VISUAL INSPECTION OF THYRISTOR DIE

All Motorola thyristor die meet the visual inspection criteria of MIL-Standard 750B, Method 2073, with the exception of specific criteria listed below. All thyristor dice are visually screened to a 1% AQL level.

DIE BACKING

All standard thyristor die come with the following metallization: low current (< 8 amps) — aluminum front metal and gold back metal, and medium current (> 8 amps) solderable titanium nickel silver on both front and back metal. This metallization is suitable for solder preform mounting. Commonly used header materials such as copper, nickel plated copper, gold plated molybdenum, beryllia, and alumina are acceptable. The substrate must be free of all oxides prior to assembly. Mounting is generally accomplished in a profiled belt furnace (hydrogen atmosphere is recommended).

WIRE BONDING AND CLIP ATTACHMENT

Electrical connection for low current thyristors can be accomplished by ultrasonic wire bonding, using AlMg* wire having an elongation of 10%. Caution should be exercised during wire bonding that the bond footprint remains within the bonding pad area. Wire bond settings should be optimized and a wire pull test performed (see Method 2037, MIL-STD 750B) to monitor wire bond strength uniformity. Destructive sample testing and 100% non-destructive testing is recommended. Electrical connection for medium current thyristors can be accomplished through the solder clip method as the pad metallization is a solderable TiNiAg. Assembly techniques such as a profiled belt furnace (hydrogen atmosphere) is recommended for attachment of the clips. Clips are recommended in order to withstand the high surge currents.

*Wire sizes of 15 mils and greater are pure Al.

ENCAPSULATION

Before encapsulation, the assembly must be kept in a moisture-free environment. For a non-hermetic package, a high grade electronic coating such as Dow Corning RTV3140 should be applied (coating is optional with hermetic package). Before encapsulation, a 150°C two-hour bake should be performed to remove any surface moisture, and any capping of hermetic packages must be performed in a dry nitrogen atmosphere.

HANDLING AND SHIPPING

Thyristor die are packaged several ways.

MULTI-PAK

This is a 2″ x 2″ or a 4″ x 4″ waffle type carrier with a separate carrier for each die, holding 100 to 400 die depending upon die size. The multi-pak is shown in Figure 9.1.

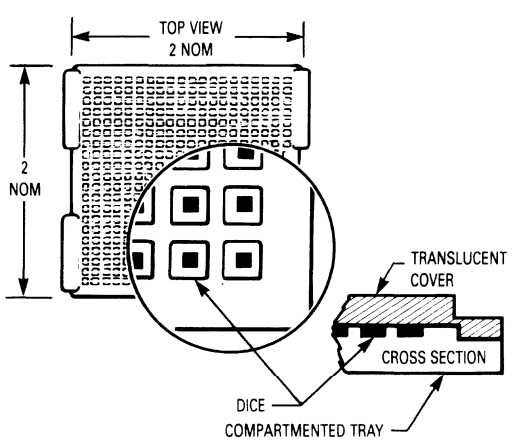


Figure 9.1. Multi-Pak

CIRCLE PAK

The wafer is placed on a sticky film before being sawed and broken. Each wafer is completely sawed through with one side backed against the PVC film. The die adhere to the PVC film and maintain their exact orientation and spacing. This packaging method also offers the convenience and storage with original orientation and spacing even after a portion of the wafer is used. The evacuated plastic bag is thermally sealed, holds the contents securely, and allows no die movement. Die can be removed from the sticky film by a sharp ejector pin pushing a die up and a vacuum needle manually picking it up. The circle-pak can also be handled by an automatic die loader with minor adjustment. The circle pak is shown in Figure 9.2.

Circle pak packaging method is patented by Motorola Inc.

WAFER PAK

The die are 100% electrically tested (rejects are inked) but the wafer is left unsawed. No visual inspection is performed.

VACUUM PAK

The die are 100% electrically tested (rejects are inked). A wafer or a quarter wafer is scribed and broken with the wafer left on the mylar. This is then sealed in a vacuum bag. No visual inspection is performed.

Upon opening the packaging medium, dice should be stored in a nitrogen atmosphere to prevent oxidation of bond areas prior to assembly. All dice should be handled with teflon tipped probes to prevent any mechanical damage.

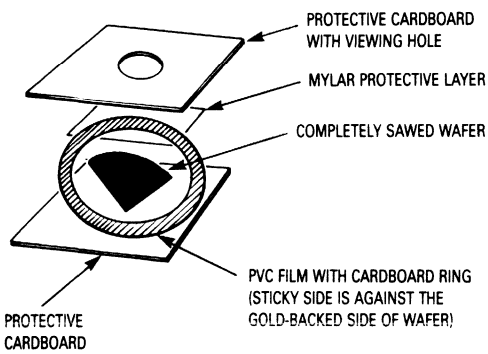


Figure 9.2. Circle Pak (CP Suffix)

APPENDICES

APPENDIX I

USING THE TWO TRANSISTOR ANALYSIS

DEFINITIONS:

I_C ≡ Collector current
I_B ≡ Base current
I_{CS} ≡ Collector leakage current (saturation component)
I_A ≡ Anode current
I_K ≡ Cathode current
α ≡ Current amplification factor
I_G ≡ Gate current

The subscript "i" indicates the appropriate transistor.

FOR TRANSISTOR #1:

$I_{C1} = \alpha_1 I_A + I_{CSI}$

and

$I_{B1} = I_A - I_{C1}$

Combining these equations,

$$I_{B1} = (1 - \alpha_1) I_A - I_{CS1} \qquad (1)$$

LIKEWISE, FOR TRANSISTOR #2

$$I_{C2} = \alpha_2 I_K + I_{CS2} \qquad (2)$$

$I_{B1} = I_{C2}$

and by combining Equations (1) and (2) and substituting $I_K = I_A + I_G$, it is found that

$$I_A = \frac{\alpha_2 I_G + I_{CS1} + I_{CS2}}{1 - \alpha_1 - \alpha_2} \qquad (3)$$

Equation (3) relates I_A to I_G, and note that as $\alpha_1 + \alpha_2 = 1$, I_A goes to infinity. I_A can be put in terms of I_K and α's as follows:

$I_{B1} = I_{C2}$

Combining equations (1) and (2):

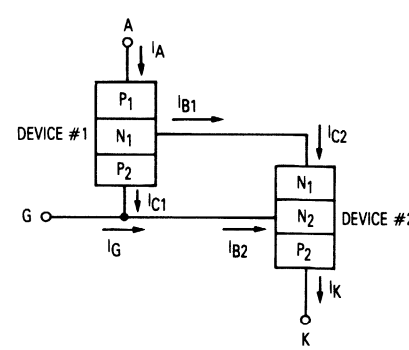
$$I_A = \frac{I_{CS1} + I_{CS2}}{1 - \alpha_1 - (\frac{I_K}{I_A})\alpha_2}$$

I_A — ∞ if denominator approaches zero, i.e., if

$$\frac{I_K}{I_A} = \frac{1 - \alpha_1}{\alpha_2}$$

Note that just prior to turn-on there is a majority carrier build-up in the P_2 "base." If the gate bias is small there will actually be hole current flowing out from P_2 into the gate circuit so that I_G is negative, $I_K = I_A + I_G$ is less than I_A so: (see Figure 3.2 for the directions of current components)

$\frac{I_K}{I_A} < 1$ which corresponds to $\alpha_1 + \alpha_2 > 1$



Schematic Diagram of the Two Transistor Model of a Thyristor

APPENDIX II

CHARGE AND PULSE WIDTH

1

In the region of large pulse widths using current triggering, where transit time effects are not a factor, we can consider the input gate charge for triggering, Q_{in}, as consisting of three components:

1) Triggering charge Q_{tr}, assumed to be constant.
2) Charge lost in recombination, Q_r, during current regeneration prior to turn-on.
3) Charge drained, Q_{dr}, which is by-passed through the built-in gate cathode shunt resistance (the presence of this shunting resistance is required to increase the dv/dt capability of the device).

Mathematically, we have

$$Q_{in} = Q_{tr} + Q_{dr} + Q_r = I_G\tau \qquad (1)$$

Q_r is assumed to be proportional to Q_{in}; to be exact,

$$Q_r = Q_{in}(1 - \exp -\tau/\tau_1) \qquad (2)$$

where I_G = gate current,

τ = pulse width of gate current,

τ_1 = effective life time of minority carriers in the bases

The voltage across the gate to cathode P-N junction during forward bias is given by V_{GK} (usually 0.6 V for silicon).* The gate shunt resistance is R_s (for the MCR729, typically 100 ohms), so the drained charge can be expressed by

$$Q_{dr} = \frac{V_{GC}}{R_s}\tau \qquad (3)$$

Combining equations (1), (2), and (3), we get

$$Q_{in} = I_G\tau = (Q_{tr} + \frac{V_{GC}}{R_s}\tau) \exp. \tau/\tau_1 \qquad (4)$$

Note that at region A and C of Figure 3.4(b) Q_{in} has an increasing trend with pulse width as qualitatively described by Equation (4).

Assume life time at the temperature range of operation increases as some power of temperature

$$\tau_1 = KT^m \qquad (5)$$

where K and m are positive real numbers. Combining Equations (4) and (5), we can get the slope of Q_{in} with respect to temperature to be

$$\text{slope} = \frac{dQ_{in}}{dT} = -m(Q_{tr} + \frac{V_{GC}}{R_s}\tau)\frac{\tau}{\tau_1}\frac{\exp. \tau/\tau_1}{T} \qquad (6)$$

In reality, Q_{tr} is not independent of temperature, in which case the Equation (6) must be modified by adding an additional term to become:

$$\text{slope} = -m(Q_{tr} + \frac{V_{GC}}{R_s}\tau)\frac{\tau}{\tau_1}\frac{\exp.\tau/\tau_1}{T} + \frac{dQ_{tr}}{dT}\exp\tau/\tau_1 \qquad (7)$$

Physically, not only does Q_{tr} decrease with temperature so that dQ_{tr}/dT is a negative number, but also $|dQ_{tr}/dT|$ decreases with temperature as does $|d\alpha/dT|$ in the temperature range of interest.

Equation (6) [or (7)] indicates two things:

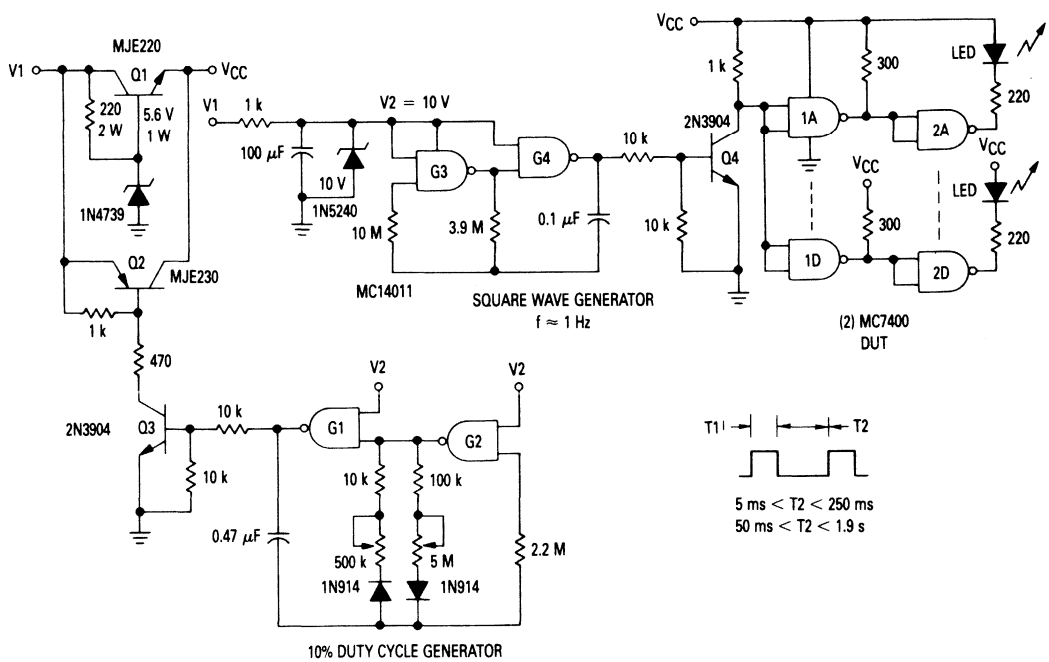
1) The rate of change of input trigger charge decreases as temperature (life time) increases.
2) The larger the pulse width of gate trigger current, the faster the rate of change of Q_{in} with respect to change in temperature. Figure 3.11 shows these trends.

*V_{GC} is not independent of I_G. For example, for the MCR729 the saturation V_{GC} is typically 1 V, but at lower I_G's the V_{GC} is also smaller, e.g. for I_G = 5 mA, V_{GC} is typically 0.3 V.

APPENDIX III

TTL SOA TEST CIRCUIT

Using the illustrated test circuit, the two TTL packages (quad, 2-input NAND gates) to be tested were powered by the simple, series regulator that is periodically shorted by the clamp transistor, Q2, at 10% duty cycle rate. By varying the input to the regulator V1 and the clamp pulse width, various power levels can be supplied to the TTL load. Thus, as an example, V_{CC} could be at 5 V for 90 ms and 10 V for 10 ms, simulating a transient on the bus or a possibly shorted power supply pass transistor for that duration. These energy levels are progressively increased until the gate (or gates) fail, as detected by the status of the output LEDs, the voltage and current waveforms and the device case temperature.



TTL SOA Test Circuit

APPENDIX IV

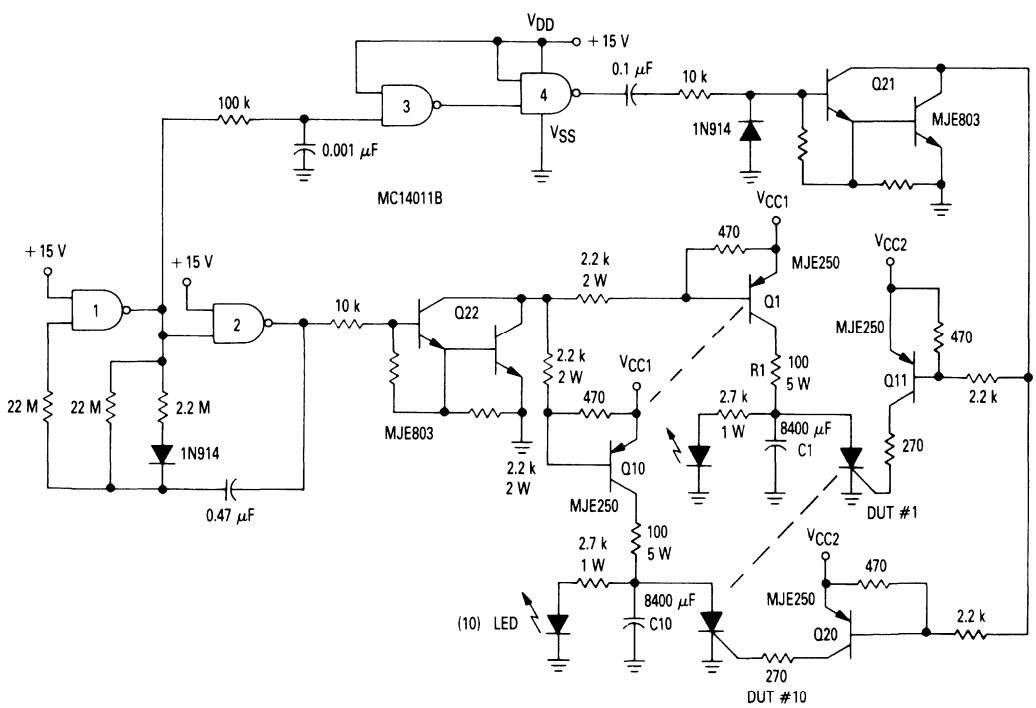
SCR CROWBAR LIFE TESTING

This crowbar life test fixture can simultaneously test ten SCRs under various crowbar energy and gate drive conditions and works as follows.

The CMOS Astable M.V. (Gates 1 and 2) generate an asymmetric Gate 2 output of about ten seconds high, one second low. This pulse is amplified by Darlington Q22 to turn on the capacitor charging transistors Q1–Q10 for the ten seconds. The capacitors for crowbarring are thus charged in about four seconds to whatever power supply voltage to which V_{CC1} is set. The charging transistors are then turned off for one second and the SCRs are fired by an approximately 100 μs delayed trigger derived from Gates 3 and 4. The R-C network on Gate 3 input integrates the complementary pulse from Gate 1, resulting in the delay, thus insuring non-coincident firing of the test circuit. The shaped pulse out of Gate 4 is differentiated and the positive-going pulse is amplified by Q21 and the following ten SCR gate drivers (Q11–Q20) to form the approximate 2 ms wide, 1 μs rise time, SCR gate triggers, I_{GT}. I_{GT} is set by the collector resistors of the respective gate drivers and the supply voltage, V_{CC2}; thus, for $I_{GT} \approx 100$ mA, $V_{CC2} \approx 30$ V, etc.

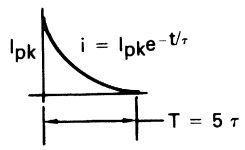
The LEDs across the storage capacitors show the state of the voltage on the capacitors and help determine whether the circuit is functioning properly. The timing sequence would be an off LED for the one-second capacitor dump period followed by an increasingly brighter LED during the capacitor charge time. Monitoring the current of V_{CC1} will also indicate proper operation.

The fixture's maximum energy limits are set by the working voltage of the capacitors and breakdown voltage of the transistors. For this illustration, the 60 V, 8400 μF capacitors (ESR $\approx$ 20 mΩ) produced a peak current of about 2500 A lasting for about 0.5 ms when V_{CC1} equals 60 V. Other energy values (lower i_{pk}, greater t_w) can be obtained by placing a current limiting resistor between the positive side of the capacitor and the crowbar SCR anode.



APPENDIX V

DERIVATION OF THE RMS CURRENT OF AN EXPONENTIALLY DECAYING CURRENT WAVEFORM



$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i^2(t)dt}$$

$$= \left[\frac{1}{T}\int_0^T (I_{pk}e^{-t/\tau})^2 dt\right]^{1/2}$$

$$= \left[\frac{I_{pk}^2}{T}\left.\frac{e^{-2t/\tau}}{(-2/\tau)}\right|_0^T\right]^{1/2}$$

$$= \left[\frac{I_{pk}^2}{T}\left(\frac{-\tau}{2}\right)(e^{-2T/\tau} - e^0)\right]^{1/2}$$

where $T = 5\,\tau$,

$$= \left[-\frac{I_{pk}^2}{10}(e^{-10} - 1)\right]^{1/2}$$

$$I_{rms} = \frac{I_{pk}}{\sqrt{10}} = 0.316\, I_{pk}$$

APPENDIX VI

DERIVATION OF I^2t FOR VARIOUS TIMES

Thermal Equation $\Delta t = Z(\theta)P_D$

where $Z(\theta) = r(t)R_{\theta JC}$

and $r(t) = K\sqrt{t}$

Therefore, for the same Δt,

$$\Delta t = K\sqrt{t_1}\, R_{\theta JC}P_{D_1} = K\sqrt{t_2}\, R_{\theta JC}P_{D_2},$$

$$\frac{P_{D_1}}{P_{D_2}} = \sqrt{\frac{t_2}{t_1}} = \frac{I_1^2R}{I_2^2R},$$

$$\frac{I_1^2}{I_2^2} = \sqrt{\frac{t_2}{t_1}}$$

Multiplying both sides by (t_1/t_2),

$$\frac{I_1^2t_1}{I_2^2t_2} = \left(\frac{t_2}{t_1}\right)^{1/2}\frac{t_1}{t_2} = \left(\frac{t_1}{t_2}\right)^{1/2}$$

$$I_1^2t_1 = I_2^2t_2\sqrt{\frac{t_1}{t_2}}$$

1

APPENDIX VII

THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D),
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation (1), thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that ΔT could be thought of as a voltage; thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor (indicated by Figure A3).

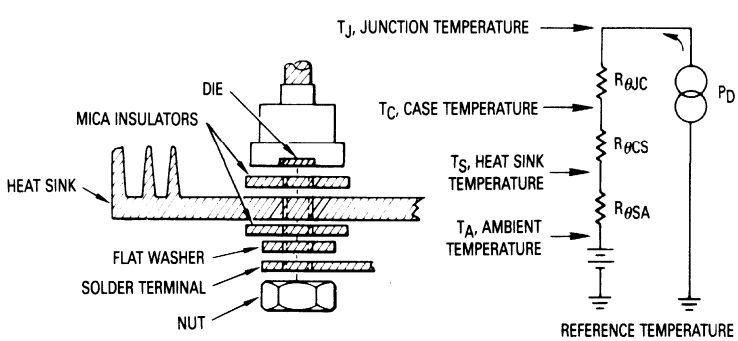
The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
P_D = power dissipation,
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat sink),
$R_{\theta SA}$ = heat sink thermal resistance (heat sink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result. The value for the interface thermal resistance, $R_{\theta CS}$, is affected by the mounting procedure and may be significant compared to the other thermal-resistance terms.

The thermal resistance of the heat sink is not constant; it decreases as ambient temperature increases and is affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. In some applications such as in RF power amplifiers and short-pulse applications, the concept may be invalid because of localized heating in the semiconductor chip.



Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX VIII

SOURCES OF ACCESSORIES

Manufacturer	Joint Compound	Insulators						Heat Sinks					
		BeO	Al_2O_3	Anodize	Mica	Plastic Film	Silicone Rubber	Stud	Flange	Disc	Thermowatt	Uni/Duo Watt	RF Stripline
Aavid Eng.	Ther-o-link 1000	—	—	—	—	—	—	X	X	—	X	—	—
AHAM	—	—	—	—	—	—	—	X	X	—	X	—	—
Astrodyne	#829	—	—	—	—	—	—	X	X	X	X	X	—
Delbert Blinn	—	X	—	X	X	X	X	X	X	—	—	—	—
IERC	Thermate	—	—	—	—	—	—	X	X	—	X	X	X
Staver	—	—	—	—	—	—	—	X	X	—	X	X	X
Thermalloy	Thermacote	X	X	X	—	X	—	X	X	X	X	X	X
Tor	TJC	X	—	X	X	X	—	X	X	—	X	—	—
Tran-tec	XL500	X	—	—	—	X	X	X	X	X	X	X	X
Wakefield Eng.	Type 120	X	—	X	—	—	—	X	X	X	X	X	—
Wei Corp.	—	—	—	—	—	—	—	X	X	—	—	—	—

Other sources for Joint Compounds: Dow Corning, Type 340
Emerson & Cuming, Eccoshield — SO (Electrically Conducting)
Emerson & Cuming, Eccotherm — TC-4 (Electrically Insulating)

SUPPLIERS' ADDRESSES

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM Heat Sinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astrodyne, Inc., 353 Middlesex Avenue, Wilmington, Massachusetts 01887 (617) 272-3850

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91766 (714) 623-1257

Dow Corning, Savage Road Building, Midland, Michigan 48640 (517) 636-8000

Eaton Corporation, Engineered Fasteners Division, Tinnerman Plant, P.O. Box 6688, Cleveland, Ohio 44101 (216) 523-5327

Emerson & Cuming, Inc., Dielectric Materials Division, 869 Washington Street, Canton, Massachusetts 02021 (617) 828-3300

International Electronics Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481

The Staver Company, Inc., 41-51 North Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tor Corporation, 14715 Arminta Street, Van Nuys, California 91402 (213) 786-6524

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

Wei Corporation, 1405 South Village Way, Santa Ana, California 92705 (614) 834-9333

APPENDIX IX

DERIVATION OF RFI DESIGN EQUATIONS

The relationship of flux to voltage and time is $E = N\frac{d\phi}{dt}$ or $E = NA_c\frac{dB}{dt}$ since $\phi = BA_c$ and A_c is a constant. Rearranging this equation and integrating we get:

$$\int E\,dt = NA_c\,(B_2 - B_1) = NA_c\,\Delta B \qquad (1)$$

which says that the volt-second integral required determines the size of the core. In an L-R circuit such as we have with a thyristor control circuit, the volt-second characteristic is the area under an exponential decay. A conservative estimate of the area under the curve may be obtained by considering a triangle whose height is the peak line voltage and the base is the allowable switching time. The area is then 1/2 bh or $\frac{E_p t_r}{2}$. Substituting in Equation (1):

$$\frac{E_p t_r}{2} = N\,A_c\,\Delta B \qquad (2)$$

where:

E_p is the peak line voltage

t_r is the allowable current rise time

N is the number of turns on the coil

A_c is the usable core area in cm^2

ΔB is the maximum usable flux density of the core material in W/m^2

Rewriting Equation (2) to change ΔB from W/m^2 to gauss, substituting $\sqrt{2}\,E_{rms}$ for E_p and solving for N, we get:

$$N = \frac{\sqrt{2}\,E_{rms}\,t_r}{2\,A_c\,\Delta B} \times 10^8 = \frac{0.707\,E_{rms}\,t_r \times 10^8}{B_{MAX}\,A_c}$$

A_c in this equation is in cm^2. To change to in^2, multiply A_c by 6.452. Then:

$$N = \frac{10.93\,E_{rms}\,t_r \times 10^6}{B_{MAX} \times A_c} \qquad (3)$$

where:

N is total turns

E_{rms} is line voltage

t_r is allowable current rise time in seconds

B_{MAX} is maximum usable flux density of core material

A_c is usable core area in square inches

Window area necessary is:

$$A_w = N\,A_{wire} \times 3 \qquad (4)$$

The factor of 3 is an approximation which allows for insulation and winding space not occupied by wire. Substituting equation (3) in (4):

$$A_w = \frac{10.93\,E_{rms}\,t_r \times 10^6}{B_{MAX}\,A_c}\,A_{wire} \times 3$$

(The factor 10.93 may be rounded to 11 since two significant digits are all that are necessary.)

The factor A_cA_w can easily be found for most cores and is an easy method for selecting a core.

$$A_cA_w = \frac{33\,E_{rms}\,t_r A_{wire} \times 10^6}{B_{MAX}}$$

In this equation, the core area is in in^2. To work with circular mils, multiply by 0.78×10^{-6} so that:

$$A_cA_w = \frac{26\,E_{rms}\,t_r A_{wire}}{B_{MAX}}$$

where A_{wire} is the wire area in circular mils.

Inductance of an iron core inductor is

$$L = \frac{3.19\,N^2\,A_c\,10^{-8}}{lg + \frac{l_c}{\mu}}$$

Rearranging terms,

$$lg = \frac{3.19\,N^2\,A_c\,10^{-8}}{L} - \frac{l_c}{\mu}$$

APPENDIX X

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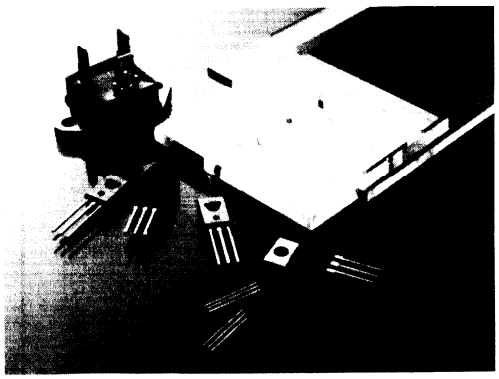


Motorola's broad line of Thyristors include. . . .

- A full line of TRIACs and SCRs covering a forward current range from 0.5 to 55 amperes and blocking voltages from 15 to 800 volts.
- Two basic package categories — plastic for lowest cost — including fully insulated plastic Case 221C-02 (TO-220 Full Pak); metal for hemetically-sealed requirements in high-reliability projects.
- An extensive line of trigger devices that includes UJTs, PUTs, SBS — even optically-coupled TRIAC drivers from Motorola's optoelectronic product line.

Then there are the special applications devices — for Radar Modulation and Crowbar applications; even specially packaged devices with quick-disconnect terminals for appliances and SOT packages for surface mounting in space-saving requirements.

Finally, there is the continued Motorola investment in discrete-product R & D, producing new capabilities such as "gate-turnoff" (GTO) devices which facilitates the use of thyristors in dc power-switching applications.

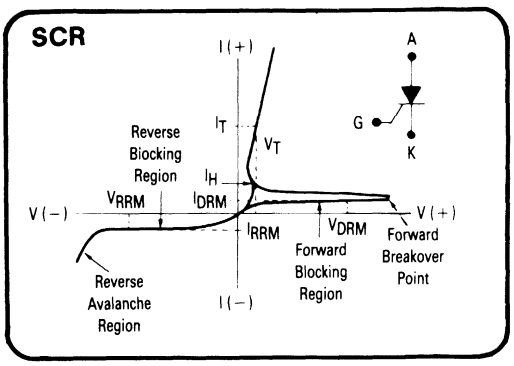
Selector Guide

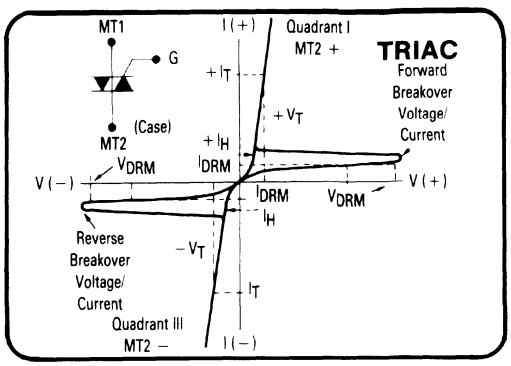
2

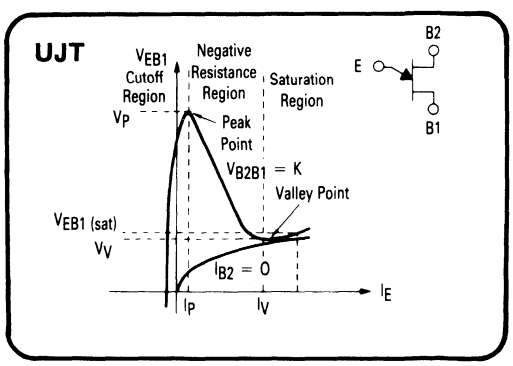
Contents **Page**

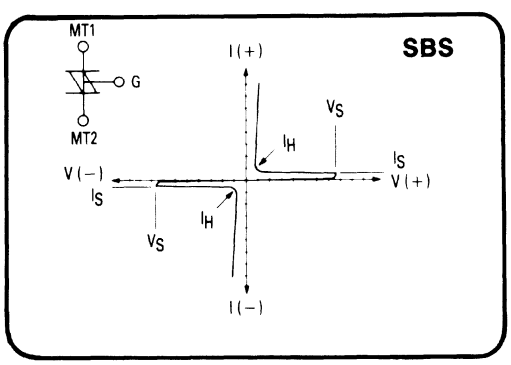
Numeric Index 2-3
GTOs (Gate Turn-Off). 2-4
Isolated TRIAC Mold Type 2-4
SCRs
General Purpose. 2-4
Radar Modulator 2-15
TRIACs
General Purpose. 2-16
Optically Isolated. 2-27
Triggers
UJT — Unijunction Trnasistors. 2-28
SIDACs 2-28
PUT — Programmable Unijunctions 2-28
SBS — Silicon Bidirectional Switch 2-28

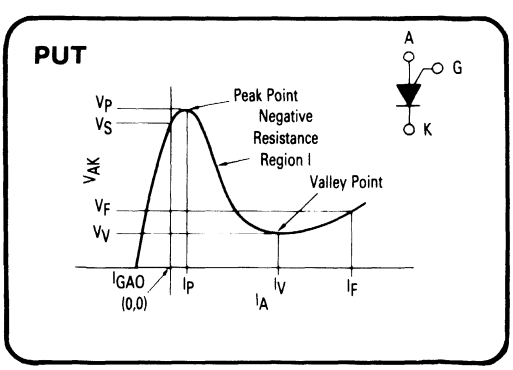
Characteristic Curves

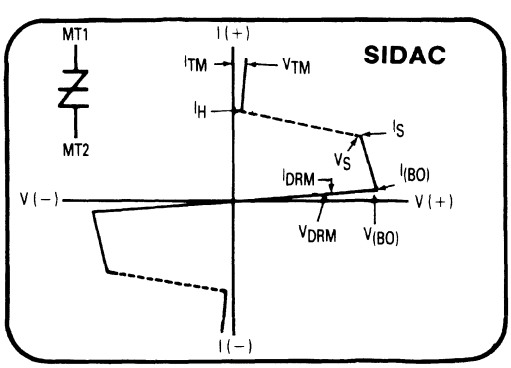












2

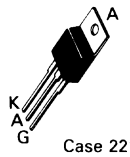
Numeric Index

Device	Page
2N Devices	
2N1595-99	2-5
2N2323-29	2-6
2N2646-47	2-19
2N3980	2-19
2N4199-4204	2-10
2N4851-53	2-19
2N4870-71	2-19
2N5060-64	2-5
2N5444-46	2-17
2N6027-28	2-19
2N6071-6075B	2-11
2N6237-41	2-6
2N6342-49	2-13
2N6342A-49A	2-15
2N6394-405	2-8
2N6400-05	2-8
2N6504-09	2-8
"B" Devices (SCRs)	
BRX44 Series	2-5
BRY55 Series	2-5
"C" Devices (SCRs)	
C106 Series	2-6
C122 Series	2-7
C205 Series	2-5
MAC Devices (TRIACs)	
MAC15A Series	2-15
MAC15AFP Series	2-16
MAC97,A,B Series	2-16
MAC210A Series	2-14
MAC210AFP Series	2-14
MAC212A Series	2-15
MAC212AFP Series	2-14
MAC218A Series	2-12
MAC218AFP Series	2-12
MAC223A Series	2-16
MAC223AFP Series	2-16
MAC224A Series	2-17
MAC228A Series	2-13
MAC229A Series	2-13
MAC310A Series	2-14
MAC320A Series	2-16
MAC320AFP Series	2-16
MAC625 Series	2-17
MAC635 Series	2-17
MAC3010 Series	2-18
MAC3020 Series	2-18
MAC3030 Series	2-18
MAC3040 Series	2-18
MAC3060 Series	2-18
MBS Devices (Bilateral Switches)	
MBS4991-92	2-19
MCR Devices (SCRs)	
MCR22 Series	2-5
MCR68 Series	2-8
MCR69 Series	2-8
MCR72 Series	2-7
MCR100 Series	2-5
MCR102-3	2-5
MCR106 Series	2-6
MCR218 Series	2-7
MCR218FP Series	2-7
MCR225FP Series	2-9
MCR264 Series	2-9
MCR265 Series	2-9
MCR310 Series	2-7
MCR506 Series	2-6
MCR729 Series	2-10
MPU Devices (PUTs)	
MMBP6027/6028	2-3
GTO Devices (MGTO)	
MGTO1000,1200	2-4
"S" Devices (SCRs)	
S2800 Series	2-7
"SC" Devices (TRIACs)	
SC141 Series	2-12
"T" Devices (TRIACs)	
T2500 Series	2-12
T2500FP Series	2-12
"MK" Devices (SIDACs)	
MK1V Series	2-19
MKP9V Series	2-19

2

GTOs

Gate Turn-Off Thyristors



Case 221A-04

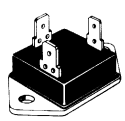
GTOs are thyristors that can be turned off as well as on by a gate signal. They are rugged, efficient high voltage switches that are particularly well suited for pulse width modulation circuits and in applications such as motor drives, switching power supplies, inverters and other functions requiring high surge-current capabilities and fast switching speeds.

Specification Max	Device Number	
	MGTO1000	MGTO1200
VDRXM (V)	1000	1200
I_{TSM} (A)	200	
I_{GTM} (mA)	300	
V_{GTM} (V)	1.5	
I_H (mA)	400	
V_{GRM} (V)	15	

2

ATTENTION: PACKAGE INNOVATION

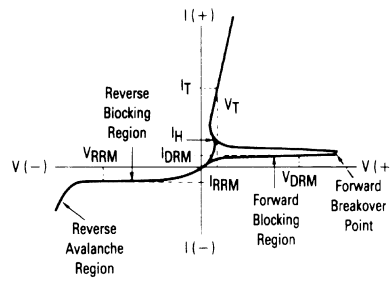
Isolated TRIAC Mold Type



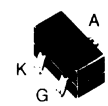
Features a TO-3 isolated mounting with a high isolation voltage of 2.5 kVrms min. This package also offers quick disconnect lead attachments, is plastic encapsulated to provide economical cost and is UL recognized. See pages 2-26 and 2-27 for the MAC625 and MAC635 series.

SCRs

Silicon Controlled Rectifiers



On-State
0.8 A
T_C = 67°C

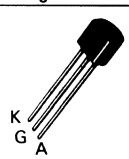


		Sensitive Gate
		Case 318-02 SOT-23
V_{DRM}	25 V	MMBS5060
	50 V	MMBS5061
	100 V	MMBS5062
	200 V	
V_{RRM}	400 V	
	500 V	
	600 V	
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps) 60 Hz	
	I_{GT} (mA)	0.2
	V_{GT} (V)	0.8
	T_J Operating Range (°C)	−25 to +150

Thyristors — SCR's

Metal/Plastic Packages

0.5 to 55 Amperes RMS
25–1000 Volts

On-State (RMS) Current					
0.8 AMP	**1.2 AMPS**	**1.5 AMPS**	**1.6 AMPS**		
$T_C = 58°C$	$T_C = 25°C$	$T_C = 50°C$	$T_C = 80°C$		
					
Sensitive Gate					
Case 29-04 TO-226AA (TO-92) Style 10			**Case 79-04 TO-205AD (TO-39) Style 3**		
MCR102 2N5060 BRX44/BRY55-30*	C205Y			**25V**	V_{DRM}
MCR103 2N5061 BRX45/BRY55-60*	C205YY	MCR22-2	2N1595	**50V**	
MCR100-3 2N5062 BRX46/BRY55-100*	C205A	MCR22-3	2N1596	**100V**	
MCR100-4 2N5064 BRX47/BRY55-200*	C205B	MCR22-4	2N1597	**200V**	
MCR100-6 BRX49/BRY55-400*	C205D	MCR22-6	2N1599	**400V**	V_{RRM}
BRY55-500*				500V	
MCR100-8 BRY55-600*		MCR22-8		600V	
10		150[1]	15	**I_{TSM} (Amps) 60 Hz**	**MAXIMUM ELECTRICAL CHARACTERISTICS**
0.2			10	**I_{GT} (mA)**	
0.8			3	**V (V)**	
–65 to +100	–65 to +125°C	–40 to +125	–65 to +125	**T_J Operating Range (°C)**	

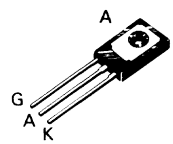
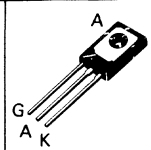
NOTE:
Industry Standards, with a variety of Custom Specifications and Leadforms available on Case 29-04 product.

[1] Exponential decay for 1 µs, 10 Hz pulse width (CD ignition)
* European Part Numbers. Package is Case 29 with Leadform 18. Case is Style 3.

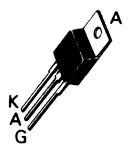
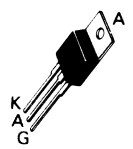
2

SCR's (continued)

2

		On-State (RMS) Current			
		1.6 AMPS	4 AMPS		6 AMPS
		$T_C = 85°C$	$T_C = 93°C$	$T_C = 30°C$	$T_C = 30°C$
					 Sensitive Gate
		Case 79-04 TO-205AD (TO-39) Style 3	Case 77-05 TO-126 Style 2		Case 77-05 TO-126 Style 2
V_{DRM}	50 V	2N2323	MCR106-2 2N6237	C106F	MCR506-2
V_{DRM}	100 V	2N2324	MCR106-3 2N6238	C106A	MCR506-3
V_{DRM}	200 V	2N2326	MCR106-4 2N6239	C106B	MCR506-4
V_{RRM}	400 V	2N2329	MCR106-6 2N6240	C106D	MCR506-6
V_{RRM}	600V		MCR106-8 2N6241	C106M	MCR506-8
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps) 60 Hz	15	25	20 150[1]	40
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{GT} (mA)	0.2	0.2		0.2
MAXIMUM ELECTRICAL CHARACTERISTICS	V_{GT} (V)	0.8	1	0.8	1
MAXIMUM ELECTRICAL CHARACTERISTICS	T_J Operating Range (°C)	−65 to +125	−40 to +110		−40 to +110

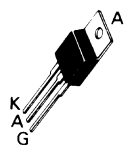
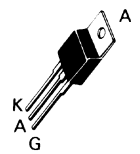
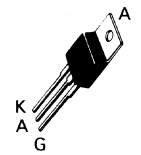
[1] Exponential decay for 1 µs, 10 Hz pulse width (CD ignition)

On-State (RMS) Current						
8 AMPS				10 AMPS		
T_C = 70°C	T_C = 75°C		T_C = 83°C	T_C = 75°C		
						
			Sensitive Gate	Sensitive Gate		
Case 221C-02 Style	Case 221A-04 TO-220AB Style 3			Case 221A-04 TO-220AB Style 3		
MCR218-2FP	MCR218-2	C122F S2800F	MCR72-2	MCR310-2	50 V	V_{DRM}
	MCR218-3	C122A S2800A	MCR72-3	MCR310-3	100 V	
MCR218-4FP	MCR218-4	C122B S2800B	MCR72-4	MCR310-4	200 V	
MCR218-6FP	MCR218-6	C122D S2800D	MCR72-6	MCR310-6	400 V	
MCR218-8FP	MCR218-8	C122M S2800M	MCR72-8	MCR310-8	600 V	V_{RRM}
MCR218-10FP	MCR218-10	C122M S2800N			800 V	
80		C122/S2800 90/100	100	100	I_{TSM} (Amps) 60 Hz	MAXIMUM ELECTRICAL CHARACTERISTICS
30	25	C122/S2800 25/25	0.2	0.2	I_{GT} (mA)	
2.5	1.5				V_{GT} (V)	
−40 to +125		−40 to +100		−40 to +110	T_J Operating Range (°C)	

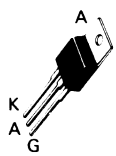
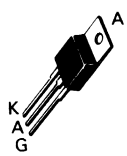
2

SCR's (continued)

2

		On-State (RMS) Current				
		12 AMPS		16 AMPS	25 AMPS	
		$T_C = 85°C$	$T_C = 90°C$	$T_C = 90°C$	$T_C = 85°C$	
						
		Case 221A-04 TO-220AB Style 3				
V_{DRM} / V_{RRM}	50 V	MCR68-2	2N6394	2N6400	2N6504	MCR69-2
	100 V	MCR68-3	2N6395	2N6401	2N6505	MCR69-3
	200 V		2N6396	2N6402	2N6506	
	400 V	MCR68-6	2N6397	2N6403	2N6507	MCR69-6
	600 V		2N6398	2N6404	2N6508	
	800 V		2N6399	2N6405	2N6509	
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps) 60 Hz	300(1)	100	160	300	750(1)
	I_{GT} (mA)	30		30	40	30
	V_{GT} (V)	1.5				
	T_J Operating Range (°C)	– 40 to +125				

(1) Peak capacitor discharge current for $t_w = 1$ µs. t_w is defined as five time constants of an exponentially decaying current pulse (crowbar applications).

On-State (RMS) Current				
25 AMPS	**40 AMPS**	**55 AMPS**		
T_C = 85°C	**T_C = 80°C**	**T_C = 70°C**		
				
Case 221C-02 Style 3	**Case 221A-04 TO-220AB Style 3**	**Cases 221A-04 TO-220AB Style 3**		
MCR225-2FP	MCR264-2	MCR265-2	**50 V**	**V_{DRM}**
	MCR264-3	MCR265-3	**100 V**	
MCR225-4FP	MCR264-4	MCR265-4	**200 V**	**V_{RRM}**
MCR225-6FP	MCR264-6	MCR265-6	**400 V**	
MCR225-8FP	MCR264-8	MCR265-8	**600 V**	
MCR225-10FP	MCR264-10	MCR265-10	**800 V**	
300	400	550	**I_{TSM} (Amps) 60 Hz**	**MAXIMUM ELECTRICAL CHARACTERISTICS**
40	50	50	**I_{GT} (mA)**	
1.5			**V_{GT} (V)**	
–40 to +125			**T_J Operating Range (°C)**	

(1) Peak capacitor discharge current for t_w = 1 µs. t_w is defined as five time constants of an exponentially decaying current pulse (crowbar applications).

2

Radar Modulators

		On State Pulsed Current 100 AMPS TC = 85°C	
		Case 63-03 TO-64 Style 1	
VDRM	300 V	2N4199 2N4199JAN	MCR729-5
	400 V	2N4200 2N4200JAN	MCR729-6
VRRM	500 V	2N4201 2N4201JAN	MCR729-7
	600 V	2N4202 2N4202JAN	MCR729-8
	700 V	2N4203 2N4203JAN	MCR729-9
	800 V	2N4204 2N4204JAN	MCR729-10

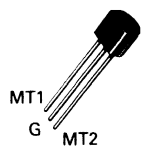
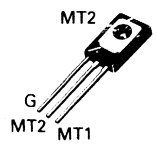
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps) 60 Hz	100*
	I_{GT} (mA)	50
	V_{GT} (V)	1.5
	T_J Operating Range (°C)	–65 to +105

* Indicates pulse rating P_W = 3 µs duty cycle = 0.60%.

Thyristors — TRIACs

Metal/Plastic Packages

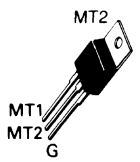
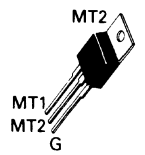
0.6 to 40 Amperes RMS
25–800 Volts

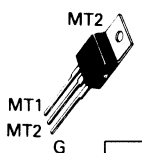
On-State (RMS) Current						
0.6 AMPS		4 AMPS				
T_C = 50°C		T_C = 85°C				
						
Sensitive Gate			Sensitive Gate			
Case 29-04 TO-226AA (TO-92) Style 12		Case 77-05 Style 5				
MAC97-4	MAC97A4	2N6071	2N6071A	2N6071B	**200 V**	**V_{DRM}**
MAC97-6	MAC97A6	2N6073	2N6073A	2N6073B	**400 V**	
MAC97-8	MAC97A8	2N6075	2N6075A	2N6075B	**600 V**	
8		30			**I_{TSM} (Amps)**	**MAXIMUM ELECTRICAL CHARACTERISTICS**
10 10 10 10	5 5 5 7	30 – 30 –	5 5 5 10	3 3 3 5	**I_{GT} @ 25°C (mA)** **MT2(+)G(+)** **MT2(+)G(–)** **MT2(–)G(–)** **MT2(–)G(+)**	
2 2 2 2.5		@ –40°C 2.5 – 2.5 –	@ –40°C 2.5 2.5 2.5 2.5		**I_{GT} @ 25°C (mA)** **MT2(+)G(+)** **MT2(+)G(–)** **MT2(–)G(–)** **MT2(–)G(+)**	
		–40 to +110			T_J Operating Range (°C)	

2

TRIACs (continued)

2

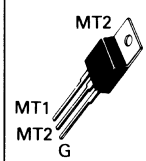
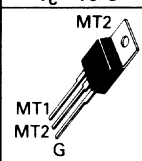
		On-State (RMS) Current				
		6 AMPS			8 AMPS	
		T_C = 80°C				
						
		Case 221A-04 TO-220AB Style 4	Case 221C-02 Style 3	Case 221A-04 TO-220AB Style 4		Case 221C-02 Style 3
V_{DRM}	200 V	T2500B	T2500BFP	SC141B	MAC218A4	MAC218A4FP
	400 V	T2500D	T2500DFP	SC141D	MAC218A6	MAC218A6FP
	600 V	T2500M	T2500MFP	SC141M	MAC218A8	MAC218A8FP
	800 V	T2500N	T2500BFP	SC141N	MAC218A10	MAC218A10FP
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	60	80		100	
	I_{GT} @ 25°C (mA)					
	MT2(+)G(+)	25	80	50	50	
	MT2(+)G(–)	60	80	50	50	
	MT2(–)G(–)	25	80	50	50	
	MT2(–)G(+)	60	80	–	80	
	V_{GT} @ 25°C (V)					
	MT2(+)G(+)	2.5	4	2.5	2	
	MT2(+)G(–)	2.5	4	2.5	2	
	MT2(–)G(–)	2.5	4	2.5	2	
	MT2(–)G(+)	2.5	4	–	2.5	
	TJ Operating Range (°C)	–40 to +110			–40 to +125	

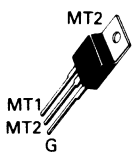
On-State (RMS) Current				
8 AMPS				
T_C = 80°C				
				
	Sensitive Gate			
Case 221A-04 TO-220AB Style 4				
2N6342 **2N6346**	MAC228A4	MAC229A4	**200 V**	V_{DRM}
2N6343 **2N6347**	MAC228A6	MAC229A6	**400 V**	
2N6344 **2N6348**	MAC228A8	MAC229A8	**600 V**	
2N6345 **2N6349**	MAC228A10	MAC229A10	**800 V**	
80			**I_{TSM} (Amps)**	MAXIMUM ELECTRICAL CHARACTERISTICS
50 75# 50 75#	5 5 5 10	10 10 10 20	**I_{GT} @ 25°C (mA)** **MT2(+)G(+)** **MT2(+)G(–)** **MT2(–)G(–)** **MT2(–)G(+)**	
2 2.5# 2.5 2.5#	2 2 2 2.5		**V_{GT} @ 25°C (V)** **MT2(+)G(+)** **MT2(+)G(–)** **MT2(–)G(–)** **MT2(–)G(+)**	
–40 to +125	–40 to +110		**TJ Operating Range (°C)**	

# Denotes 2N6346–49 series only.

TRIACs (continued)

2

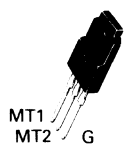
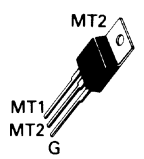
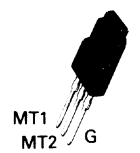
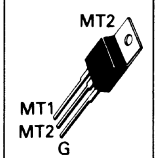
		On-State (RMS) Current			
		10 AMPS			12 AMPS
		T_C = 70°C	T_C = 70°C	T_C = 75°C	T_C = 85°C
				 Sensitive Gate	
		Case 221A-04 TO-220AB Style 4	Case 221C-02 Style 3	Case 221A-04 TO-220AB Style 4	Case 221C-02 Style 3
V_{DRM}	200 V	MAC210A4	MAC210A4FP	MAC310A4	MAC212A4FP
	400 V	MAC210A6	MAC210A6FP	MAC310A6	MAC212A6FP
	600 V	MAC210A8	MAC210A8FP	MAC310A8	MAC212A8FP
	800 V	MAC210A10	MAC210A10FP		MAC212A10FP
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	100			
	I_{GT} @ 25°C (mA)				
	MT2(+)G(+)	50	50	10	50
	MT2(+)G(–)	50	50	10	50
	MT2(–)G(–)	50	50	10	50
	MT2(–)G(+)	80	80	10	80
	V_{GT} @ 25°C (V)				
	MT2(+)G(+)	2	2	2.5	2
	MT2(+)G(–)	2	2	2.5	2
	MT2(–)G(–)	2	2	2.5	2
	MT2(–)G(+)	2.5	2.5	2.5	2.5
	TJ Operating Range (°C)	–40 to +125			

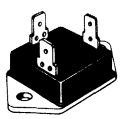
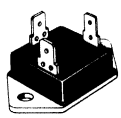
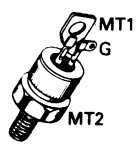
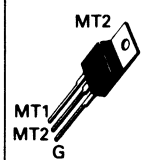
On-State (RMS) Current					
12 AMPS			15 AMPS		
T_C = 85°C	T_C = 80°C		T_C = 90°C		
					
Case 221A-04 TO-220AB Style 4					
MAC212A4	2N6342A	2N6346A	MAC15A4	200 V	V_{DRM}
MAC212A6	2N6343A	2N6347A	MAC15A6	400 V	
MAC212A8	2N6344A	2N6348A	MAC15A8	600 V	
MAC212A10	2N6345A	2N6349A	MAC15A10	800 V	
100	120		150	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
				I_{GT} @ 25°C (mA)	
50	50	50	50	MT2(+)G(+)	
50	–	75	50	MT2(+)G(–)	
50	50	50	50	MT2(–)G(–)	
80	–	75	80	MT2(–)G(+)	
				V_{GT} @ 25°C (V)	
2	2	2	2	MT2(+)G(+)	
2	–	2.5	2	MT2(+)G(–)	
2	2	2	2	MT2(–)G(–)	
2.5	–	2.5	2.5	MT2(–)G(+)	
–40 to +125				T_J Operating Range (°C)	

2

TRIACs (continued)

2

		On-State (RMS) Current				
		15 AMPS	20 AMPS			
		T_C = 90°C	T_C = 75°C		T_C = 80°C	
					
		Case 221C-02 Style 3		Case 221A-04 TO-220AB Style 4	Case 221C-02 Style 3	Case 221A-04 TO-220AB Style 4
V_{DRM}	200 V	MAC15A4FP	MAC320A4FP	MAC320A4	MAC223A4FP	MAC223A4
	400 V	MAC15A6FP	MAC320A6FP	MAC320A6	MAC223A6FP	MAC223A6
	600 V	MAC15A8FP	MAC320A8FP	MAC320A8	MAC223A8FP	MAC223A8
	800 V	MAC15A10FP	MAC320A10FP	MAC320A10	MAC223A10FP	MAC223A10
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	150			250	
	I_{GT} @ 25°C (mA) MT2(+)G(+) MT2(+)G(–) MT2(–)G(–) MT2(–)G(+)	 50 50 50 80			 50 50 50 80	
	V_{GT} @ 25°C (V) MT2(+)G(+) MT2(+)G(–) MT2(–)G(–) MT2(–)G(+)	 2 2 2 2.5			 2 2 2 2.5	
	TJ Operating Range (°C)	–40 to +125			–40 to +125	

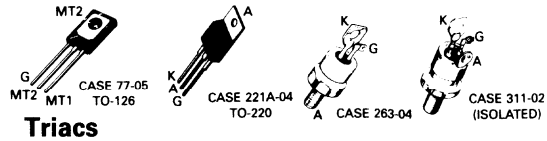
On-State (RMS) Current					
25 AMPS	35 AMPS	40 AMPS			
T_C = 75°C	T_C = 58°C	T_C = 65°C	T_C = 75°C		
					
Case 383-01 Style 1	Case 383-01 Style 1	Case 263-04 Style 2	Case 221A-04 TO-220AB Style 4		
		2N5444	MAC224A4	200 V	V_{DRM}
MAC625-4	MAC635-4	2N5445	MAC224A6	400 V	
MAC625-6	MAC635-6	2N5446	MAC224A8	600 V	
MAC625-8	MAC635-8		MAC224A10	800 V	
250	330	300	350	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
50	50	70	50	I_{GT} @ 25°C (mA) MT2(+)G(+)	
50	50	70	50	MT2(+)G(–)	
50	50	70	50	MT2(–)G(–)	
–	–	100	80	MT2(–)G(+)	
3	3	2	2	V_{GT} @ 25°C (V) MT2(+)G(+)	
3	3	2	2	MT2(+)G(–)	
3	3	2	2	MT2(–)G(–)	
–	–	2.5	2.5	MT2(–)G(+)	
–40 to +125	–40 to +125	–65 to +110	–40 to +125	TJ Operating Range (°C)	

2

TRIACs
Optically Isolated

Triac Driver/Triac Combinations

This series of Triac Drivers consists of infrared LEDs optically coupled to photodetectors with Triac output. 7500 V isolation between input and output allows safe, economical triggering of higher power triacs from logic sources with output as low as 3 volts, 10 mA. Associated voltage-compatible triacs provide matched pairs for a variety of voltage/current requirements.



Triac Drivers — all in Case 730A

Peak Blocking Voltage Volts	LED Trigger Current I_{FT} mA, Max	Device
250	30	MOC3009
	15	3010
	10	3011
400	30	3020
	15	3021
For Zero Crossover Firing		
250	30	MOC3030*
	15	3031*
400	30	3040
	15	3031
600	30	3060
	15	3061

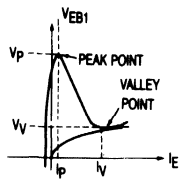
*Underwriters' Laboratories Recognition, File No. E54915.

Triacs

Output Current I_{RMS} A, Max	Peak Blocking Voltage Volts			Case
	250	400	600	
4	MAC3010-4	MAC3020-4	—	77-05
8	-8	-8	—	221A
15	-15	-15	—	221A
25	-25	-25	—	221A
40	-40	-40	—	263
40	-40I	-40I	—	311
For Zero Crossover Firing				
4	MAC3030-4	MAC3040-4	MAC3060-4	77-05
8	-8	-8	-8	221A
15	-15	-15	-15	221A
25	-25	-25	-25	221A
40	-40	-40	-40	263
40	-40I	-40I	-40I	311

Thyristor Triggers

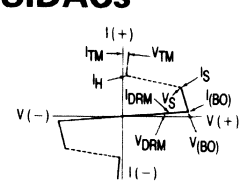
Unijunction Transistors — UJT



Highly stable devices for general-purpose trigger applications and as pulse generators (oscillators) and timing circuits. Useful at frequencies ranging (generally) from 1 Hz to 1 MHz.

Device Type	η Min	η Max	I_P µA Max	I_{EB20} µA Max	I_V mA Min
Plastic TO-92 (Case 29-04/9)					
2N4870	0.56	0.75	5	1	2
2N4871	0.7	0.85	5	1	4
Plastic TO-92 (Case 29-04/9)					
2N2646	0.56	0.75	5	12	4
2N2647	0.68	0.82	2	0.2	8
2N3980	0.68	0.82	2	0.01	1
2N4851	0.56	0.75	2	0.1	2
2N4852	0.7	0.85	2	0.1	4
2N4853	0.7	0.85	0.4	0.05	6

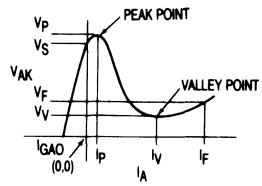
SIDACs



High voltage trigger devices similar in operation to a Triac. Upon reaching the breakover voltage in either direction, the device switches to a low-voltage on-state.

Device Type	I_{TSM} Amps	V_{BO} Volts Min	V_{BO} Volts Max
Case 267-03/1			
MK1V115	20	104	115
MK1V125	20	110	125
MK1V135	20	120	135
MK1V240	20	220	250
MK1V260	20	240	270
MK1V270	20	250	280
CASE 59-04/1			
MKP9V120	4	110	125
MKP9V130	4	120	135
MKP9V240	4	220	250
MKP9V260	4	240	270
MKP9V270	4	250	280

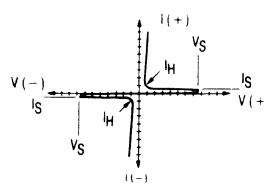
Programmable Unijunction Transistors — PUT



Similar to UJTs, except that I_V, I_P and intrinsice standoff voltage are programmable (adustable) by means of external voltage divider. This stabilizes circuit performance for variations in device paramaters. General operating frequency range is from 0.01 Hz to 10 kHz, making them suitable for long-duration timer circuits.

Device Type	I_P R_G = 10 kΩ	I_P R_G = 1MΩ	I_{GAO} @ 40 V nA Max	I_V R_G = 10 kΩ	I_V R_G = 1MΩ
	µA Max			µA Min	µA Max
Plastic TO-92 (Case 29-04/16)					
2N6027	5	2	10	70	50
2N6028	1	0.15	10	25	25
Surface Mount SOT-23 (Case 318-03/20)					
MMBP6027	5	2	10	70	50
MMBP6028	1	0.15	10	70	25

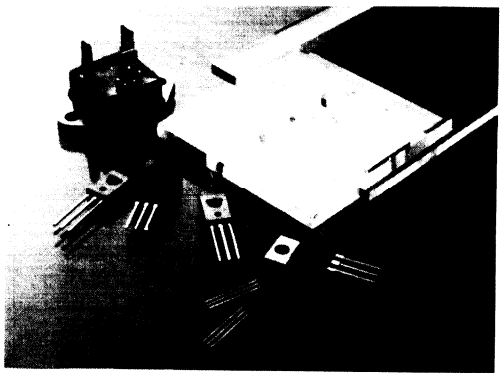
Silicon Bidirectional Switch (SBS)



This versatile trigger device exhibits highly symmetrical bidirectional switching characteristics which can be modified by means of a gate lead. Requires a gate trigger current of only 250 µA dc for triggering.

Device Type	V_S Volts Min	V_S Volts Max	I_S µA Max	I_H mA Max
Plastic TO-92/TO-226AA				
MBS4991	6	10	500	1.5
MBS4992	7.5	9	120	0.5
MBS4993	7.5	9	250	0.75

2



Data Sheets 3

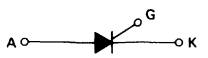
Silicon Controlled Rectifier
Reverse Blocking Triode Thyristors

2N682 thru 2N692

SCRs
25 AMPERES RMS
25 thru 800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Blocking Voltage to 800 Volts



CASE 263-04
STYLE 1

3

MAXIMUM RATINGS (T_J = 125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Blocking Voltage, Note 1	V_{RRM} or V_{DRM}		Volts
2N682		50	
2N683		100	
2N685		200	
2N688		400	
2N690		600	
2N692		800	
*Peak Non-Repetitive Reverse Voltage	V_{RSM}		Volts
2N682		75	
2N683		150	
2N685		300	
2N688		500	
2N690		720	
2N692		960	
*RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	25	Amps
*Average On-State Current (T_C = 65°C)	$I_{T(AV)}$	16	Amps
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)	I_{TSM}	150	Amps
Circuit Fusing Considerations (T_J = −40 to +125°C, t = 1 to 8.3 ms)	I^2t	93	A^2s
*Peak Gate Power	P_{GM}	5	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt

*Indicates JEDEC Registered Data

(cont.)

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

MAXIMUM RATINGS — continued (T_J = 125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Forward Gate Current 2N682–2N688 2N690, 2N692	I_{GM}	2 1.2	Amps
*Peak Gate Voltage — Forward Reverse	V_{FGM} V_{RGM}	10 5	Volts
*Operating Junction Temperature Range	T_J	−65 to +125	°C
*Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open, T_J = 125°C) 2N682–2N683 2N685 2N688 2N690 2N692	$I_{D(AV)}$, $I_{R(AV)}$	 — — — — —	 — — — — —	 6.5 6 4 2.5 2	mA
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	 — —	 — —	 10 20	 μA mA
*Peak On-State Voltage (I_{TM} = 50.3 A peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	2	Volts
Gate Trigger Current (Continuous dc) (V_{AK} = 12 Vdc, R_L = 50 Ω) *(V_{AK} = 12 Vdc, R_L = 50 Ω, T_C = −65°C)	I_{GT}	 — —	 — —	 40 80	mA
Gate Trigger Voltage (Continuous dc) (V_{AK} = 12 Vdc, R_L = 50 Ω) *(V_{AK} = 12 Vdc, R_L = 50 Ω, T_J = −65°C)	V_{GT}	 — —	 0.65 —	 2 3	Volts
*Gate Non-Trigger Voltage (Rated V_{DRM}, R_L = 50 Ω, T_J = 125°C)	V_{GD}	0.25	—	—	Volts
Holding Current (V_{AK} = 12 Vdc, Gate Open)	I_H	—	7.3	50	mA
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Exponential Waveform, T_J = 125°C, Gate Open)	dv/dt	—	30	—	V/μs

*Indicates JEDEC Registered Data.

3

TYPICAL CHARACTERISTICS

FIGURE 1 – AVERAGE CURRENT DERATING

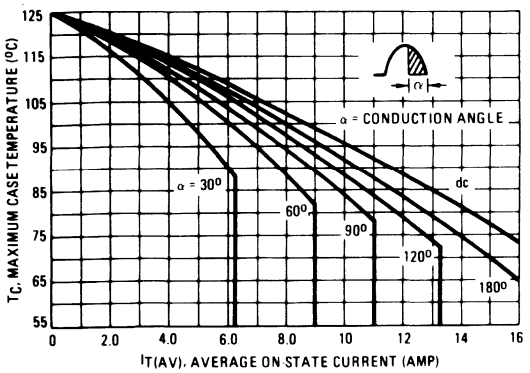


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

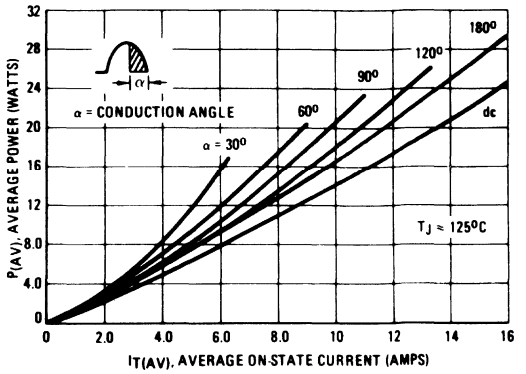


FIGURE 3 – ON-STATE CHARACTERISTICS

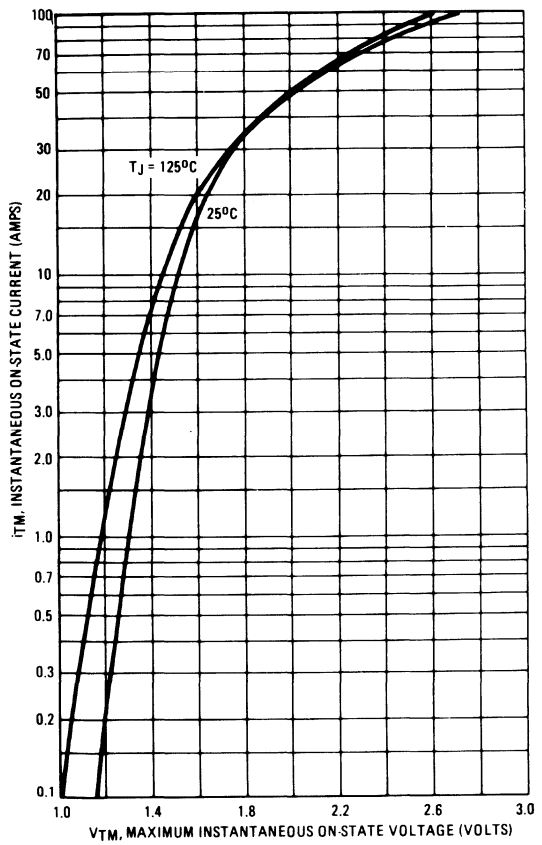
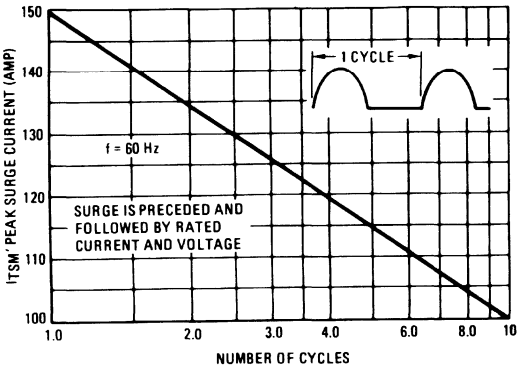


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT



3

FIGURE 5 – THERMAL RESPONSE

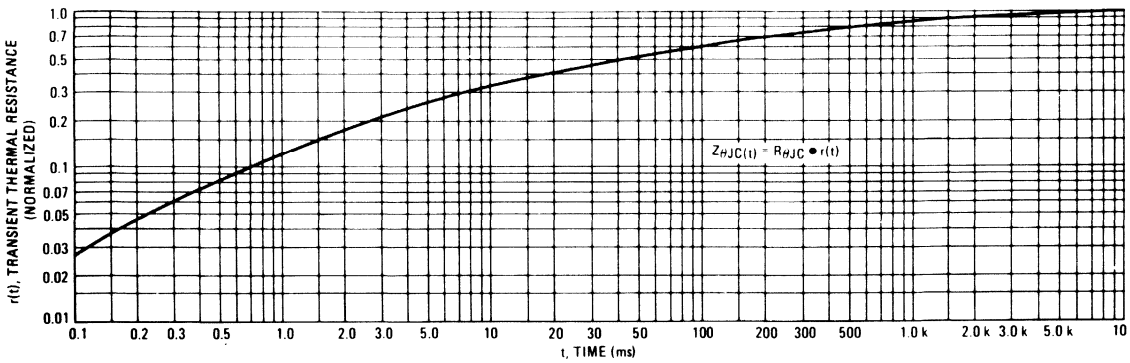


FIGURE 6 – PULSE TRIGGER CURRENT

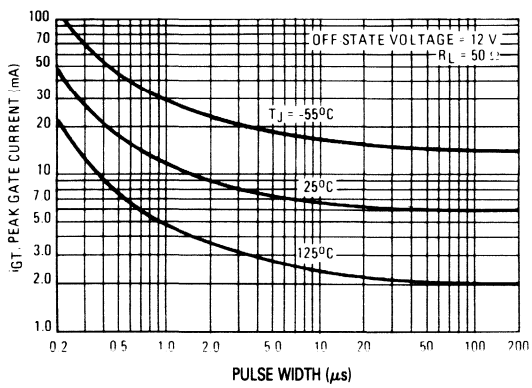


FIGURE 7 – GATE TRIGGER CURRENT

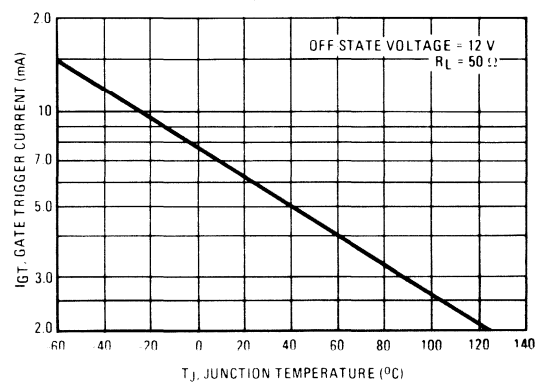


FIGURE 8 – GATE TRIGGER VOLTAGE

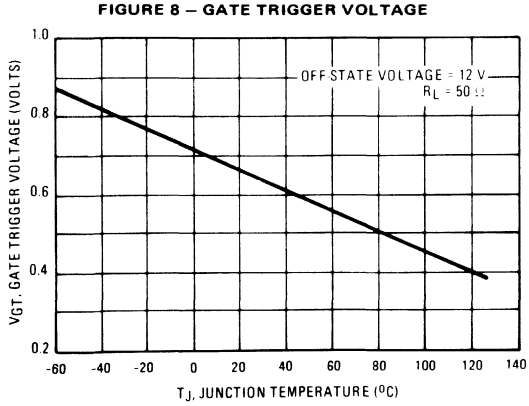
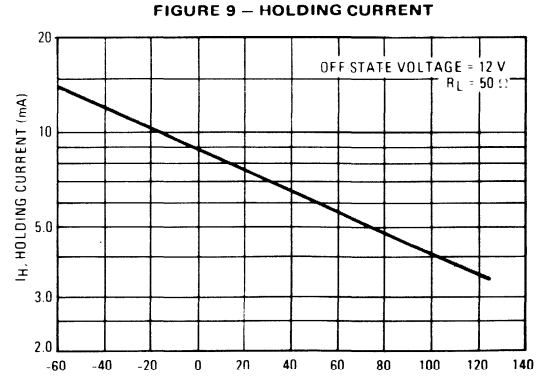


FIGURE 9 – HOLDING CURRENT



3

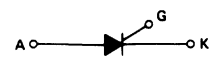
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristors

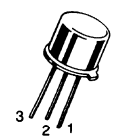
2N1595 thru 2N1599

SCRs
1.6 AMPERES RMS
50 thru 600 VOLTS

These devices are glassivated planar construction designed for gating operation in mA/μA signal or detection circuits.

- Low-Level Gate Characteristics — I_{GT} = 10 mA (Max) @ 25°C
- Low Holding Current — I_H = 5 mA (Typ) @ 25°C
- Glass-to-Metal Bond for Maximum Hermetic Seal





CASE 79-04
(TO-205AD)
STYLE 3

3

***MAXIMUM RATINGS** (T_J = 125°C unless otherwise noted, R_{GC} = 1 kΩ.)

Rating		Symbol	Value	Unit
Repetitive Peak Reverse Blocking Voltage, Note 1	2N1595 2N1596 2N1597 2N1599	V_{RRM}	50 100 200 400	Volts
Repetitive Peak Forward Blocking Voltage, Note 1	2N1595 2N1596 2N1597 2N1599	V_{DRM}	50 100 200 400	Volts
RMS On-State Current (All Conduction Angles)		$I_{T(RMS)}$	1.6	Amps
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_J = −65 to +125°C)		I_{TSM}	15	Amps
Peak Gate Power		P_{GM}	0.1	Watt
Average Gate Power		$P_{G(AV)}$	0.01	Watt
Peak Gate Current		I_{GM}	0.1	Amp
Peak Gate Voltage — Forward Reverse		V_{GFM} V_{GRM}	10 10	Volts
Operating Junction Temperature Range		T_J	−65 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

*Indicates JEDEC Registered Data.

Note 1. V_{DRM} or V_{RRM} for all types can be applied on a continuous DC basis without incurring damage.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	— —	— —	10 6	μA mA
*Peak On-State Voltage (I_F = 1 Adc, Pulsed, 1 ms (Max), Duty Cycle ≤ 1%)	V_{TM}	—	1.1	2	Volts
*Gate Trigger Current (Continuous dc) (V_D = 7 V, R_L = 12 Ohms)	I_{GT}	—	2	10	mA
*Gate Trigger Voltage (Continuous dc) (V_D = 7 V, R_L = 12 Ohms) (V_D = 7 V, R_L = 12 Ohms, T_J = 125°C)	V_{GT}	— 0.2	0.7 —	3 —	Volts
Reverse Gate Current (V_{GK} = 10 V)	I_{GR}	—	17	—	mA
Holding Current (V_D = 7 V)	I_H	—	5	—	mA
Turn-On Time (I_{GT} = 10 mA, I_F = 1 A) (I_{GT} = 20 mA, I_F = 1 A)	t_{gt}	— —	0.8 0.6	— —	μs
Turn-Off Time (I_F = 1 A, I_R = 1 A, dv/dt = 20 V/μs, T_J = 125°C)	t_q	—	10	—	μs

*Indicates JEDEC Registered Data.

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE REFERENCE

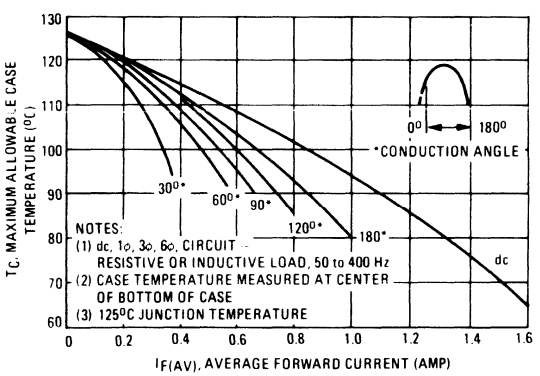
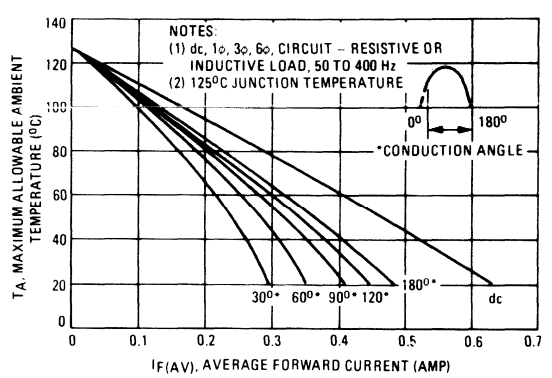


FIGURE 2 – AMBIENT TEMPERATURE REFERENCE



3

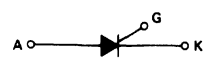
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristor

2N1843 thru 2N1849

SCRs
16 AMPERES RMS
50 thru 400 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Blocking Voltage to 400 Volts



CASE 263-04
STYLE 1

3

MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage, Note 1 2N1843 2N1844 2N1846 2N1849	V_{DRM} or V_{RRM}	 50 100 200 400	Volts
*Non-Repetitive Peak Reverse Voltage 2N1843 2N1844 2N1846 2N1849	V_{RSM}	 75 150 300 500	Volts
*Average On-State Current (T_C = 35°C)	$I_{T(AV)}$	10	Amps
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)	I_{TSM}	125	Amps
Circuit Fusing (T_J = −40 to +100°C, t = 1 to 8.3 ms)	I^2t	60	A^2s
*Peak Gate Power	P_{GM}	5	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2	Amps
*Peak Gate Voltage — Forward Reverse	V_{FGM} V_{RGM}	10 5	Volts
*Operating Junction Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +125	°C

*Indicates JEDEC Registered Data.

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (V_D = Rated V_{DRM}, V_R = Rated V_{RRM}, T_C = 35°C)	$I_{D(AV)}$, $I_{R(AV)}$				mA
2N1843		—	—	19	
2N1844		—	—	12.5	
2N1846		—	—	6	
2N1849		—	—	4	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = 100°C		—	—	6	mA
*Peak On-State Voltage (I_{TM} = 31.4 A peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	2.5	Volts
Gate Trigger Current (Continuous dc)	I_{GT}				mA
(V_D = 12 Vdc, R_L = 50 Ω)		—	6	80	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −40°C)		—	—	150	
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_D = 12 Vdc, R_L = 50 Ω)		—	0.65	—	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −40°C)		—	—	3.5	
*(V_D Rated V_{DRM}, R_L = 50 Ω, T_C = 100°C)		0.3	—	—	
Holding Current (V_D = 12 Vdc, Gate Open)	I_H	—	7	—	mA
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 100°C, Gate Open)	dv/dt	—	30	—	V/μs

*Indicates JEDEC Registered Data.

3

FIGURE 1 – AVERAGE CURRENT DERATING

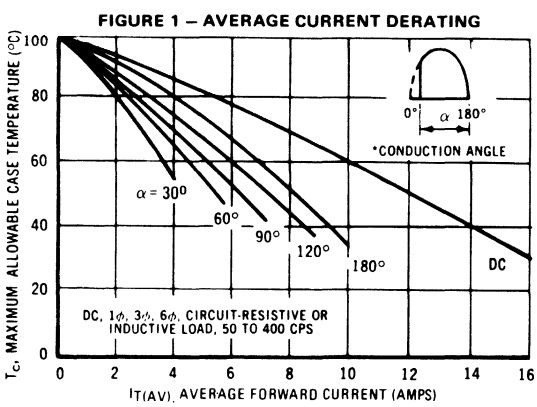


FIGURE 2 – GATE TRIGGER CURRENT

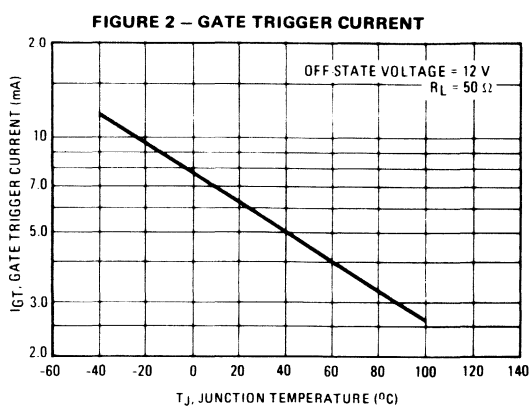


FIGURE 3 – GATE TRIGGER VOLTAGE

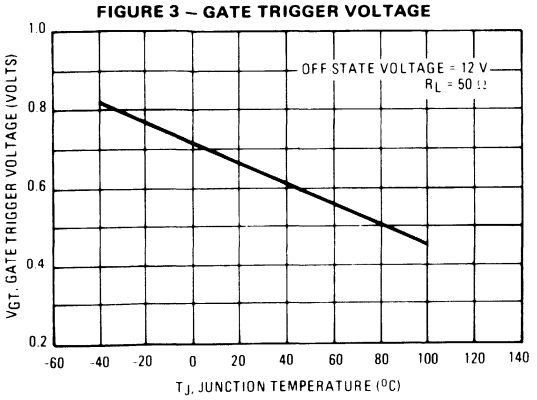
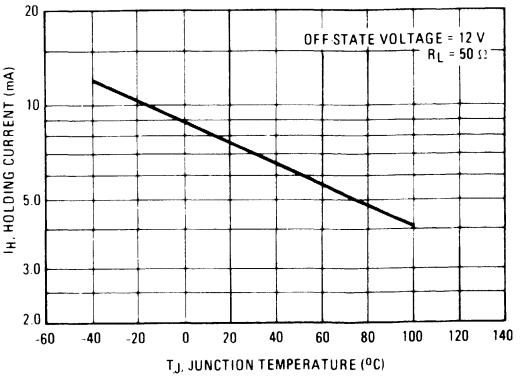


FIGURE 4 – HOLDING CURRENT



3

Silicon Controlled Rectifiers

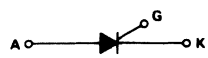
Reverse Blocking Triode Thyristor

2N1843A thru 2N1849A

SCRs
16 AMPERES RMS
50 thru 400 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Blocking Voltage to 400 Volts
- Junction Temperature Rated @ 125°C



CASE 263-04
STYLE 1

MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage, Note 1 2N1843A 2N1844A 2N1846A 2N1849A	V_{DRM} or V_{RRM}	 50 100 200 400	Volts
*Non-Repetitive Peak Reverse Voltage 2N1843A 2N1844A 2N1846A 2N1849A	V_{RSM}	 75 150 300 500	Volts
*Average On-State Current (T_C = 80°C)	$I_{T(AV)}$	10	Amps
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)	I_{TSM}	125	Amps
Circuit Fusing (T_J = >5 to +125°C, t = 1 to 8.3 ms)	I^2t	60	A^2s
*Peak Gate Power	P_{GM}	5	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2	Amps
*Peak Gate Voltage — Forward Reverse	V_{FGM} V_{RGM}	10 5	Volts
*Operating Junction Temperature Range	T_J	−65 to +125	°C
*Storage Temperature Range	T_{stg}	−65 to +125	°C

*Indicates JEDEC Registered Data.

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (V_D = Rated V_{DRM} or V_R = Rated V_{RRM}, gate open, T_C = 125°C)	$I_{D(AV)}$, $I_{R(AV)}$				mA
2N1843A		—	—	19	
2N1844A		—	—	12.5	
2N1846A		—	—	6	
2N1849A		—	—	4	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	6	mA
*Peak On-State Voltage (I_{TM} = 31.4 A peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	2.5	Volts
Gate Trigger Current (Continuous dc)	I_{GT}				mA
(V_D = 12 Vdc, R_L = 50 Ω)		—	6	80	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −65°C)		—	—	150	
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_D = 12 Vdc, R_L = 50 Ω)		—	0.65	—	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −40°C)		—	—	3.5	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = −65°C)		—	—	3.7	
*(V_D = Rated V_{DRM}, R_L = 50 Ω, T_C = 125°C)		0.25	—	—	
Holding Current (V_D = 12 Vdc, Gate Open)	I_H	—	7	—	mA
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C, Gate Open)	dv/dt	—	30	—	V/μs

*Indicates JEDEC Registered Data.

3

FIGURE 1 – AVERAGE CURRENT DERATING

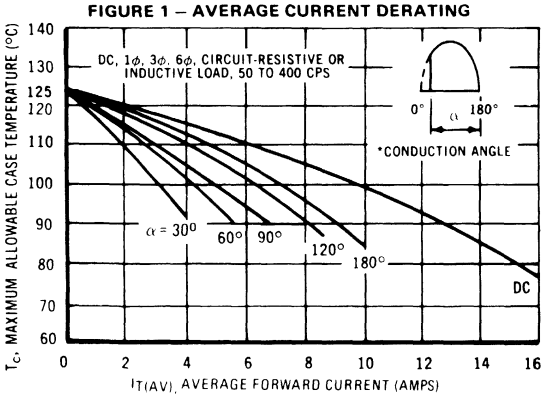


FIGURE 2 – GATE TRIGGER CURRENT

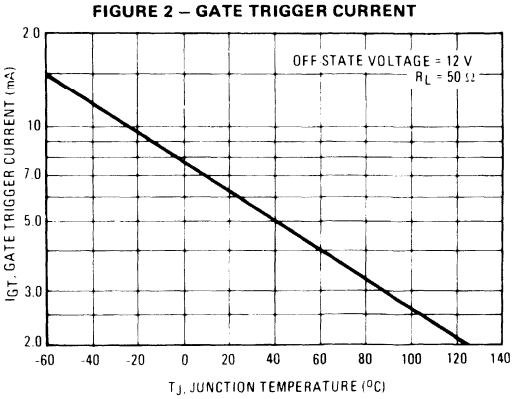


FIGURE 3 – GATE TRIGGER VOLTAGE

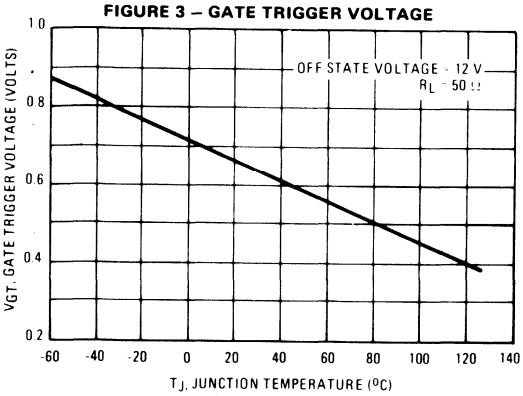
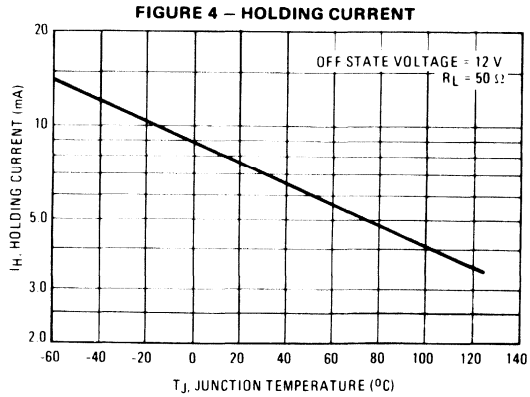


FIGURE 4 – HOLDING CURRENT



3

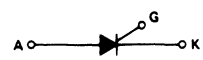
Silicon Controlled Rectifier
Reverse Blocking Triode Thyristor

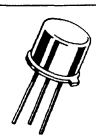
2N2323 thru 2N2329

SCRs
1.6 AMPERES RMS
50 thru 400 VOLTS

. . . all diffused PNP devices designed for gating operation in mA/μA signal or detection circuits.

- Low-Level Gate Characteristics — I_{GT} = 200 μA (Max) @ 25°C
- Low Holding Current — I_H = 2 mA (Max) @ 25°C
- Anode Common to Case
- Glass-to-Metal Bond for Maximum Hermetic Seal





CASE 79-04
(TO-205AD)
STYLE 3

3

***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage, Notes 1 and 2 2N2323 2N2324 2N2326 2N2329	V_{DRM} or V_{RRM}	 50 100 200 400	Volts
Non-Repetitive Peak Reverse Blocking Voltage (t ≤ 5 ms, Notes 1 and 2) 2N2323 2N2324 2N2326 2N2329	V_{RSM}	 75 150 300 500	Volts
RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amps
Average On-State Current T_C = 85°C T_A = 30°C	$I_{T(AV)}$	1 0.45	Amp
Peak Non-Repetitive Surge Current (One cycle, 60 Hz, T_C = 80°C) Preceded and followed by rated current and voltage	I_{TSM}	15	Amps

*Indiciates JEDEC Registered Data.

(cont.)

Notes: 1. Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

2. Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

***MAXIMUM RATINGS — continued** (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Rating	Symbol	Value	Unit
Peak Gate Power	P_{GM}	0.1	Watt
Average Gate Power	$P_{G(AV)}$	0.01	Watt
Peak Gate Current	I_{GM}	0.1	Amp
Peak Gate Voltage	V_{GM}	6	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Solder Temperature (>1/16" from case, 10 s max)	—	+230	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Characteristic	Symbol	Min	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	10	μA
T_J = 125°C		—	100	μA
Peak On-State Voltage (I_{TM} = 1 A peak)	V_{TM}	—	1.5	Volts
(I_{TM} = 3.14 A Peak, T_C = 85°C)*		—	2	
Gate Trigger Current (Continuous dc), Note 1 (V_D = 6 Vdc, R_L = 100 ohms)	I_{GT}	—	200	μA
(V_D = 6 Vdc, R_L = 100 ohms, T_C = −65°C)		—	350*	
Gate Trigger Voltage (Continuous dc) (V_D = 6 Vdc, R_L = 100 ohms)	V_{GT}	—	0.8	Volts
(V_D = 6 Vdc, R_L = 100 ohms, T_C = −65°C)*		—	1	
(V_D = Rated V_{DRM}, R_L = 100 ohms, T_J = 125°C)*		0.1	—	
Holding Current (V_D = 6 Vdc)	I_H	—	2	mA
(V_D = 6 Vdc, T_C = −65°C)*		—	3	
(V_D = 6 Vdc, T_C = 125°C)*		0.15	—	

*Indicates JEDEC Registered Data.

Note 1. R_{GK} current is not included in measurement.

3

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE

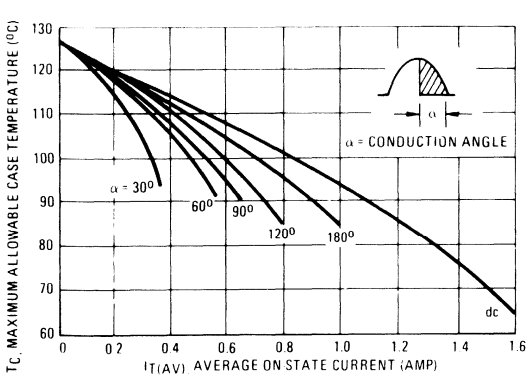
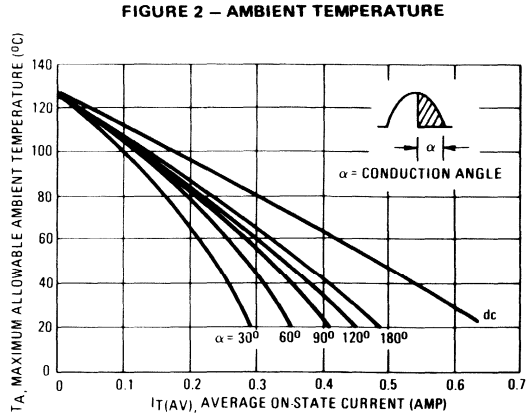


FIGURE 2 – AMBIENT TEMPERATURE



Silicon Controlled Rectifier

Reverse Blocking Triode Thyristor

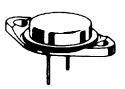
2N2574 thru 2N2579 MCR649AP 1 thru 10

SCRs
20 and 25 AMPERES RMS
25 thru 800 VOLTS

. . . designed for industrial applications such as motor controls, heater controls, and power supplies, wherever half-wave or dc silicon gate controlled devices are needed.

- Glass Passivated Junctions for Maximum Reliability
- Center Gate Geometry for Parameter Uniformity
- High Surge Current, I_{TSM} = 260 A, for Crowbar Service

CASE 61-03
STYLE 1
2N2574 thru 2N2579



CASE 54-05
STYLE 2
MCR649AP-1 thru MCR649AP-10

MAXIMUM RATINGS (T_J = 125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage, Note 1	V_{DRM} or V_{RRM}		Volts
MCR649AP1		25	
2N2574, MCR649AP2		50	
2N2575, MCR649AP3		100	
2N2576, MCR649AP4		200	
2N2578, MCR649AP6		400	
MCR649AP8		600	
MCR649AP9		700	
MCR649AP10		800	
On-State Current — 2N Series	$I_{T(RMS)}$	25	Amps
On-State Current — MCR Series		20	
Circuit Fusing (T_J = −65°C to +125°C, t ≤ 8.3 ms) — 2N Series	I^2t	275	A^2s
Circuit Fusing (T_J = −65°C to +125°C, t ≤ 8.3 ms) — MCR Series		235	
Peak Surge Current (Half Cycle, 60 Hz, T_J = −65° to +125°C)	I_{TSM}	260	Amps
Peak Gate Power — Forward	P_{GM}	5	Watts
Average Gate Power — Forward	$P_{G(AVG)}$	0.5	Watt
Peak Gate Current — Forward	I_{GM}	2	Amps
Peak Gate Voltage — Forward	V_{GFM}	10	Volts
Peak Gate Voltage — Reverse	V_{GRM}	5	
Operating Junction Temperature	T_J	−65 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis without incurring damage. Ratings apply for zero or negative gate voltage.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	— —	— 0.6	10 5	μA mA
Gate Trigger Current (Continuous dc) (V_D = 7 Vdc, R_L = 100 Ω)	I_{GT}	—	—	40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 100 Ω) (V_D = Rated V_{DRM}, R_L = 100 Ω, T_J = 125°C)	V_{GT}	— 0.3	0.7 —	3.5 —	Volts
Forward On Voltage (I_{TM} = 20 Adc)	V_{TM}	—	1.1	1.4	Volts
Holding Current (V_D = 7 Vdc, Gate Open)	I_H	—	10	—	mA
Turn-On Time (t_d + t_r) (I_{GT} = 50 mA, I_T = 10 A, V_D = Rated V_{DRM})	t_{gt}	—	1	—	μs
Turn-Off Time (I_T = 10 A, I_R = 10 A, dv/dt = 20 V/μs, T_J = 125°C) (V_D = Rated Voltage V_{DRM})	t_q	—	30	—	μs
Forward Voltage Application Rate (Exponential) (Gate Open, T_J = 125°C, V_D = Rated V_{DRM})	dv/dt	—	30	—	V/μs

FIGURE 1 – CURRENT DERATING

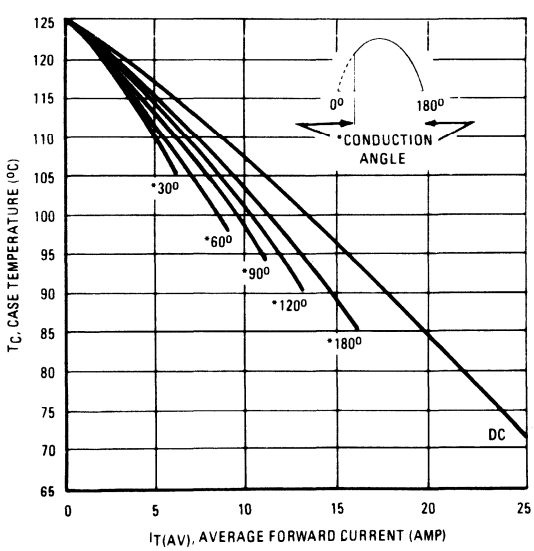


FIGURE 2 – GATE TRIGGER CHARACTERISTICS

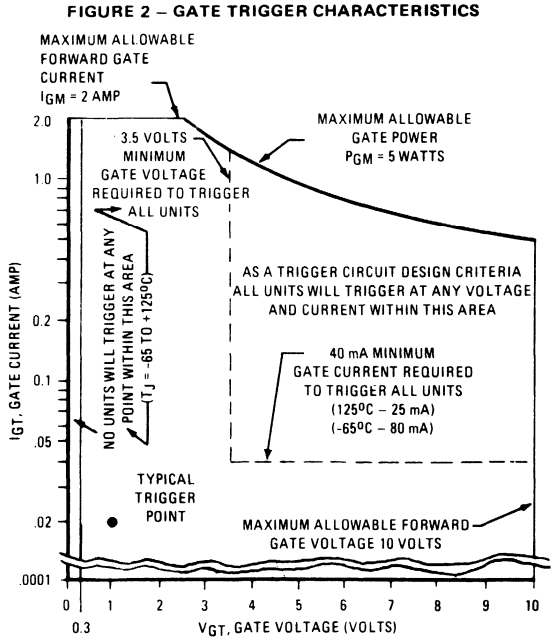


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FIGURE 3 – ON-STATE CHARACTERISTICS

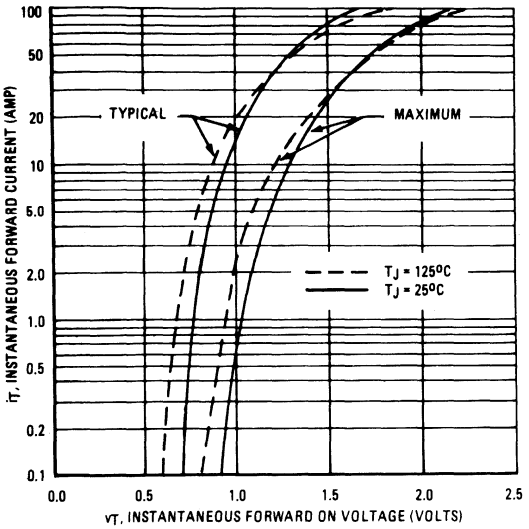


FIGURE 4 – MAXIMUM ALLOWABLE NON-RECURRENT SURGE CURRENT

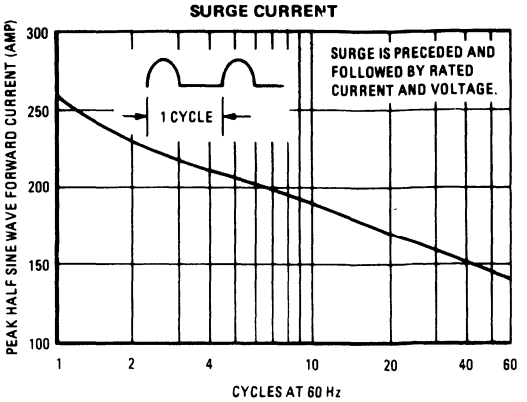


FIGURE 5 – EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT

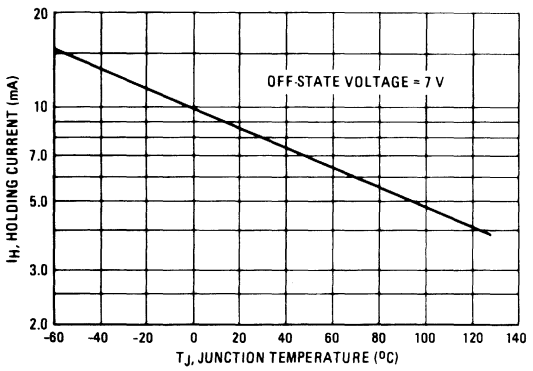


FIGURE 6 – EFFECT OF TEMPERATURE ON TYPICAL GATE CURRENT

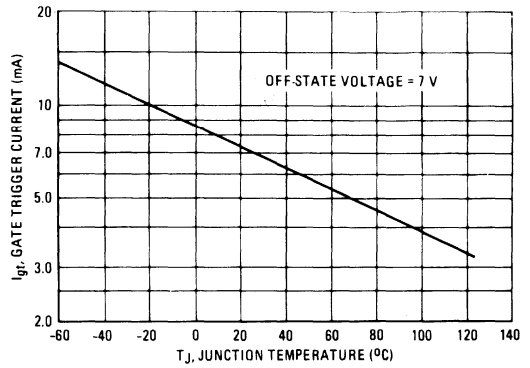


FIGURE 7 – EFFECT OF TEMPERATURE ON TYPICAL GATE VOLTAGE

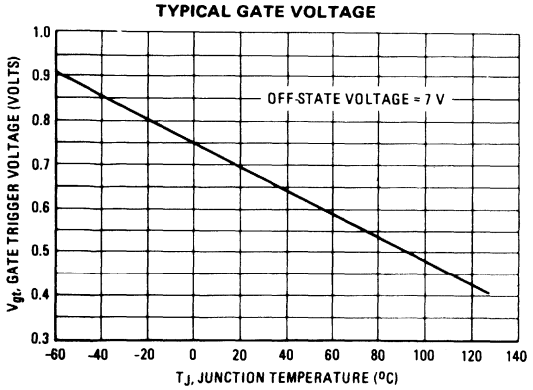
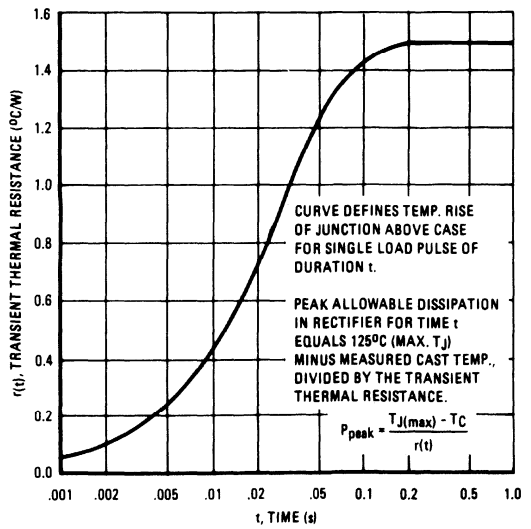


FIGURE 8 – MAXIMUM TRANSIENT THERMAL RESISTANCE JUNCTION TO CASE



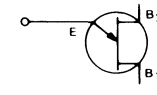
PN Unijunction Transistors
Silicon PN Unijunction Transistors

2N2646
2N2647

PN UJTs

. . . designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits. These devices feature:

- Low Peak Point Current — 2 μA (Max)
- Low Emitter Reverse Current — 200 nA (Max)
- Passivated Surface for Reliability and Uniformity



CASE 22A-01
STYLE 1

***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Dissipation, Note 1	P_D	300	mW
RMS Emitter Current	$I_{E(RMS)}$	50	mA
Peak Pulse Emitter Current, Note 2	i_E	2	Amps
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

*Indicates JEDEC Registered Data.

Notes: 1. Derate 3 mW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.

2. Capacitor discharge — 10 μF or less, 30 volts or less.

3

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V), Note 1	2N2646 2N2647	η	0.56 0.68	— —	0.75 0.82	—
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)		r_{BB}	4.7	7	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = −55°C to +125°C)		αr_{BB}	0.1	—	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA), Note 2		$V_{EB1(sat)}$	—	3.5	—	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	—	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	2N2646 2N2647	I_{EB2O}	— —	0.005 0.005	12 0.2	μA
Peak Point Emitter Current (V_{B2B1} = 25 V)	2N2646 2N2647	I_P	— —	1 1	5 2	μA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms), Note 2	2N2646 2N2647	I_V	4 8	6 10	— 18	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N2646 2N2647	V_{OB1}	3 6	5 7	— —	Volts

*Indicates JEDEC Registered Data.

Notes:

1. Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_F}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
V_F = Emitter to Base-One Junction Diode Drop (≈ 0.45 V @ 10 μA)

2. Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.
3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1
UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

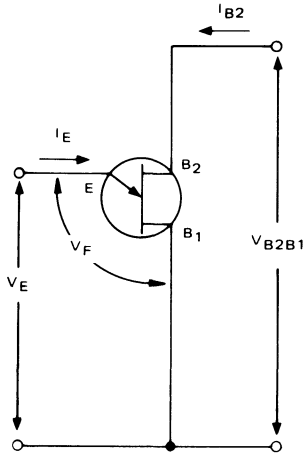


FIGURE 2
STATIC EMITTER CHARACTERISTIC CURVES
(Exaggerated to Show Details)

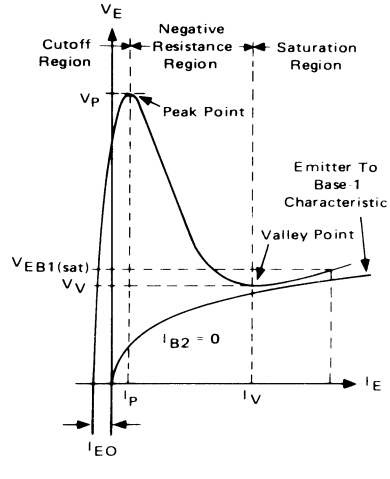
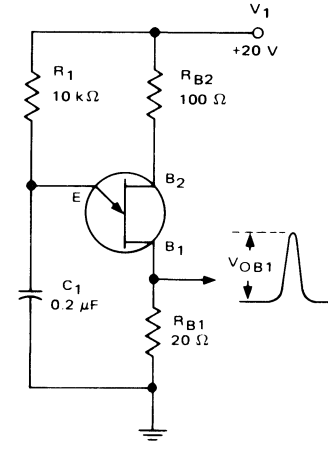


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)



Silicon Controlled Rectifiers

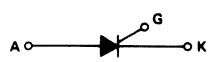
Reverse Blocking Triode Thyristors

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 350 Amp
- Practical Level Triggering and Holding Characteristics — 4 and 5.2 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud or Isolated Stud Package

2N3870 thru 2N3873
2N3896 thru 2N3899
2N6171 thru 2N6174

SCRs
35 AMPERES RMS
100 thru 800 VOLTS



MAXIMUM RATINGS (T_C = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage, Note 1 (T_J = −40 to +100°C, 1/2 Sine Wave, 50 to 400 Hz, Gate Open)	V_{RRM} or V_{DRM}		Volts
2N3870, 2N3896, 2N6171		100	
2N3871, 2N3897, 2N6172		200	
2N3872, 2N3898, 2N6173		400	
2N3873, 2N3899, 2N6174		600	
*Peak Non-Repetitive Forward or Reverse Blocking Voltage (t ≤ 5 ms)	V_{RSM} or V_{DSM}		Volts
2N3870, 2N3896, 2N6171		150	
2N3871, 2N3897, 2N6172		330	
2N3872, 2N3898, 2N6173		660	
2N3873, 2N3899, 2N6174		700	
*Average On-State Current, Note 2	$I_{T(AV)}$		Amps
(T_C = −40 to +65°C)		22	
(T_C = +85°C)		11	
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz) (T_C = +65°C)	I_{TSM}	350	Amps
Circuit Fusing (T_C = −40 to +100°C) (t = 1 to 8.30 ms)	I^2t	510	A^2s

* Indicates JEDEC Registered Data.

Notes: 1. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

2. Isolated stud devices must be derated an additional 10 percent.

CASE 174-04
(TO-203)
STYLE 1
2N3870 thru 2N3873

CASE 175-03
STYLE 1
2N3896 thru 2N3899

CASE 311-02
STYLE 1
(Stud Isolated)
2N6171 thru 2N6174

3

MAXIMUM RATINGS (T_C = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Gate Power	P_{GM}	20	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2	Amps
Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Stud Torque	—	30	in. lb.

*Indicates JEDEC Registered Data.

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
2N3870 thru 2N3873, 2N3896 thru 2N3899		0.9	
2N6171 thru 2N6174		1	

* Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open, T_J = 100°C)	I_{DRM}, I_{RRM}				mA
2N3870, 2N3896, 2N6171		—	1	2	
2N3871, 2N3897, 2N6172		—	1	2.5	
2N3872, 2N3898, 2N6173		—	1	3	
2N3873, 2N3899, 2N6174		—	1	4	
(Rated V_{DRM} or V_{RRM}, gate open, T_J = 25°C) All Devices		—	—	10	μA
*Peak On-State Voltage (I_{TM} = 69 A Peak)	V_{TM}	—	1.5	1.85	Volts
*Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 24 ohms) *T_C = −40°C	I_{GT}	—	9	80	mA
T_C = 25°C		—	4	40	
*Gate Trigger Voltage (Continuous dc) (V_D = q2 V, R_L = 24 ohms) *T_C = −40°C	V_{GT}	—	0.9	3	Volts
T_C = 25°C		—	0.69	1.6	
*Holding Current (Gate Open) (V_D = 12 V, I_{TM} = 200 mA) *T_C = −40°C	I_H	—	14	90	mA
T_C = 25°C		—	5.2	50	
*Gate Controlled Turn-On Time (t_d + t_r) (I_{TM} = 41 Adc, V_D = rated V_{DRM}, I_{GT} = 40 mAdc, Rise Time ≤ 0.05 μs, Pulse Width = 10 μs)	t_{gt}	—	—	1.5	μs
Circuit Commutated Turn-Off Time	t_q				μs
(I_{TM} = 10 A, I_R = 10 A)		—	25	—	
(I_{TM} = 10 A, I_R = 10 A, T_C = 100°C)		—	35	—	
Forward Voltage Application Rate (T_C = 100°C, V_D = Rated V_{DRM})	dv/dt	—	50	—	V/μs

*Indicates JEDEC Registered Data.

3

FIGURE 1 – AVERAGE CURRENT DERATING

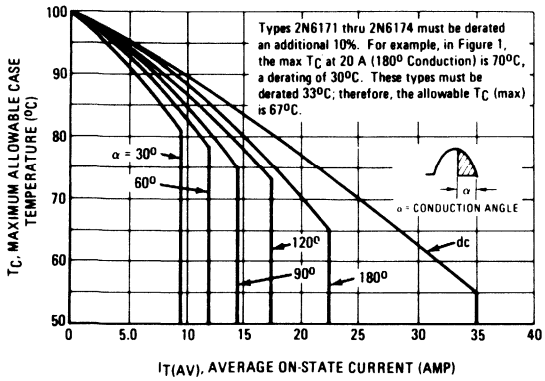


FIGURE 2 – ON-STATE POWER DISSIPATION

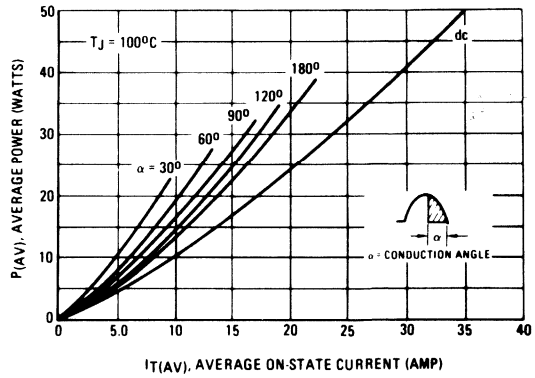


FIGURE 3 – ON-STATE CHARACTERISTICS

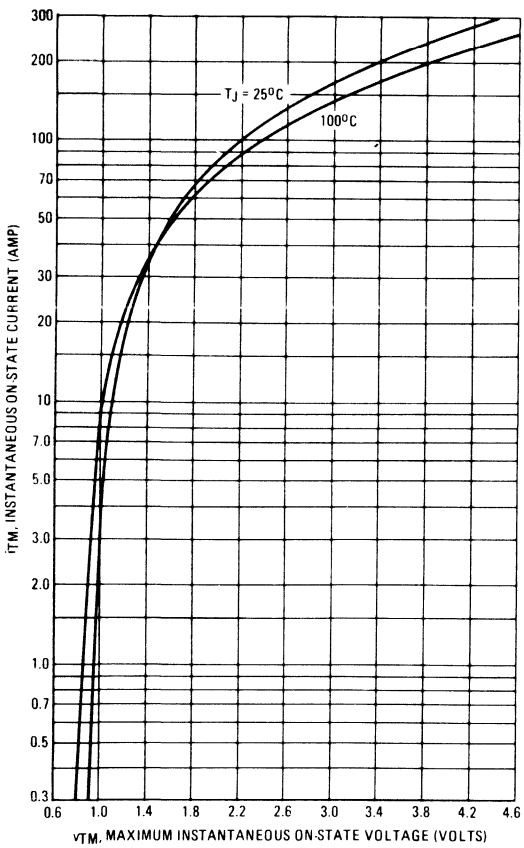


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

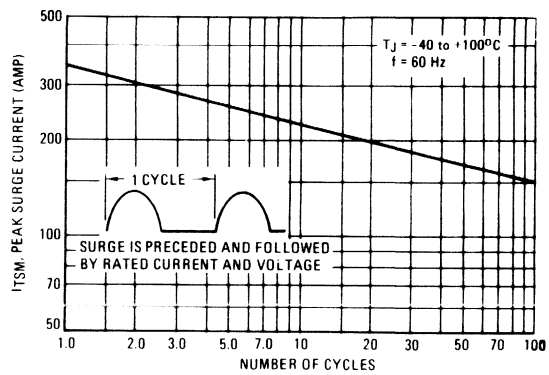


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FIGURE 5 – TYPICAL THERMAL RESPONSE

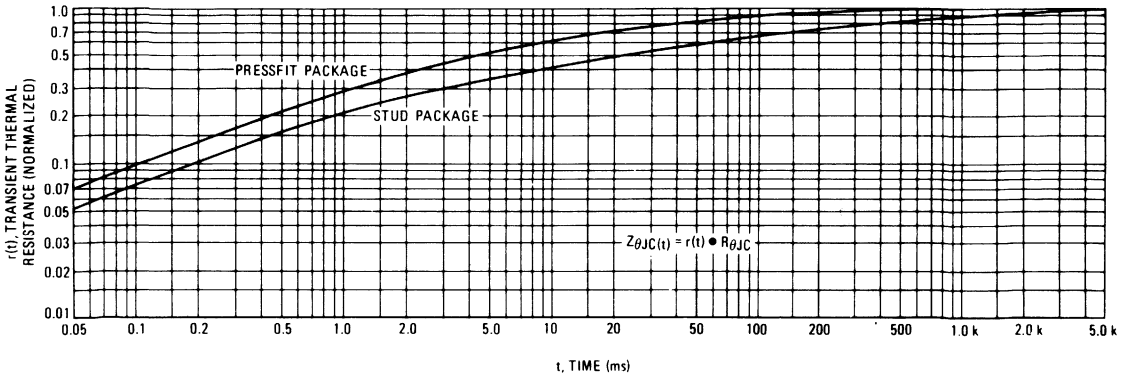


FIGURE 6 – PULSE TRIGGER CURRENT

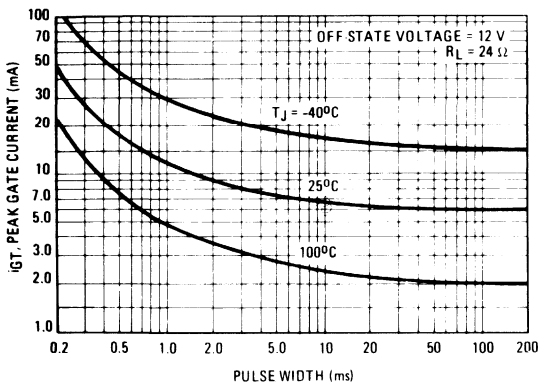


FIGURE 7 – GATE TRIGGER CURRENT

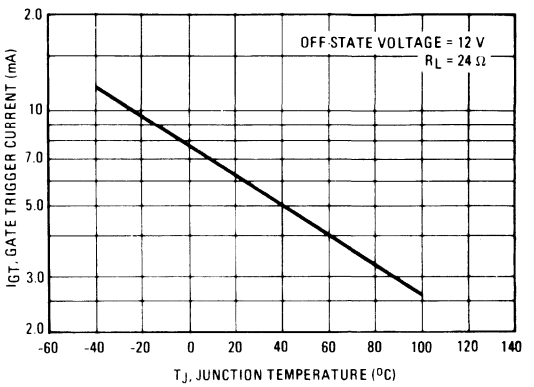


FIGURE 8 – GATE TRIGGER VOLTAGE

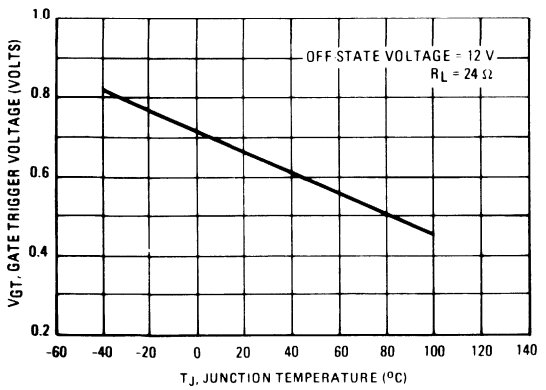
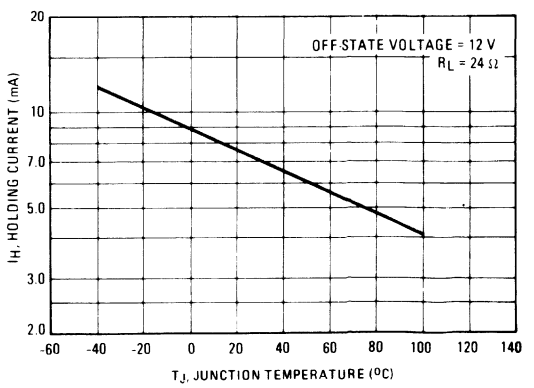


FIGURE 9 – HOLDING CURRENT



PN Unijunction Transistor

Silicon Annular PN Unijunction Transistor

2N3980

PN UJTs

. . . designed for military and industrial use in pulse, timing, sensing, and oscillator circuits. These devices feature:

- Low Peak Point Current — 2 μA max
- Fast Switching — to 1 MHz
- Low Emitter Reverse Current — 10 nA max
- Passivated Surface for Reliability and Uniformity

CASE 22A-01
STYLE 1

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Power Dissipation, Note 1	P_D	360	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current, Note 2	i_e	1	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Storage Temperature Range	T_{stg}	−65 to +200	°C

Notes: 1. Derate 2.4 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.

2. Capacitance discharge current must fall to 0.37 Amp within 3 ms and PRR ≤ 10 PPS.

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) Note 1	η	0.68	—	0.82	—
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)	R_{BB}	4	6	8	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = −65°C to +100°C)	αR_{BB}	0.4	—	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) Note 2	$V_{EB1(sat)}$	—	2.5	3	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	12	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	I_{EB20}	—	5	10	nA
(V_{B2E} = 30 V, I_{B1} = 0, T_A = 125°C)		—	—	1	μA
Peak Point Emitter Current (V_{B2B1} = 25 V)	I_P	—	0.6	2	μA

(cont.)

Notes:
1. Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - (V_{EB1})}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
V_F = Emitter to Base-One Junction Diode Drop (0.45 V @ 10 μA)

2. Use pulse techniques: PW ≈ 300 μs duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) Note 2	I_V	1	4	10	mA
Base-One Peak Pulse Voltage (Note 1, Figure 3)	V_{OB1}	6	8	—	Volts
Maximum Oscillation Frequency (Figure 4)	$f_{(max)}$	1	1.25	—	MHz

Notes:

1. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in ACR firing circuits and other types of pulse circuits.
2. Use pulse techniques: PW ≈ 300 μs duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

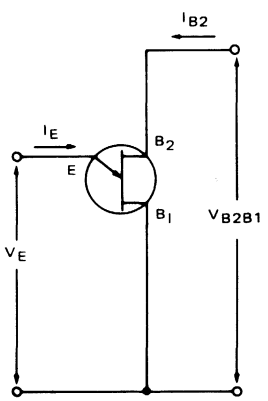


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES
(Exaggerated to Show Details)

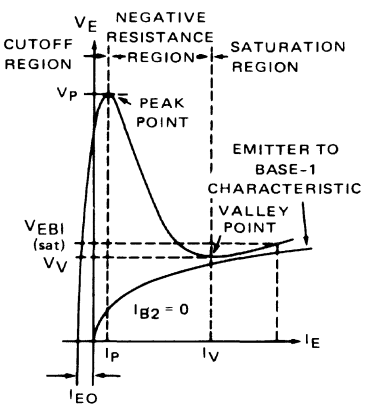


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)

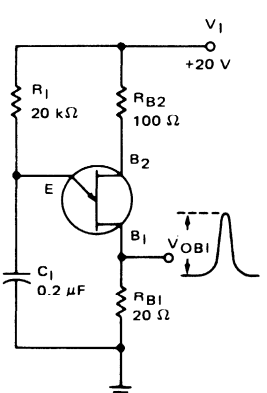
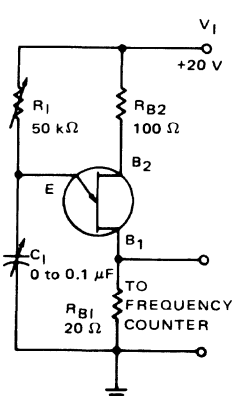


FIGURE 4 – f(max) MAXIMUM FREQUENCY TEST CIRCUIT



Silicon Controlled Rectifiers

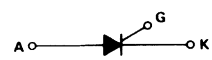
Reverse Blocking Triode Thyristor

2N4168 thru 2N4174
2N4184 thru 2N4190

SCRs
8 AMPERES RMS
50 thru 600 VOLTS

. . . multi-purpose PNPN silicon controlled rectifiers suited for industrial, consumer, and military applications. Offered in a choice of space-saving, economical packages for mounting versatility.

- Uniform Low-Level Noise-Immune Gate Triggering — I_{GT} = 10 mA (Typ) @ T_C = 25°C
- Low Forward "On" Voltage — v_T = 1 V (Typ) @ 5 Amp @ 25°C
- High Surge-Current Capability — I_{TSM} = 100 Amp Peak
- Shorted Emitter Construction

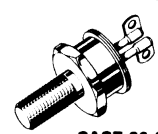


MAXIMUM RATINGS (Apply over operating temperature range and for all case types unless otherwise noted.)

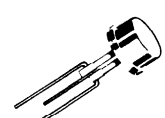
Rating	Symbol	Value	Unit
*Peak Repetitive Forward and Reverse Blocking Voltage, Note 1 — 2N4168, 84, / 2N4169, 85, / 2N4170, 86, / 2N4172, 88, / 2N4174, 90	V_{DRM} or V_{RRM}	50 / 100 / 200 / 400 / 600	Volts
Forward Current RMS	$I_{T(RMS)}$	8	Amps
*Peak Forward Surge Current (One cycle, 60 Hz, T_J = −40 to +100°C)	I_{TSM}	100	Amps
Circuit Fusing (T_J = −40 to +100°C; t ≤ 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power	P_{GM}	5	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2	Amps
Peak Gate Voltage, Note 2	V_{GM}	10	Volts
*Operating Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Stud Torque		15	in. lb.

*Indicates JEDEC Registered Data.

Notes: 1. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.
2. Devices should not be operated with a positive bias applied to the gate concurrently with a negative potential applied to the anode.



CASE 86-01
STYLE 1
2N4168 thru 2N4174



CASE 87L-02
STYLE 1
2N4184 thru 2N4190

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	2.5*	°C/W
Thermal Resistance, Case to Ambient (See Figure 11) 2N4183–98	$R_{\theta CA}$	50	—	°C/W

*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 100°C		—	—	2	mA
Gate Trigger Current (Continuous dc), Note 1	I_{GT}				mA
(V_D = 7 Vdc, R_L = 100 Ω)		—	10	30	
*(V_D = 7 Vdc, R_L = 100 Ω, T_C = −40°C)		—	—	60	
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_D = 7 Vdc, R_L = 100 Ω)		—	0.75	1.5	
*(V_D = 7 Vdc, R_L = 100 Ω, T_C = −40°C)		—	—	2.5	
*(V_D = 7 Vdc, R_L = 100 Ω, T_J = 100°C)		0.2	—	—	
*Forward "On" Voltage (pulsed, 1 ms max, duty cycle ≤ 1%) (I_{TM} = 15.7 A)	V_{TM}	—	1.4	2	Volts
Holding Current	I_H				mA
(V_D = 7 Vdc, gate open)		—	10	30	
*(V_D = 7 Vdc, gate open, T_C = −40°C)		—	—	60	
Turn-On Time (t_d + t_r) (I_G = 20 mAdc, I_F = 5 Adc, V_D = Rated V_{DRM})	t_{on}	—	1	—	μs
Turn-Off Time	t_{off}				μs
(I_F = 5 Adc, I_R = 5 Adc)		—	15	—	
(I_F = 5 Adc, I_R = 5 Adc, T_J = 100°C, V_D = Rated V_{DRM}) (dv/dt = 30 V/μs)		—	25	—	
Forward Voltage Application Rate (Exponential) (Gate open, T_J = 100°C, V_D = Rated V_{DRM})	dv/dt	—	50	—	V/μs

*Indicates JEDEC Registered Data

Note 1. For optimum operation, i.e. faster turn-on, lower switching losses, best di/dt capability, recommended I_{GT} = 200 mA minimum.

3

TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – PULSE CURRENT TRIGGERING

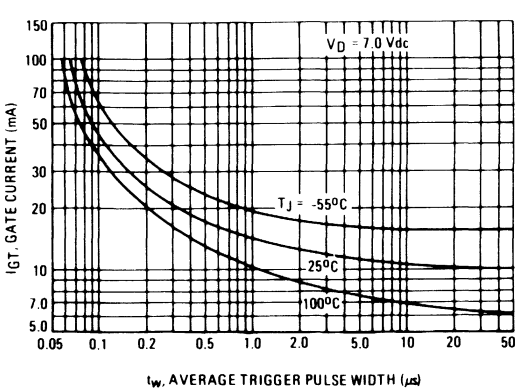
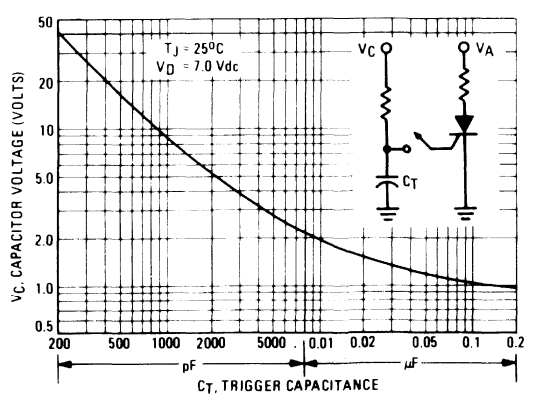


FIGURE 2 – CAPACITIVE DISCHARGE TRIGGERING



CURRENT DERATING

FIGURE 3 – MAXIMUM CASE TEMPERATURE

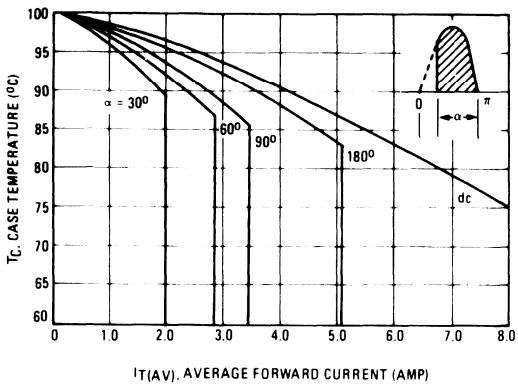


FIGURE 4 – MAXIMUM AMBIENT TEMPERATURE

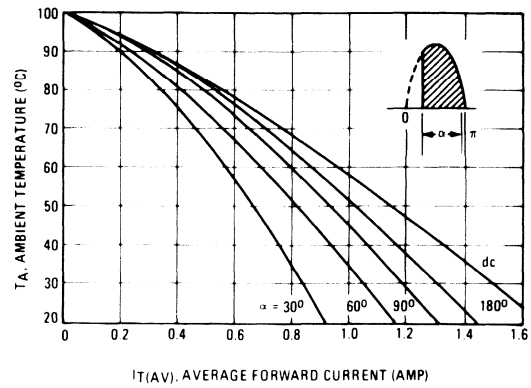


FIGURE 5 – POWER DISSIPATION

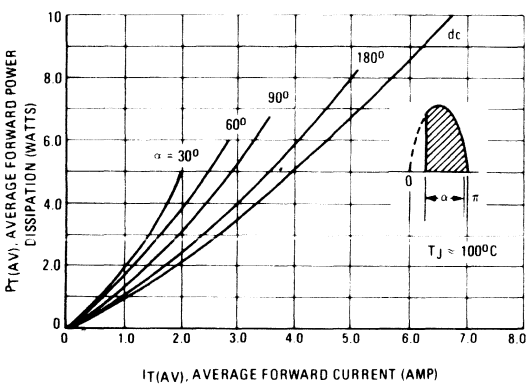


FIGURE 6 – MAXIMUM SURGE CAPABILITY

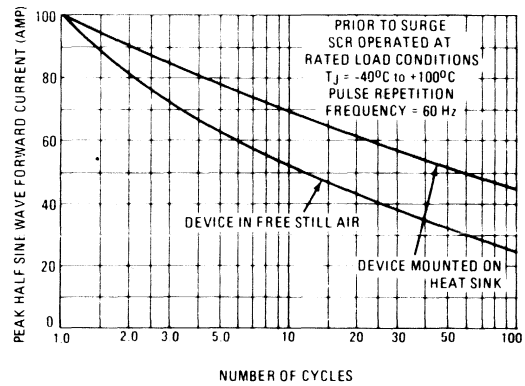


FIGURE 7 – THERMAL RESPONSE

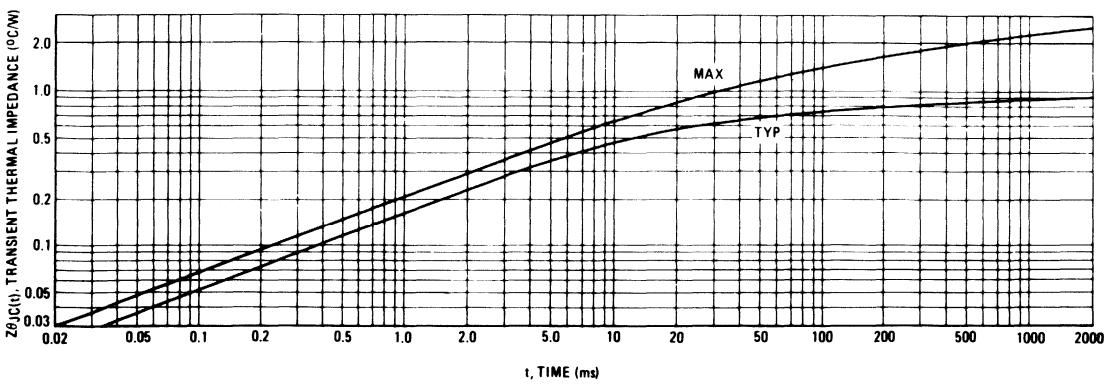


FIGURE 8 – FORWARD VOLTAGE

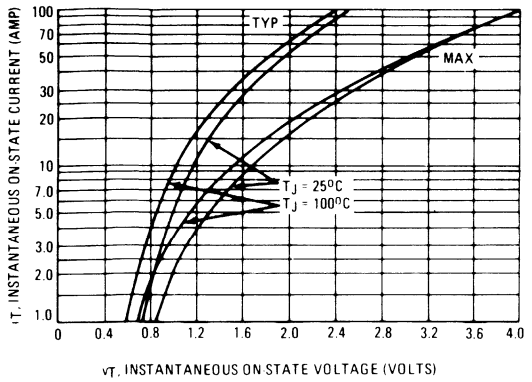


FIGURE 9 – HOLDING CURRENT

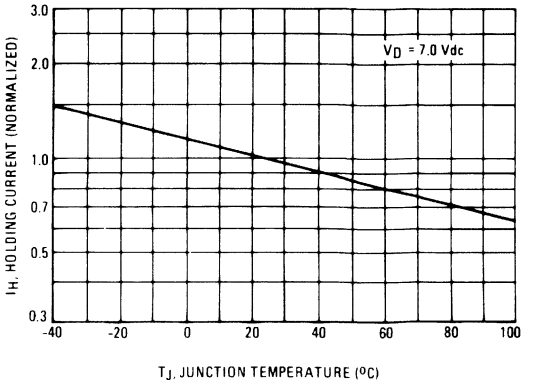


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

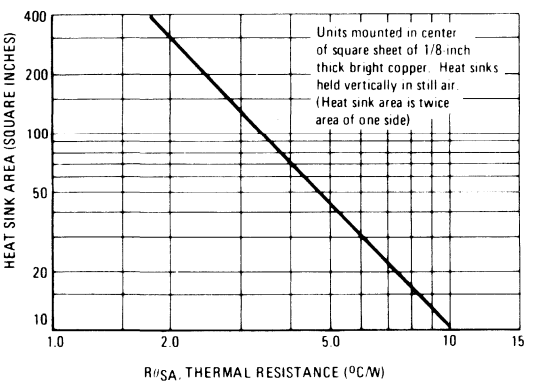
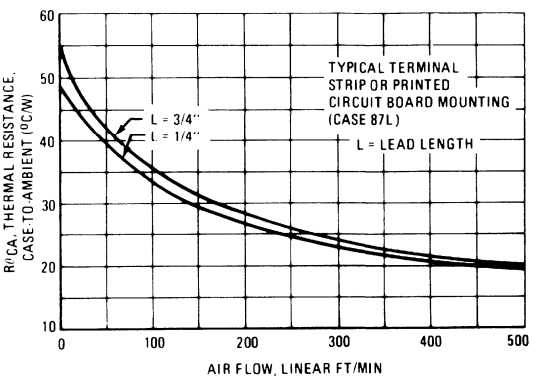


FIGURE 11 – CASE-TO-AMBIENT THERMAL RESISTANCE



3

2N4199 thru 2N4204

Designer's Data Sheet

Silicon Controlled Rectifiers

Reverse Blocking Triode Thyristor

SCRs
100 AMPERE PULSE
300 thru 800 VOLTS

. . . fast switching, high-voltage Thyristors especially designed for pulse modulator applications in radar and other similar equipment.

- Guaranteed Limits on All Critical Parameters
- High-Voltage: V_{DRM} = 300 to 800 Volts
- Maximum Turn-On Times Specified — 300 to 400 ns
- Repetitive Pulse Current to 100 Amperes
- Stable Switching Characteristics Over an Operating Temperature Range From −65 to +105°C
- Pulse Repetition Rates as High as 20,000 pps
- JAN Versions Available

CASE 63-03
(TO-64)
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage, Note 1 (T_J = 105°C)	V_{RRM}	50	Volts
*Peak Forward Blocking Voltage, Note 1 (T_C = 105°C) 2N4199	V_{DRM}	300	Volts
2N4200		400	
2N4201		500	
2N4202		600	
2N4203		700	
2N4204		800	
Repetitive Peak On-State Current (PW = 3 μs, Duty Cycle = 0.6%, T_C = 85°C)	I_{TRM}	100	Amps
Continuous On-State Current (T_C = 65°C)	I_T	5	Amps
Current Application Rate, Note 2	di/dt	5000	A/μs
Peak Forward Gate Power	P_{GFM}	20	Watts
Average Forward Gate Power	$P_{GF(AV)}$	1	Watt
Peak Forward Gate Current	I_{GFM}	5	Amps
Peak Gate Voltage — Forward	V_{GFM}	10	Volts
Reverse, Note 3	V_{GRM}	10	
Operating Junction Temperature Range	T_J		°C
Blocking State		−65 to +105	
Conducting State		−65 to +200	
Storage Temperature Range	T_{stg}	−65 to +200	°C
Stud Torque	—	15	in. lb.

*Indicates JEDEC Registered Data.

Notes: 1. Characterized for unilateral applications where reverse blocking capability is not important. Higher voltage units available upon request. V_{DRM} and V_{RRM} may be applied as a continuous dc voltage for zero or negative gate voltage but positive gate voltage must not be applied concurrently with a negative potential on the anode. When checking blocking capability, do not permit the applied voltage to exceed the rated voltage.

2. Minimum Gate Trigger Pulse: i_G = 200 mA, PW = 1 μs, t_r = 20 ns.

3. Do not reverse bias gate during forward conduction if anode current exceeds 10 amperes.

Designers Data for "Worst Case" Conditions — The Designers Data Sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

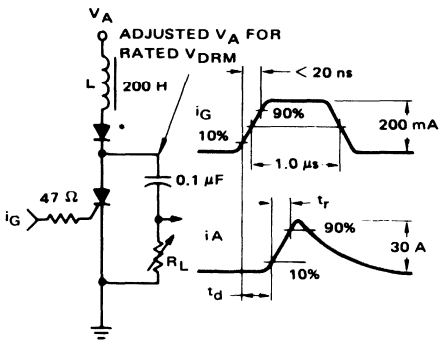
Characteristic	Fig. No.	Symbol	Min	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 105°C	17	I_{DRM}, I_{RRM}	—	2	mA
Gate Trigger Current (Continuous dc)	14	I_{GT}			mA
(Anode Voltage = 7 Vdc, R_L = 100 ohms, T_C = 25°C)			—	50	
*(Anode Voltage = 7 Vdc, R_L = 100 ohms, T_C = −65°C)			—	100	
Gate Trigger Voltage (Continuous dc)	12	V_{GT}			Volts
*(Anode Voltage = rated V_{DRM}, R_L = 100 ohms, T_C = 105°C)			0.2	—	
(Anode Voltage = 7 Vdc, R_L = 100 ohms, T_C = 25°C)			—	1.5	
*(Anode Voltage = 7 Vdc, R_L = 100 ohms, T_C = −65°C)			—	2	
*Holding Current (Anode Voltage = 7 Vdc, gate open, T_C = 105°C)	18	I_H	3	—	mA
*Forward "On" Voltage (I_{TM} = 5 Adc, PW = 1 ms max, Duty cycle ≤ 1%)	8	V_{TM}	2.6	—	Volts
*Dynamic Forward "On" Voltage (0.5 μs after 50% decay point on dynamic forward voltage waveform) Forward Current: 30 A pulse Gate Pulse: at 200 mA, PW = 1 μs, t_r = 20 ns	7	v_{TM}	—	25	Volts
*Turn-On Time I_{TM} = 30 A					ns
Delay Time — All types	1, 9	t_d	—	200	
Rise Time — 2N4199 and 2N4200	1, 11	t_r	—	200	
2N4201			—	150	
2N4202			—	130	
2N4203 and 2N4204			—	100	
*Pulse Turn-Off Time Test Conditions: PFN discharge; Forward Current = 30 A pulse; Reverse Current = 5 A, T_C = 85°C, dv/dt = 250 V/μs to Rated V_{DRM}; Reverse anode voltage during turn-off interval = 0 V; Reverse gate bias during turn-off interval = 6 V	2, 13	t_q	—	20	μs
*Forward Voltage Application Rate (Linear Rise of Voltage) (T_C = 105°C, gate open, V_D = Rated V_{DRM})	16	dv/dt	250	—	V/μs

*JEDEC Registered Data.

3

TEST CIRCUITS

FIGURE 1 – TURN-ON TIME



*Two 1N4937 fast-recovery diodes in series each shunted by a 180 kΩ resistor.

FIGURE 2 – TURN-OFF TIME

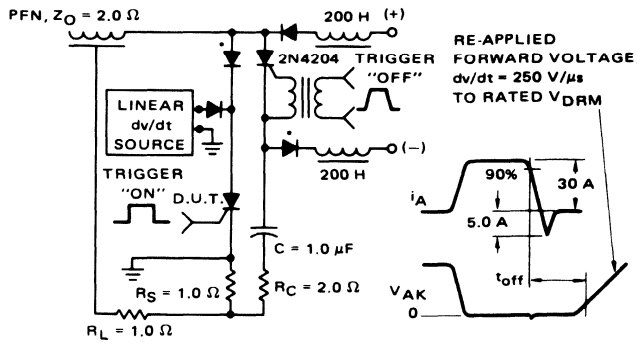


FIGURE 3 – MAXIMUM ALLOWABLE FORWARD PULSE CURRENT

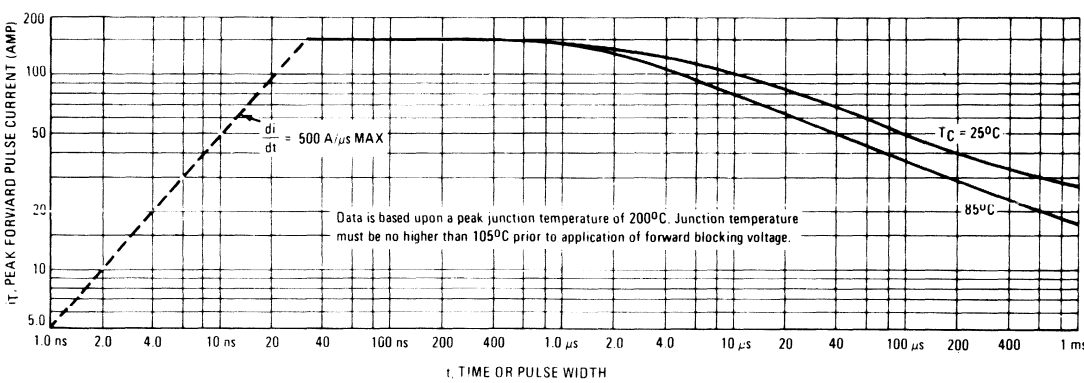


FIGURE 4 – DERATING USING NO SWITCHING LOSSES

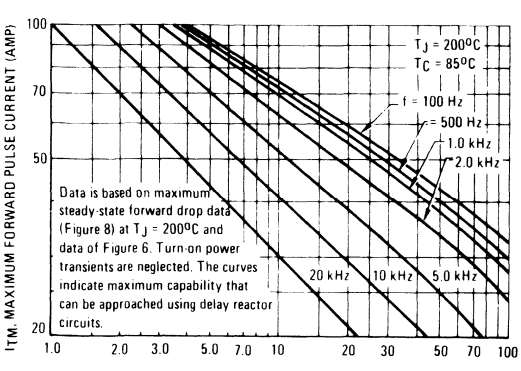


FIGURE 5 – DERATING USING TYPICAL SWITCHING LOSSES

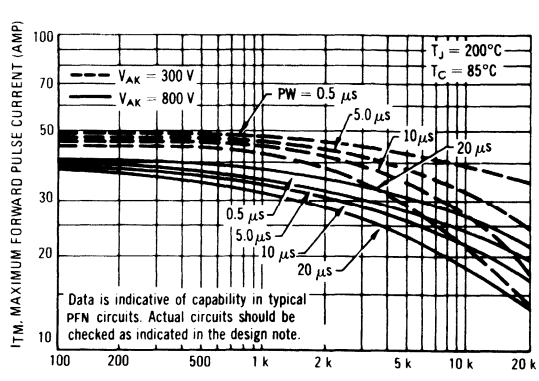
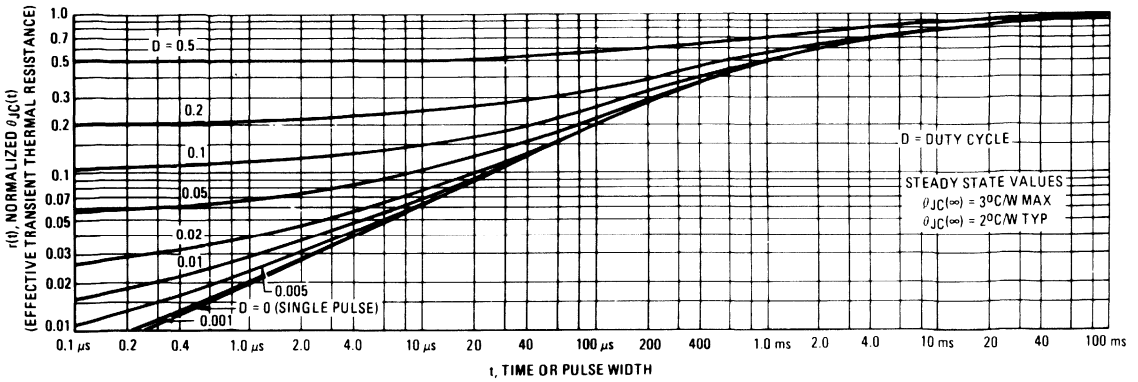


FIGURE 6 – NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE



FORWARD "ON" VOLTAGE DATA

FIGURE 7 – TYPICAL DYNAMIC FORWARD "ON" VOLTAGE

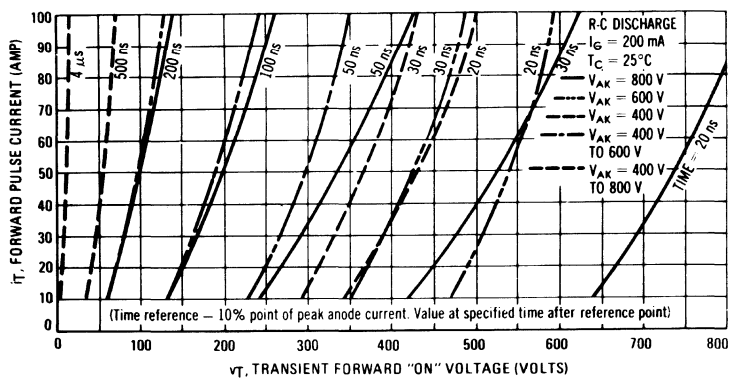
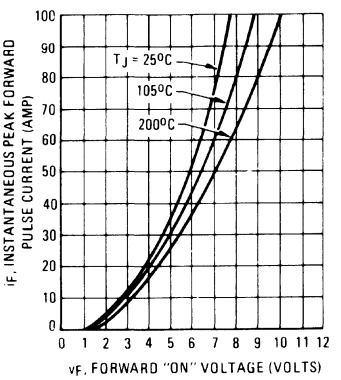


FIGURE 8 – MAXIMUM STEADY-STATE



3

DESIGN NOTE CONTINUED

$$\Delta T(t_4) = [\,1000\,[0.0205 + (1 - 5.25 \cdot 10^{-3})\,0.27 + 5.25 \cdot 10^{-3} - 0.27] + 700\,[(1 - 7.75 \cdot 10^{-3})\,0.27 + 7.75 \cdot 10^{-3} - 0.27]\,]\,3 = 93.51^{\circ}C$$

$$\Delta T(t_5) = [\,1000\,[0.032 + (1 - 5.25 \cdot 10^{-3})\,0.27 + 5.25 \cdot 10^{-3} - 0.27 - 0.0205] + 700\,[0.025 + (1 - 7.75 \cdot 10^{-3})\,0.27 + 7.75 \cdot 10^{-3} - 0.27]\,]\,3 = 105.6^{\circ}C$$

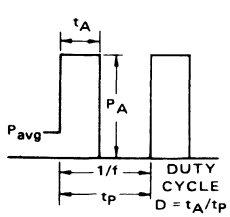


FIGURE A – SIMPLE MODEL

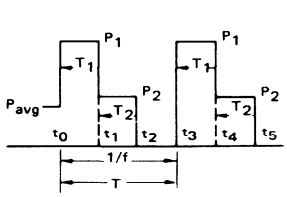


FIGURE B – MORE ACCURATE MODEL

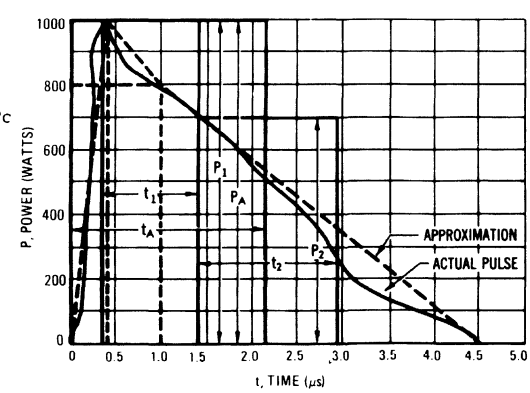
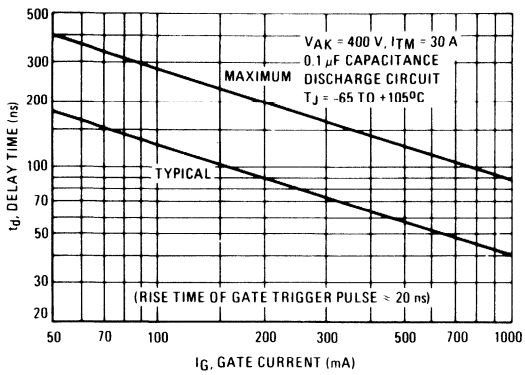


FIGURE C – AN ACTUAL TRANSIENT POWER PULSE

SWITCHING CHARACTERISTICS

FIGURE 9 – DELAY TIME



TRIGGERING CHARACTERISTICS

FIGURE 10 – TYPICAL PULSE TRIGGER CHARGE/CURRENT

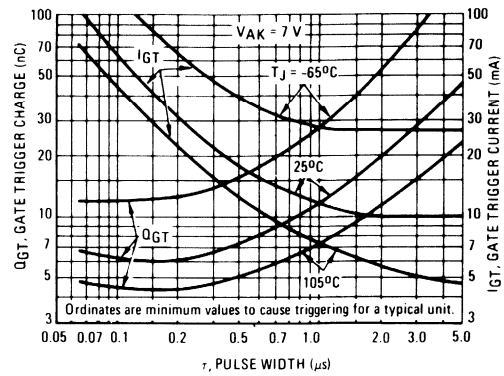


FIGURE 11 – CURRENT RISE TIME

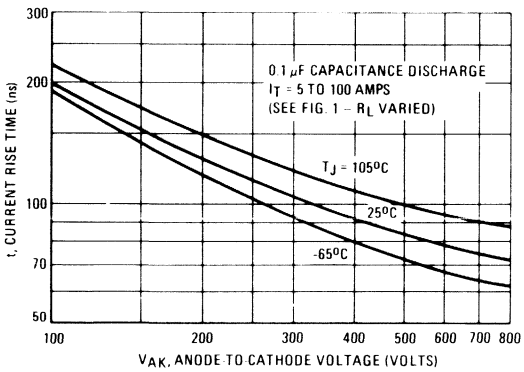


FIGURE 12 – DC GATE TRIGGER VOLTAGE

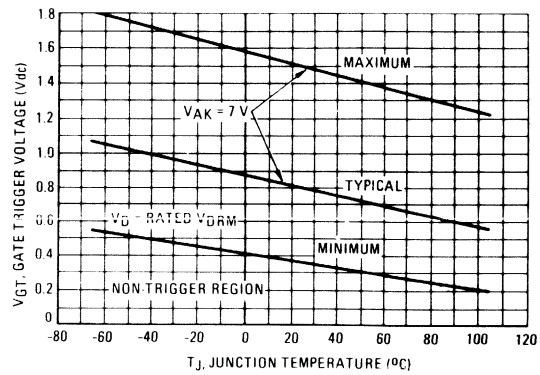


FIGURE 13 – TYPICAL TURN-OFF TIME

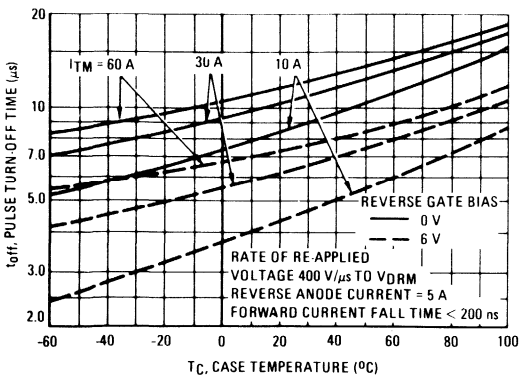


FIGURE 14 – DC GATE TRIGGER CURRENT

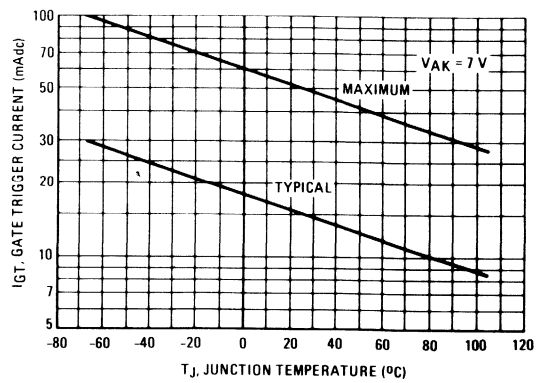


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FIGURE 15 – TYPICAL BLOCKING VOLTAGE DERATING

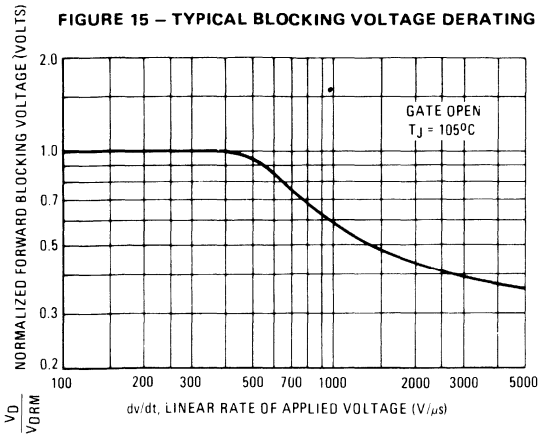


FIGURE 16 – TYPICAL LINEAR dv/dt CAPABILITY

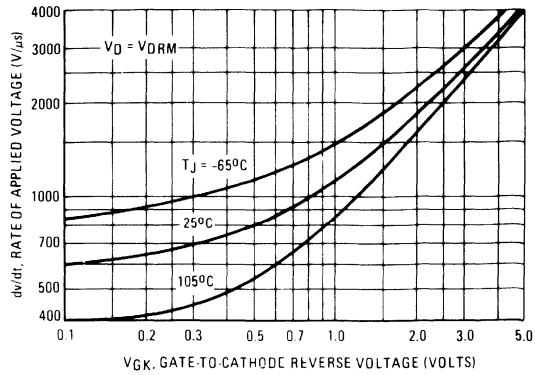


FIGURE 17 – FORWARD BLOCKING CURRENT

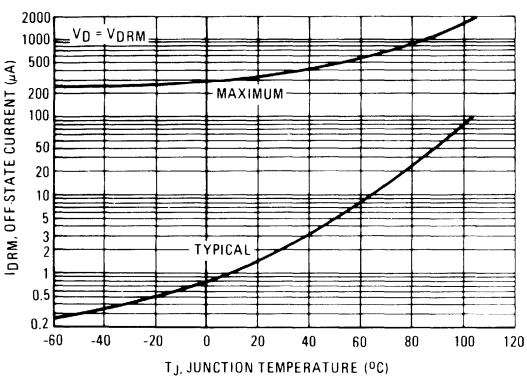


FIGURE 18 – HOLDING CURRENT

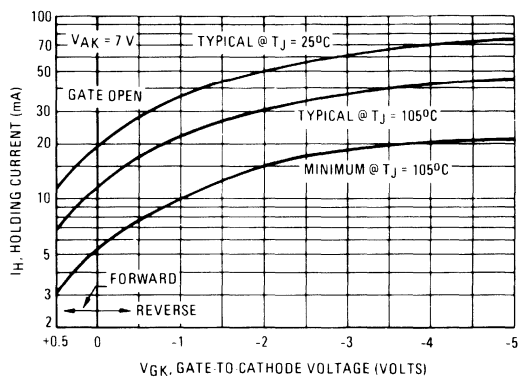


FIGURE 19 – TYPICAL ANODE-TO-CATHODE CAPACITANCE

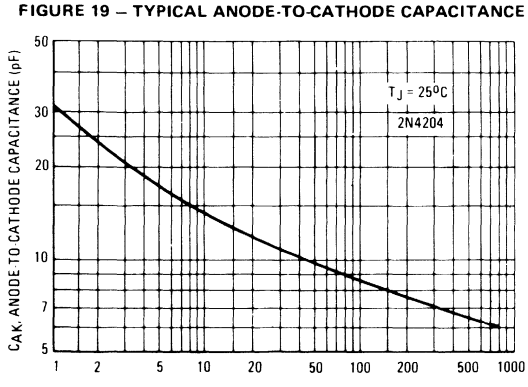
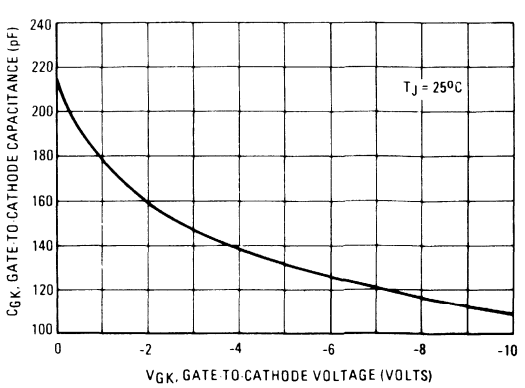


FIGURE 20 – TYPICAL GATE-TO-CATHODE CAPACITANCE



Silicon Controlled Rectifiers

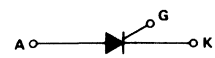
Reverse Blocking Triode Thyristor

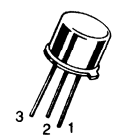
2N4213 thru 2N4219

SCRs
1.6 AMPERES RMS
50 thru 400 VOLTS

. . . all diffused PNPN devices designed for operation in mA/μA signal or detection circuits.

- Low-Level Gate Characteristics — I_{GT} = 100 μA Max @ 25°C
- Low Holding Current — I_{HX} = 3 mA Max @ 25°C
- Anode Common To Case
- Glass-to-Metal Bond for Maximum Hermetic Seal





CASE 79-04
(TO-205AD)
STYLE 3

3

***MAXIMUM RATINGS** (T_J = 125°C unless otherwise noted.)

Characteristic	Symbol	Rating	Unit
Peak Repetitive Forward and Reverse Blocking Voltage, Note 1 2N4213 2N4214 2N4216 2N4219	V_{DRM} or V_{RRM}	 50 100 200 400	Volts
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amps
Peak Surge Current (One Cycle, 60 Hz) No Repetition until Thermal Equilibrium is Restored	I_{TSM}	15	Amps
Peak Gate Power — Forward	P_{GFM}	0.1	Watt
Average Gate Power — Forward	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current — Forward	I_{GFM}	0.1	Amp
Peak Gate Voltage — Forward Reverse	V_{GFM} V_{GRM}	6 6	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Solder Temperature (>1/16" from case, 10 s max)	—	+230	°C

*Indicates JEDEC Registered Values.

Note 1. V_{DRM} and V_{RRM} can be applied for all types on a continuous dc basis without incurring damage.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.), Note 1

Characteristic	Symbol	Min	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	— —	10 200	μA μA
*Forward "On" Voltage (I_{TM} = 1 Adc peak)	V_{TM}	—	1.5	Volts
Gate Trigger Current (Continuous dc), Note 2 (V_D = 7 V, R_L = 100 ohms) (T_C = 25°C) (T_C = −65°C)	I_{GT}	— —	100 300	μAdc
Gate Trigger Voltage (Continuous dc) (V_D = 7 V, R_L = 100 ohms, T_C = 25°C) *(V_D = 7 V, R_L = 100 ohms, T_C = −65°C) *(V_D = Rated V_{DRM}, R_L = 100 ohms, T_J = 125°C)	V_{GT}	— — 0.1	0.8 1 —	Volt
Holding Current (V_D = 7 V) T_C = 25°C *T_C = −65°C	I_{HX}		3 7	mA
Turn-On Time	t_{on}	Circuit dependent, consult manufacturer		
Turn-Off Time	t_{off}			

*Indicates JEDEC Registered Values.

Notes: 1. Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

2. R_{GK} current is not included in measurement.

3

FIGURE 1 – CASE TEMPERATURE vs CURRENT

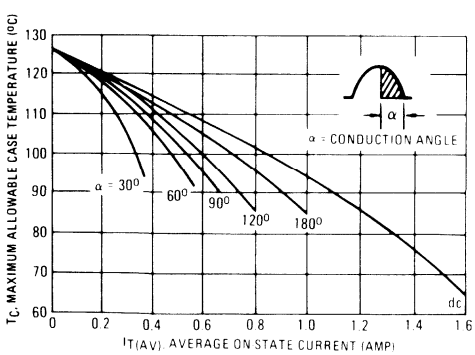
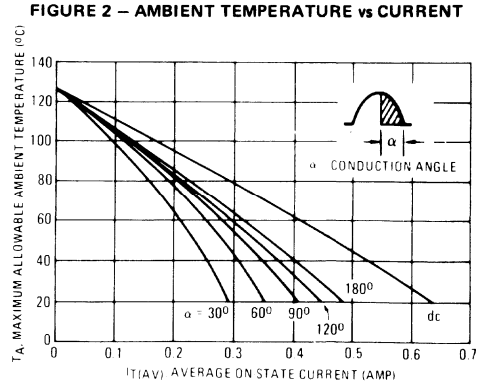


FIGURE 2 – AMBIENT TEMPERATURE vs CURRENT



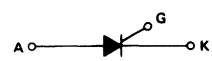
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristors

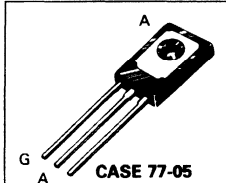
2N4441 thru 2N4444

SCRs
8 AMPERES RMS
50 thru 600 VOLTS

. . . designed for high-volume consumer phase-control applications such as motor speed, temperature, and light controls and for switching applications in ignition and starting systems, voltage regulators, vending machines, and lamp drivers requiring:

- Small, Rugged, Thermopad Construction — for Low Thermal Resistance, High Heat Dissipation, and Durability
- Practical Level Triggering and Holding Characteristics @ 25°C
  I_{GT} = 7 mA (Typ)
  I_H = 6 mA (Typ)
- Low "On" Voltage — V_{TM} = 1 Volt (Typ) @ 5 Amps @ 25°C
- High Surge Current Rating — I_{TSM} = 80 Amps





CASE 77-05
(TO-225AA)
STYLE 2

MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage, Note 1 2N4441 2N4442 2N4443 2N4444	V_{DRM} or V_{RRM}	 50 200 400 600	Volts
*Non-Repetitive Peak Reverse Blocking Voltage (t = 5 ms (max) duration) 2N4441 2N4442 2N4443 2N4444	V_{RSM}	 75 300 500 700	Volts
*RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	8	Amps
Average On-State Current, T_C = 73°C	$I_{T(AV)}$	5.1	Amps
*Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz preceded and followed by rated current and voltage)	I_{TSM}	80	Amps
Circuit Fusing (T_J = −40 to +100°C; t = 1 to 8.3 ms)	I^2t	25	A^2s
*Peak Gate Power	P_{GM}	5	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2	Amps
*Peak Reverse Gate Voltage	V_{RGM}	10	Volts

*Indicates JEDEC Registered Data.

(cont.)

Note 1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.

MAXIMUM RATINGS — continued (T_J = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Operating Junction Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque (6–32 screw), Note 1	—	8	in. lb.

THERMAL CHARACTERISITCS

Characteristic	Symbol	Typ	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	—	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 100°C		—	—	2	mA
Gate Trigger Current (Continuous dc) (V_D = 7 Vdc, R_L = 100 Ohms) T_C = 25°C	I_{GT}	—	7	30	mA
*T_C = −40°C				60	
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 100 Ohms) T_C = 25°C	V_{GT}	—	0.75	1.5	Volts
(V_D = 7 Vdc, R_L = 100 Ohms) T_C = −40°C		—	—	2.5	
(V_D = Rated V_{DRM}, R_L = 100 Ohms) T_J = 100°C		0.2	—	—	
Peak On-State Voltage (Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%) (I_{TM} = 5 A peak)	V_{TM}	—	1	1.5	Volts
*(I_{TM} = 15.7 A peak)		—	—	2	
Holding Current (V_D = 7 Vdc, gate open) T_C = 25°C	I_H	—	6	40	mA
*T_C = −40°C		—	—	70	
Gate Controlled Turn-On Time (I_{TM} = 5 A, I_{GT} = 20 mA, V_D = Rated V_{DRM})	t_{gt}	—	1	—	μs
Circuit Commutated Turn-Off Time (I_{TM} = 5 A, I_R = 5 A)	t_q	—	15	—	μs
(I_{TM} = 5 A, I_R = 5 A, T_J = 100°C)		—	20	—	
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_J = 100°C, Gate Open)	dv/dt	—	50	—	V/μs

*Indicates JEDEC Registered Data.

Note 1. Torque rating applies with use of torque washer (Shakeproof WD19522 #6 or equivalent). Mounting torque in excess of 8 in. lbs. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common.

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C.

FIGURE 1 – ON-STATE CHARACTERISTICS

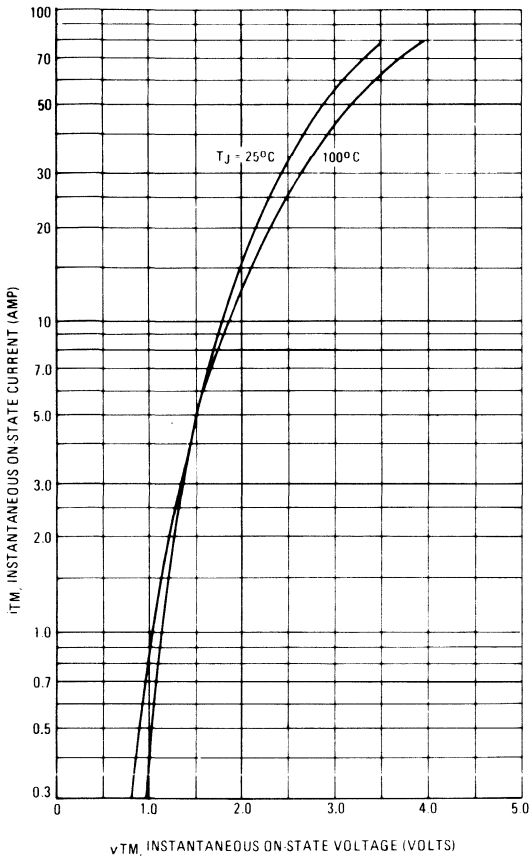


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

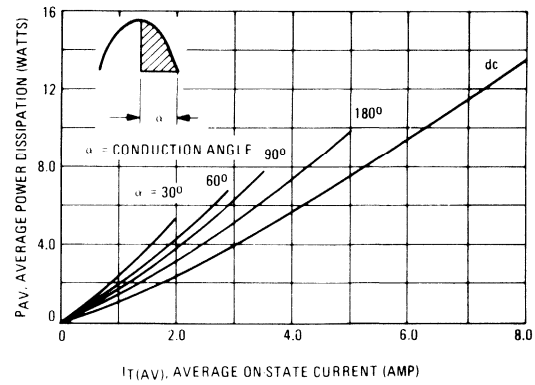


FIGURE 3 – AVERAGE CURRENT DERATING

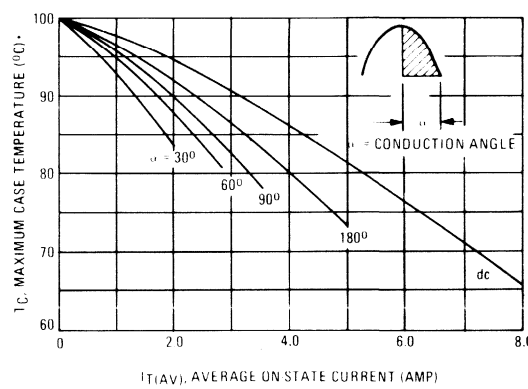


FIGURE 4 – THERMAL RESPONSE

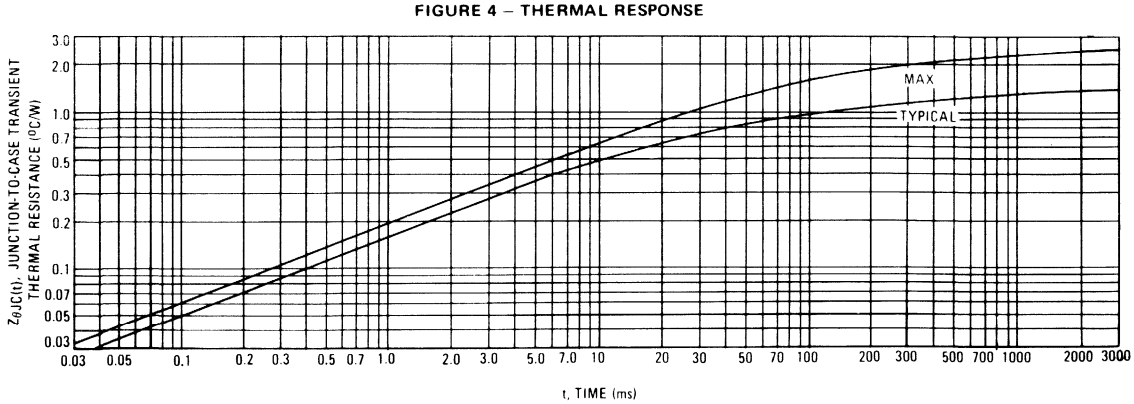


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FIGURE 5 – MAXIMUM NON-REPETITIVE SURGE CURRENT

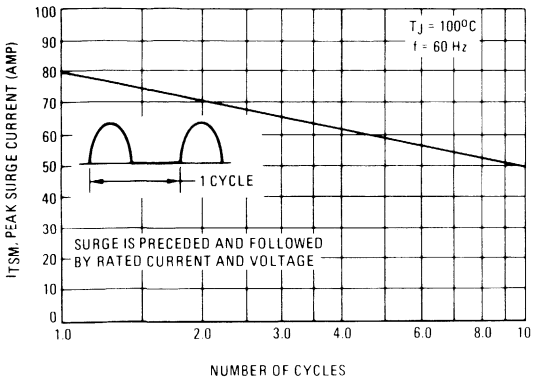


FIGURE 6 – TYPICAL HOLDING CURRENT

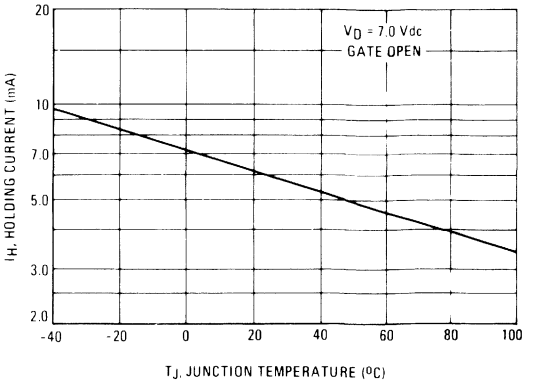


FIGURE 7 – TYPICAL GATE TRIGGER CURRENT

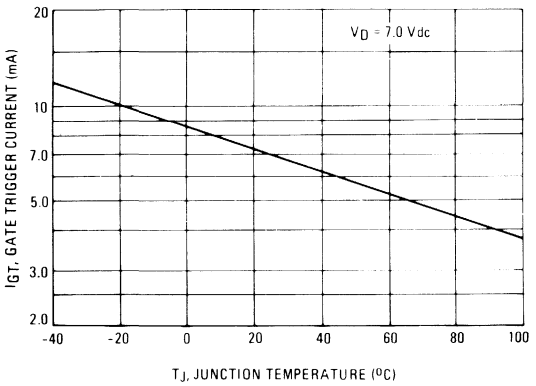
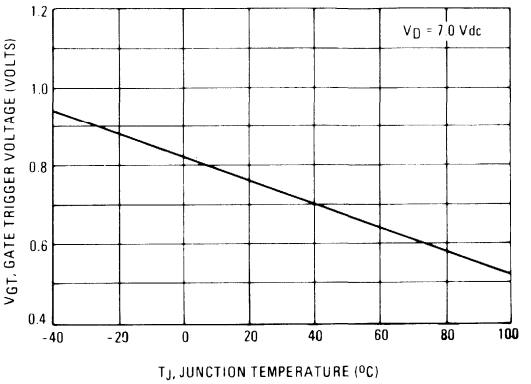


FIGURE 8 – TYPICAL GATE TRIGGER VOLTAGE



3

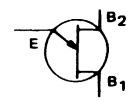
PN Unijunction Transistors
Silicon Unijunction Transistor

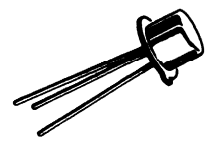
2N4851 thru 2N4853

PN UJTs

. . . designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits.

- Low Peak-Point Current — I_P = 0.4 μA Max
- Low Emitter Reverse Current — I_{EO} = 50 nA Max
- Fast Switching





CASE 22A-01
STYLE 1

***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Power Dissipation, Note 1	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current, Note 2	i_e	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage, Note 3	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

*Indicates JEDEC Registered Data.
Notes: 1. Derate 3 mW/°C increase in ambient temperature.
2. Duty cycle ≤ 1%, PRR = (see Figure 6).
3. Based upon power dissipation at T_A = 25°C.

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Rating		Fig. No.	Symbol	Min	Typ	Max	Unit
*Intrinsic Standoff Ratio, Note 1 (V_{B2B1} = 10 V)	2N4851 2N4852, 2N4853	4, 8	η	0.56 0.70	— —	0.75 0.85	—
*Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)		11, 12	r_{BB}	4.7	—	9.1	k ohms
*Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = −65 to +125°C)		12	α_{BB}	0.2	—	0.8	%/°C
Emitter Saturation Voltage, Note 2 (V_{B2B1} = 10 V, I_E = 50 mA)			$V_{EB1(sat)}$	—	2.5	—	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)			$I_{B2(mod)}$	—	15	—	mA
*Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	2N4851, 2N4852 2N4853	7	I_{EB2O}	— —	— —	0.1 0.05	μA
*Peak-Point Emitter Current (V_{B2B1} = 25 V)	2N4851, 2N4852 2N4853	9, 10	I_P	— —	— —	2 0.4	μA
*Valley-Point Current, Note 2 (V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4851 2N4852 2N4853	13, 14	I_V	2 4 6	— — —	— — —	mA
*Base-One Peak Pulse Voltage	2N4851 2N4852 2N4853	3, 17	V_{OB1}	3 5 6	— — —	— — —	Volts
*Maximum Frequency of Oscillation		5	$f_{(max)}$	—	1.25	—	MHz

*Indicates JEDEC Registered Data.

Notes: 1. η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.

2. Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2% to avoid internal heating, which may result in erroneous readings.

3

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

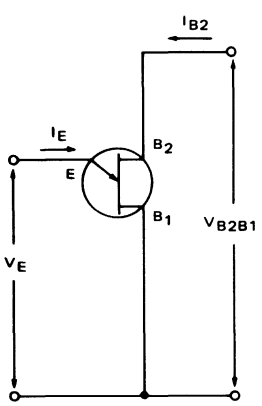


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES

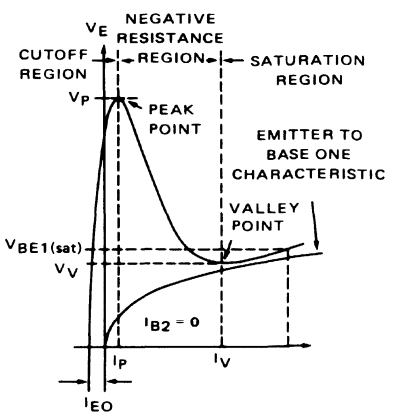


FIGURE 3 – V_{OB1} TEST CIRCUIT

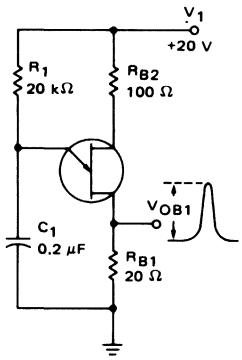


FIGURE 4 – η TEST CIRCUIT

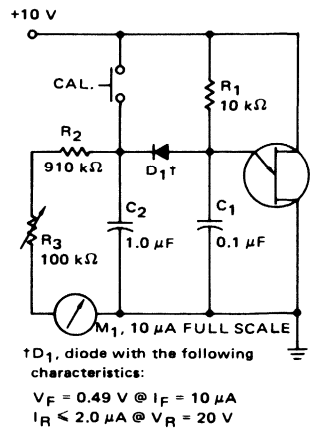


FIGURE 5 – $f_{(max)}$ TEST CIRCUIT

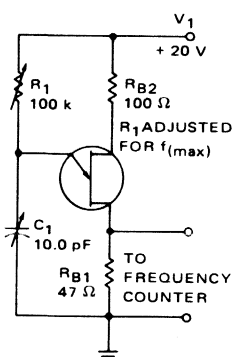
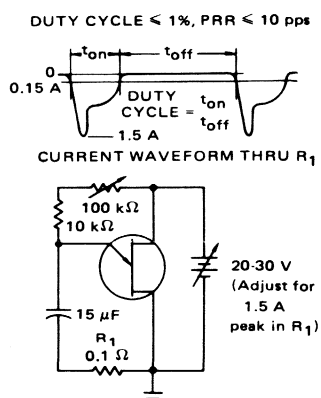


FIGURE 6 – PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS

FIGURE 7 – EMITTER REVERSE CURRENT

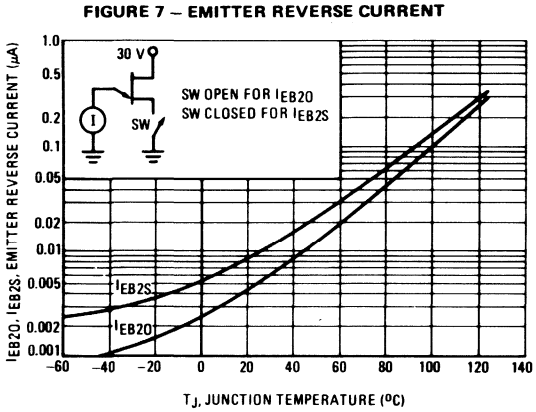
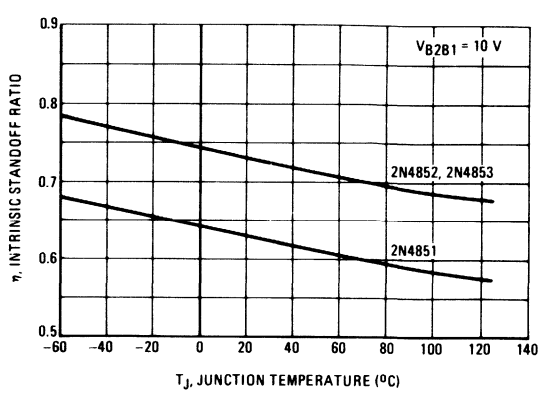


FIGURE 8 – INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 9 – EFFECT OF VOLTAGE

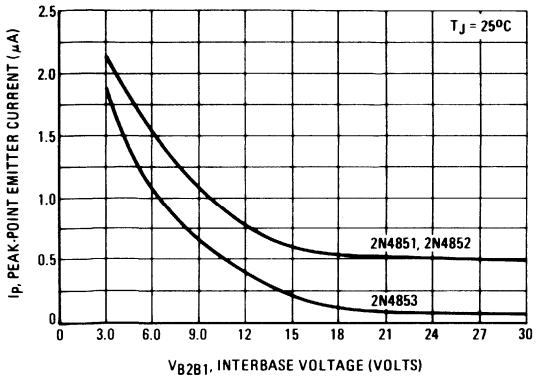
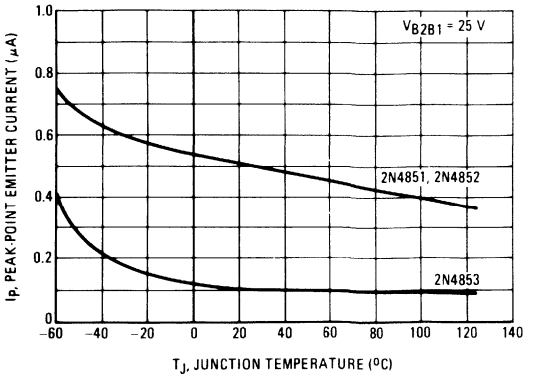


FIGURE 10 – EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 11 – EFFECT OF VOLTAGE

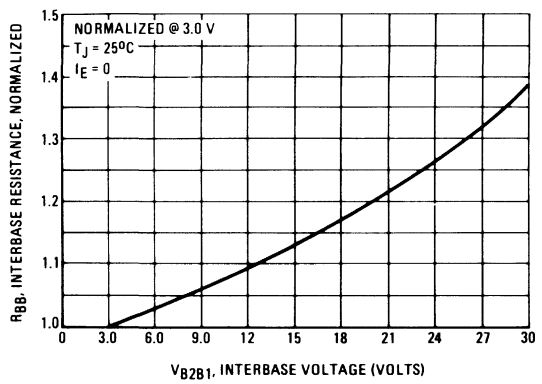
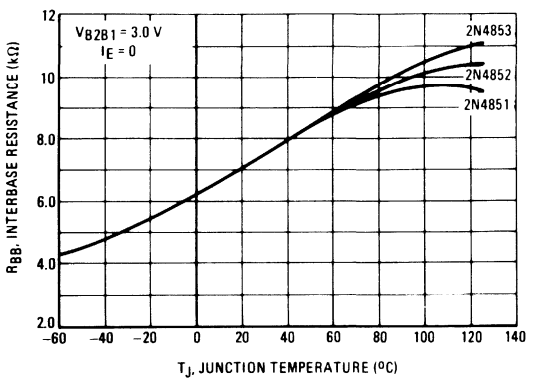


FIGURE 12 – EFFECT OF TEMPERATURE



TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 13 – EFFECT OF VOLTAGE

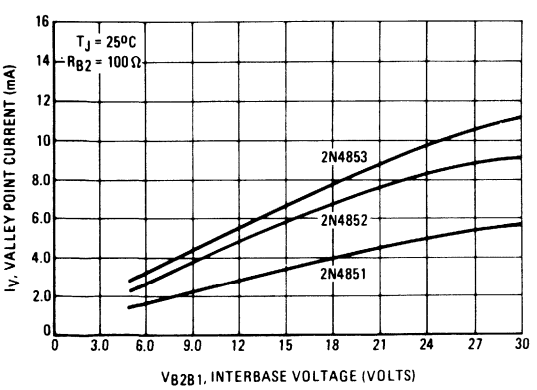
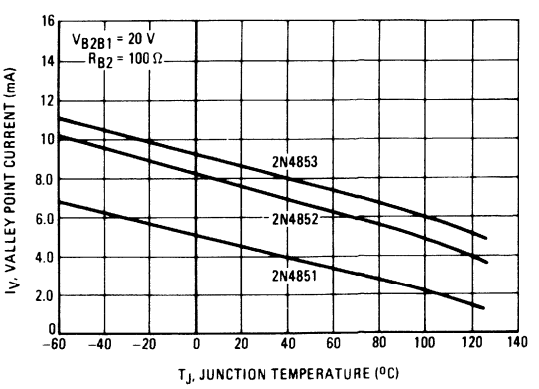


FIGURE 14 – EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 15 – EFFECT OF VOLTAGE

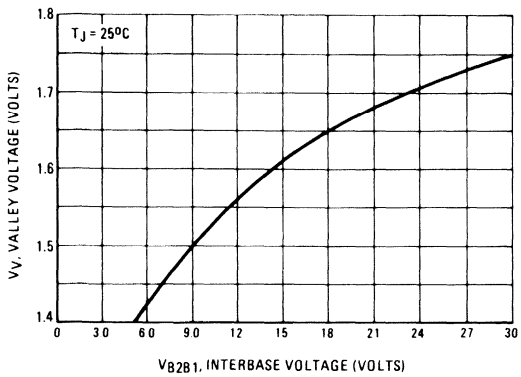


FIGURE 16 – EFFECT OF TEMPERATURE

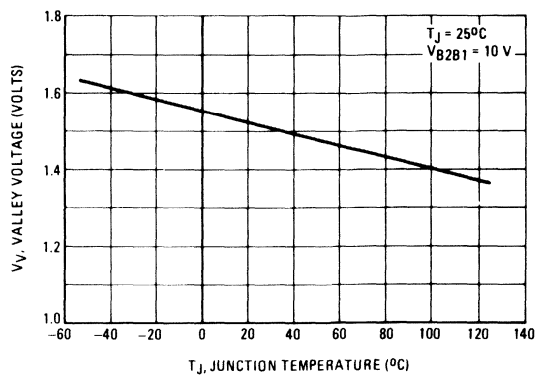
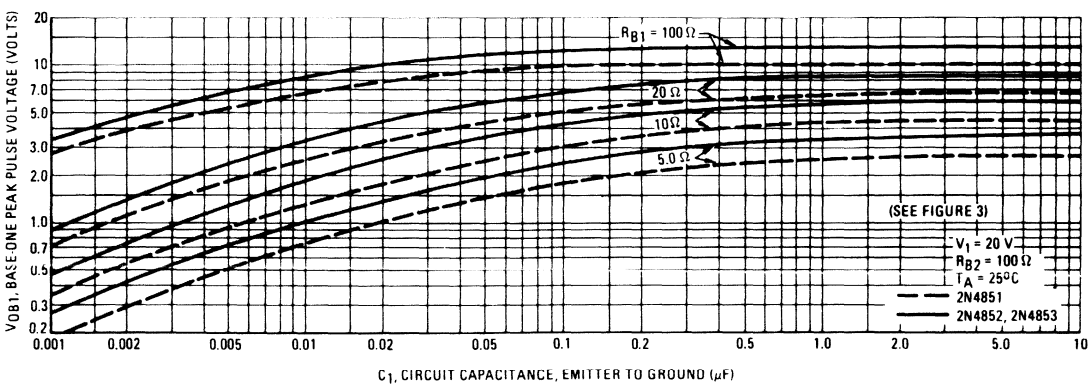


FIGURE 17 – OUTPUT VOLTAGE



3

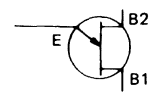
PN Unijunction Transistors
Silicon Unijunction Transistors

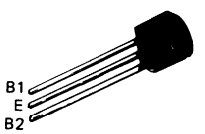
2N4870
2N4871

PN UJTs

. . . designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits. These devices feature:

- Low Peak Point Current — 1 μA Typical
- Low Emitter Reverse Current — 5 nA Typical
- Passivated Surface for Reliability and Uniformity
- One-Piece Injection-Molded Unibloc‡ Plastic Package for Economy and Reliability
- High η for greater bandwidth





CASE 29-04
STYLE 9

3

MAXIMUM RATINGS (T_A = 25° unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Power Dissipation, Note 1	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current, Note 2	i_e	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage, Note 3	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Notes: 1. Derate 3 mW/°C increase in ambient temperature.
2. Duty cycle ≤ 1%, PRR = 10 PPS (see Figure 5).
3. Based upon power dissipation at T_A = 25°C.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio, Note 1 (V_{B2B1} = 10 V)	2N4870 2N4871	4, 7	η	0.56 0.70	— —	0.75 0.85	—
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)		10, 11	R_{BB}	4	6	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = −65 to +125°C)		11	αR_{BB}	0.10	—	0.90	%/°C
Emitter Saturation Voltage, Note 2 (V_{B2B1} = 10 V, I_E = 50 mA)			$V_{EB1(sat)}$	—	2.5	—	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)			$I_{B2(mod)}$	—	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		6	I_{EB2O}	—	0.005	1	μA
Peak-Point Emitter Current (V_{B2B1} = 25 V)		8, 9	I_P	—	1	5	μA
Valley-Point Current, Note 2 (V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4870 2N4871	12, 13	I_V	2 4	5 7	— —	mA
Base-One Peak Pulse Voltage	2N4870 2N4871	3, 16	V_{OB1}	3 5	6 8	— —	Volts

Notes: 1. η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_R. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.

2. Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2% to avoid internal heating, which may result in erroneous readings.

3

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

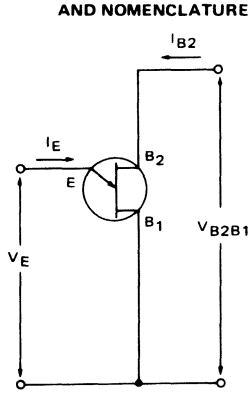


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES

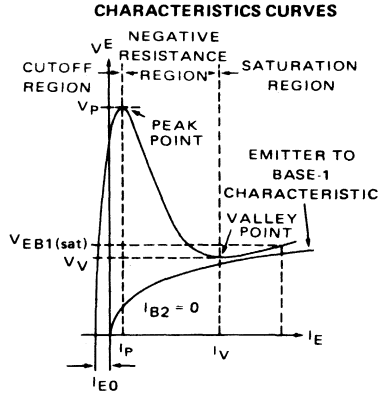


FIGURE 3 – V_{OB1} TEST CIRCUIT

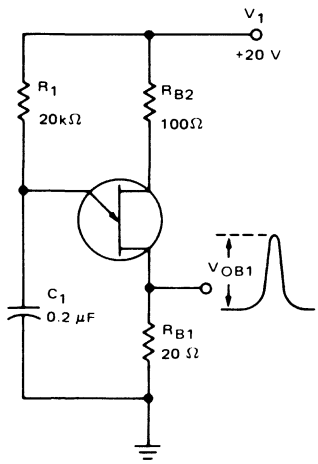


FIGURE 4 – η TEST CIRCUIT

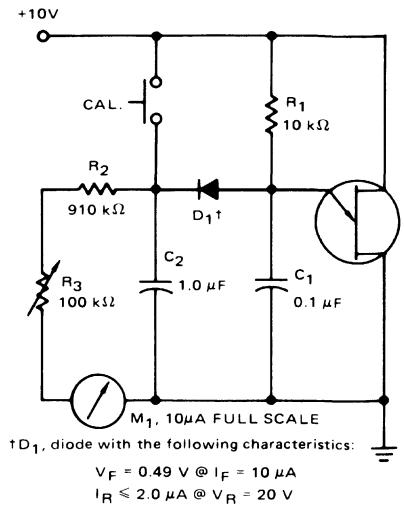
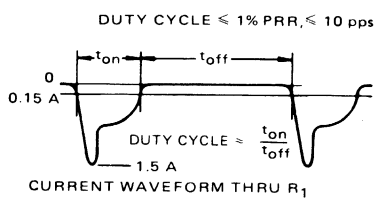
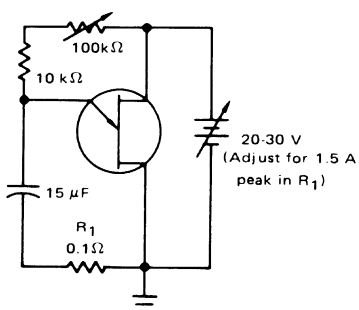


FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM





TYPICAL CHARACTERISTICS

FIGURE 6 – EMITTER REVERSE CURRENT

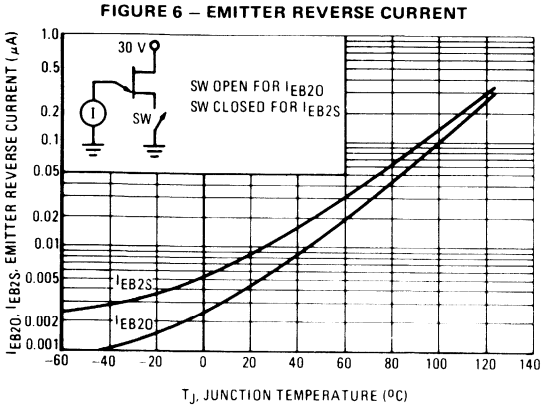
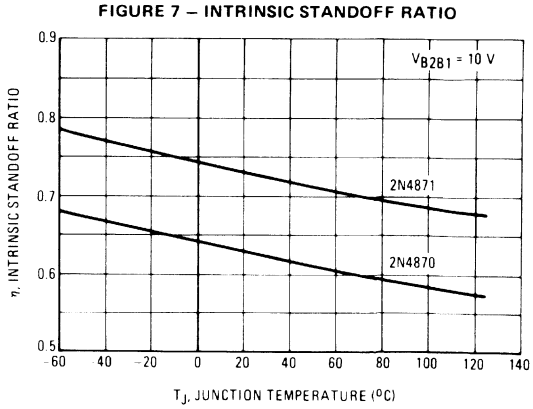


FIGURE 7 – INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 8 – EFFECT OF VOLTAGE

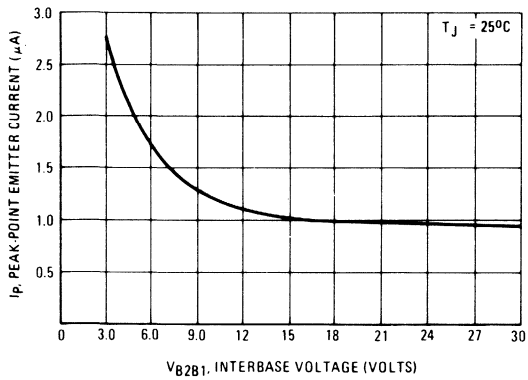
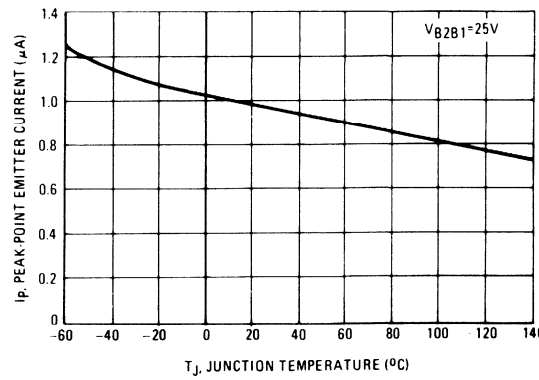


FIGURE 9 – EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 10 – EFFECT OF VOLTAGE

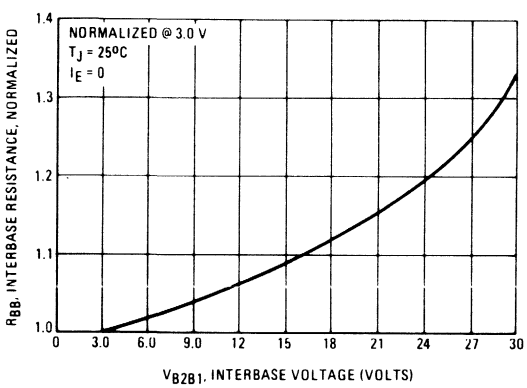
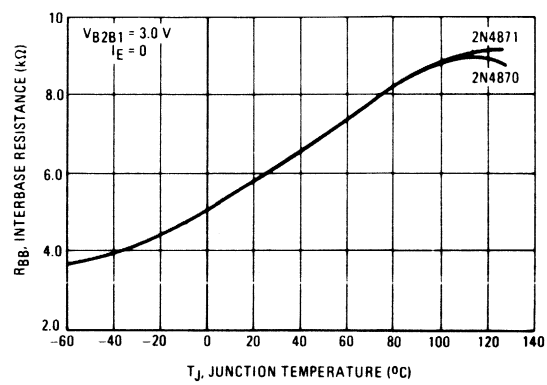


FIGURE 11 – EFFECT OF TEMPERATURE



3

TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 12 – EFFECT OF VOLTAGE

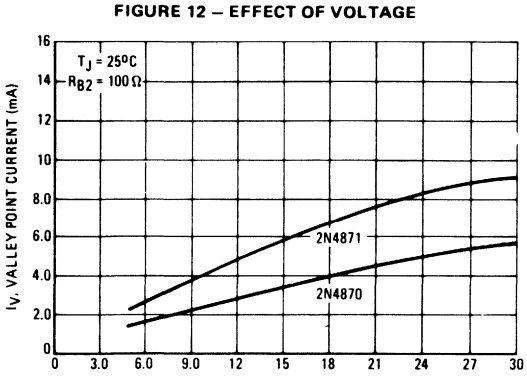
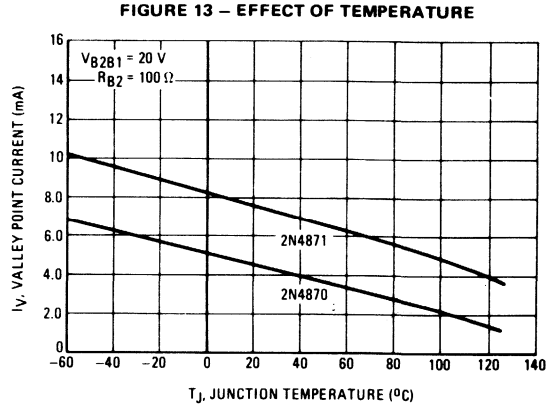


FIGURE 13 – EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 14 – EFFECT OF VOLTAGE

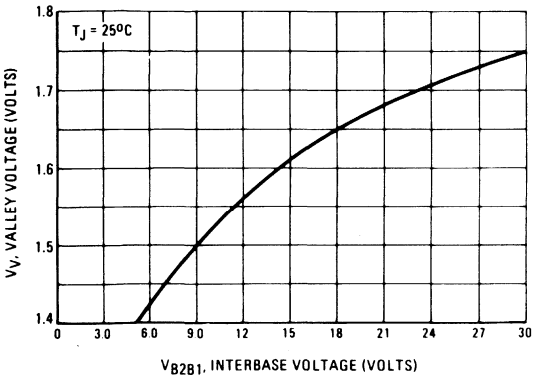


FIGURE 15 – EFFECT OF TEMPERATURE

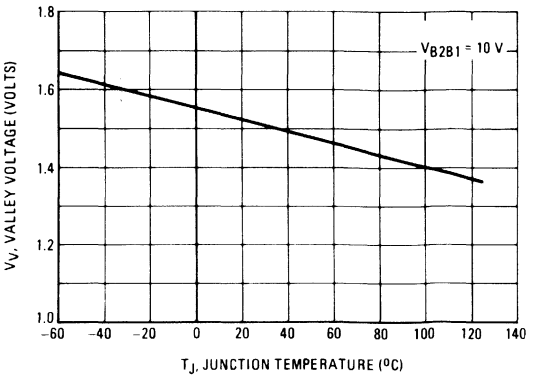
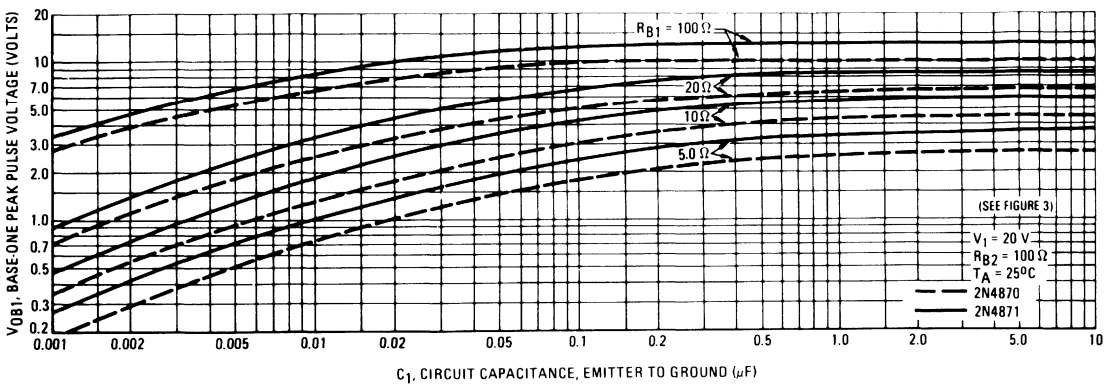


FIGURE 16 – OUTPUT VOLTAGE



3

PN Unijunction Transistors

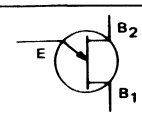
Silicon PN Unijunction Transistors

2N4948
2N4949

PN UJTs

. . . designed for military and industrial use in pulse, timing, triggering, sensing, and oscillator circuits. The annular process provides low leakage current, fast switching and low peak-point currents as well as outstanding reliability and uniformity. Recommended usage includes:

- Silicon Controlled Rectifier Triggering Circuits — 2N4948
- Long-time Delay Circuits — 2N4949



CASE 22A-01
STYLE 1

3

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Power Dissipation, Note 1	P_D	360	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current, Note 2	i_e	1	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Storage Temperature Range	T_{stg}	−65 to +200	°C

Notes: 1. Derate 2.4 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry. Interbase voltage (V_{B2B1}) limited by power dissipation, $V_{B2B1} = \sqrt{R_{BB} \cdot P_D}$.

2. Capacitance discharge current must fall to 0.37 Amp within 3 ms and PRR ≤ 10 PPS.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V), Note 1	2N4948 2N4949	η	0.55 0.74	— —	0.82 0.86	—
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)	2N4948, 2N4949	R_{BB}	4	7	12.0	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = −65°C to +100°C)		αR_{BB}	0.1	—	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA), Note 2		$V_{EB1(sat)}$	—	2.5	3	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	12	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0) (V_{B2E} = 30 V, I_{B1} = 0, T_A = 125°C)		I_{EB2O}	— —	5 —	10 1	nA μA
Peak Point Emitter Current (V_{B2B1} = 25 V)	2N4948 2N4949	I_P	— —	0.6 0.6	2 1	μA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms), Note 2	2N4948, 2N4949	I_V	2	4	—	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N4949 2N4948	V_{OB1}	3 6	5 8	— —	Volts
Maximum Oscillation Frequency (Figure 4)		$f_{(max)}$	—	1.25	—	MHz

Notes:

1. Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
V_F = Emitter to Base-One Junction Diode Drop (≈ 0.45 V @ 10 μA)

2. Use pulse techniques: PW ≈ 300 μs duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.
3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

3

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

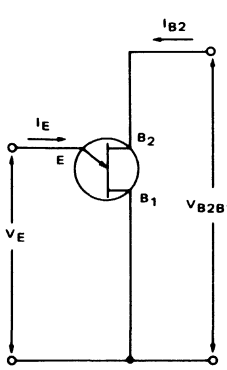


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES

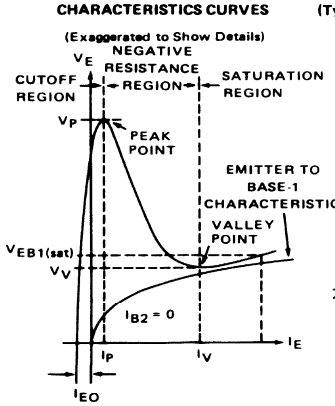


FIGURE 3 – V_{OB1} TEST CIRCUIT (Typical Relaxation Oscillator)

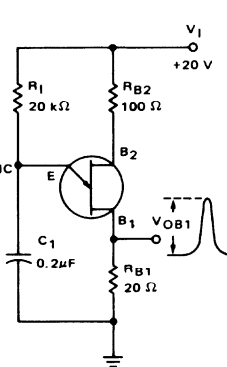
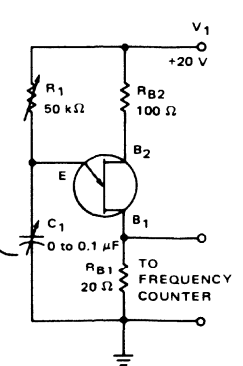


FIGURE 4 – F(max) MAXIMUM FREQUENCY TEST CIRCUIT



Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristor

2N5060 thru 2N5064

SCRs
0.8 AMPERES RMS
30 thru 200 VOLTS

. . . Annular PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current — 200 μA Maximum
- Low Reverse and Forward Blocking Current — 50 μA Maximum, T_C = 125°C
- Low Holding Current — 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form

CASE 29-04
(TO-226AA)
STYLE 10

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
*Peak Repetitive Reverse Blocking Voltage, Note 1 (R_{GK} = 1000 ohms, T_C = +125°C) 2N5060	V_{DRM} or V_{RRM}	30	Volts
2N5061		60	
2N5062		100	
2N5063		150	
2N5064		200	
On-State Current RMS (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
*Average On-State Current (T_C = 67°C)	$I_{T(AV)}$	0.51	Amp
(T_C = 102°C)		0.255	
*Peak Non-Repetitive Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amps
Circuit Fusing Considerations, T_A = 25°C (t = 1 to 8.3 ms)	I^2t	0.15	A^2s
*Peak Gate Power, T_A = 25°C	P_{GM}	0.1	Watt
*Average Gate Power, T_A = 25°C	$P_{G(AV)}$	0.01	Watt
*Peak Forward Gate Current, T_A = 25°C (300 μs, 120 PPS)	I_{FGM}	1	Amp
*Peak Reverse Gate Voltage	V_{RGM}	5	Volts

*Indicates JEDEC Registered Data.

(cont.)

Note 1. Ratings apply for zero or negative gate voltage. Device ratings exclude having a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
*Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−65 to +125	°C
*Storage Temperature Range	T_{stg}	−65 to +150	°C
*Lead Solder Temperature (Lead Length ≥ 1/16" from case, 10 s Max)	—	+230*	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case, Note 1	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.), Note 2

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage, Note 3 (T_C = 125°C, R_{GK} = 1000 Ohms)		V_{DRM}				Volts
	2N5060		30	—	—	
	2N5061		60	—	—	
	2N5062		100	—	—	
	2N5063		150	—	—	
	2N5064		200	—	—	
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, R_{GK} = 1000 Ohms)	T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
	T_C = 125°C		—	—	50	μA
*Forward "On" Voltage, Note 4 (I_{TM} = 1.2 A peak @ T_A = 25°C)		V_{TM}	—	—	1.7	Volts
Gate Trigger Current (Continuous dc), Note 5 *(Anode Voltage = 7 Vdc, R_L = 100 Ohms, R_{GK} = 1000 Ohms)	T_C = 25°C	I_{GT}	—	—	200	μA
	T_C = −65°C		—	—	350	
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	—		0.8	Volts
*(Anode Voltage = 7 Vdc, R_L = 100 Ohms)	T_C = −65°C		—		1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C	V_{GD}	0.1		—	
Holding Current	T_C = 25°C	I_H	—	—	5	mA
*(Anode Voltage = 7 Vdc, initiating current = 20 mA)	T_C = −65°C		—	—	10	
Turn-On Time						μs
Delay Time		t_d	—	3	—	
Rise Time		t_r	—	0.2	—	
(I_{GT} = 1 mA, R_{GK} = 1 Ohm, V_D = Rated V_{DRM}, Forward Current = 1 A, di/dt = 6 A/μs						
Turn-Off Time (Forward Current = 1 A pulse, Pulse Width = 50 μs, 0.1% Duty Cycle, di/dt = 6 A/μs, dv/dt = 20 V/μs, I_{GT} = 1 mA, R_{GK} = 1 k Ohm)	2N5060, 2N5061	tq	—	10	—	μs
	2N5062, 5063, 5064		—	30	—	
Forward Voltage Application Rate (Rated V_{DRM}, R_{GK} = 1 k, Exponential)		dv/dt	—	30	—	V/μs

*Indicates JEDEC Registered Data.

Notes: 1. This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.

2. For electrical characteristics for Gate-to-cathode resistance other than 1000 ohms see Motorola Bulletin EB-30.

3. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.

4. Forward current applied for 1 ms maximum duration, duty cycle ≤ 1%.

5. R_{GK} current is not included in measurement.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

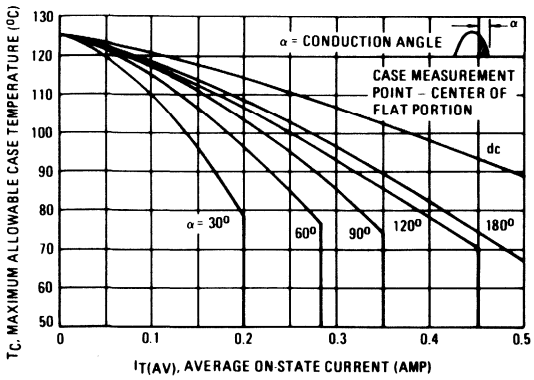


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE

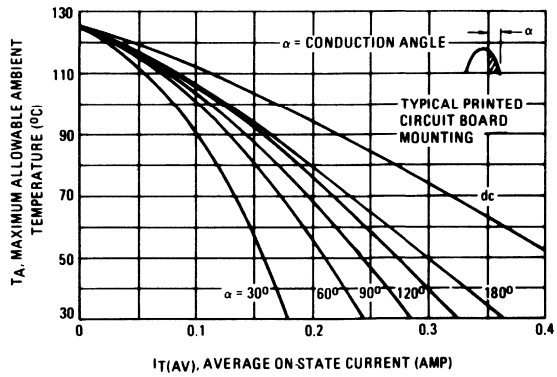


FIGURE 3 – TYPICAL FORWARD VOLTAGE

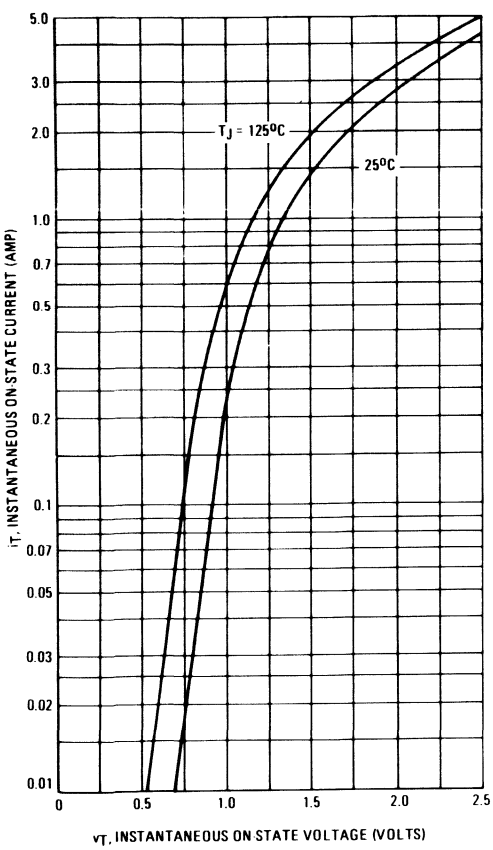


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

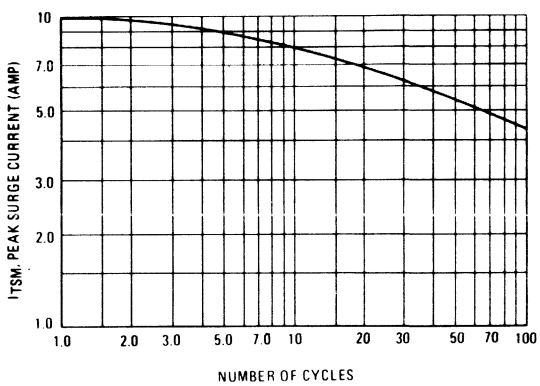


FIGURE 5 – POWER DISSIPATION

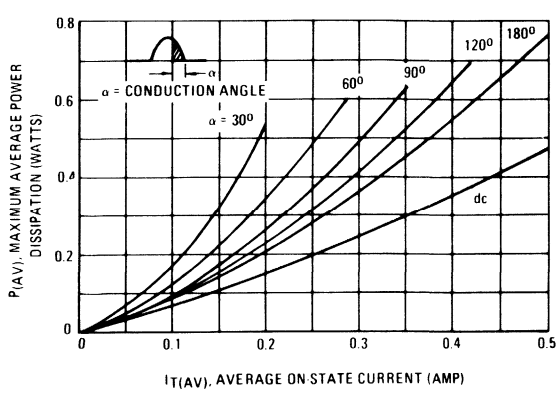
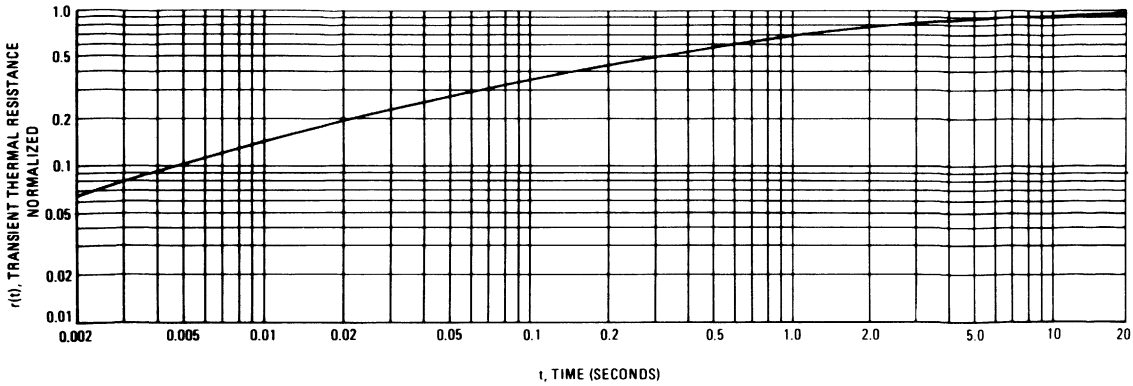


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 – GATE TRIGGER VOLTAGE

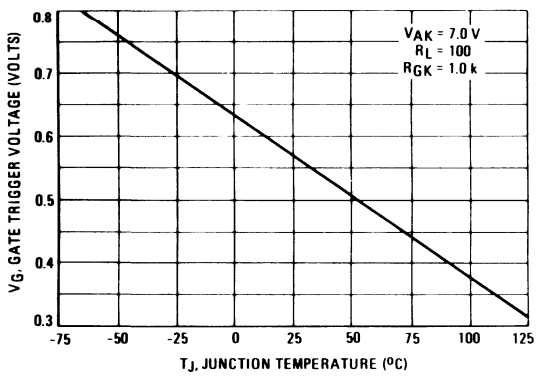


FIGURE 8 – GATE TRIGGER CURRENT

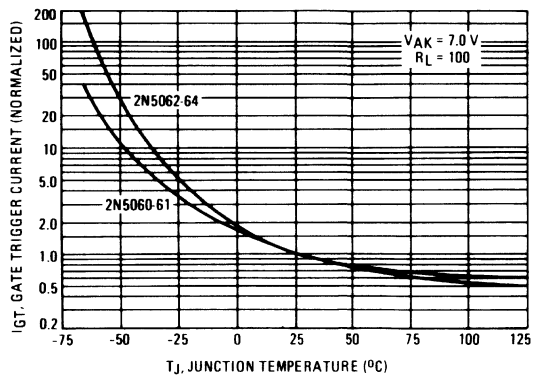


FIGURE 9 – HOLDING CURRENT

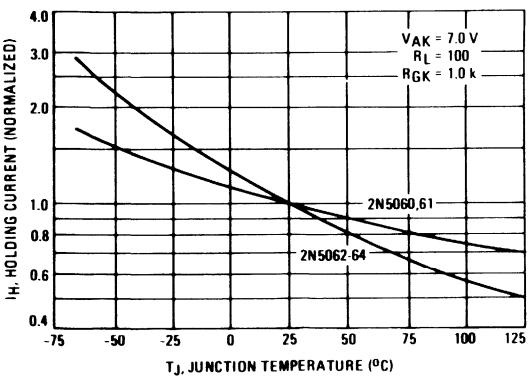
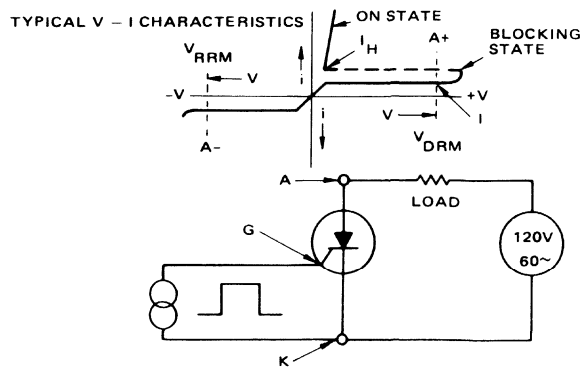


FIGURE 10 – CHARACTERISTICS AND SYMBOLS



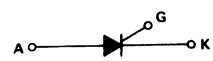
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristor

2N5164 thru 2N5171

SCRs
20 AMPERES RMS
50 thru 600 VOLTS

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Supplied in Either Pressfit or Stud Package
- High Surge Current Rating — I_{TSM} = 240 Amps
- Low On-State Voltage — 1.2 V (Typ) @ I_{TM} = 20 Amps
- Practical Level Triggering and Holding Characteristics — 40 mA (Max) and 50 mA (Max) @ T_C = 25°C



CASE 263-04
STYLE 1
2N5168 thru 2N5171

CASE 310-02
STYLE 1
2N5164 thru 2N5167

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Forward and *Repetitive Reverse Blocking Voltage, Notes 1 and 2 2N5164, 2N5168 2N5165, 2N5169 2N5166, 2N5170 2N5167, 2N5171	V_{DRM} or V_{RRM}	 50 200 400 600	Volts
*Non-Repetitive Peak Reverse Blocking Voltage 2N5164, 2N5168 2N5165, 2N5169 2N5166, 2N5170 2N5167, 2N5171	V_{RSM}	 75 300 500 700	Volts
On-State Current RMS	$I_{T(RMS)}$	20	Amps
Average On-State Current (T_C = 67°C)	$I_{T(AV)}$	13	Amps
Circuit Fusing (T_J = −40 to +100°C, t ≤ 8.3 ms)	I^2t	235	A^2s
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, T_J = −40 to +100°C) Preceded and followed by rated current and voltage	I_{TSM}	240	Amps
*Peak Gate Power (Maximum Pulse Width = 10 μs)	P_{GM}	5	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current (Maximum Pulse Width = 10 μs)	I_{GM}	2	Amps
Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Stud Torque 2N5168–2N5171		30	in. lb.

*Indicates JEDEC registered data.

Notes: 1. V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.

2. Devices should not be operated with a positive bias applied to the gate concurrent with a negative potential applied to the anode.

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$			°C/W
2N5164, 65, 66, 67		1	1.5	
2N5168, 69, 70, 71		1.1	1.6	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	10	μA
T_J = 100°C		—	5	mA
Gate Trigger Current (Continuous dc), Note 1	I_{GT}			mA
(V_D = 7 Vdc, R_L = 100 Ω)		—	40	
*(V_D = 7 Vdc, R_L = 100 Ω, T_C = −40°C)		—	75	
Gate Trigger Voltage (Continuous dc)	V_{GT}			Volts
(V_D = 7 Vdc, gate open)		—	1.5	
*(V_D = 7 Vdc, R_L = 100 Ω, T_C = −40°C)		—	2.5	
*(V_D = Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)		0.2	—	
Peak On-State Voltage (Pulse Width = 1 ms max, duty cycle ≤ 1%)	V_{TM}			Volts
(I_{TM} = 20 A)		—	1.5	
*(I_{TM} = 41 A)		8	1.7	
Holding Current	I_H			mA
(V_D = 7 Vdc, gate open)		—	50	
*(V_D = 7 Vdc, gate open, T_C = −40°C)		—	90	
		Typical		
Gate Controlled Turn-On Time (t_d + t_r) (I_{TM} = 20 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	1		μs
Circuit Commutated Turn-Off Time	t_q			μs
(I_{TM} = 10 A, I_R = 10 A)		20		
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C) (V_D = V_{DRM} = rated voltage) (dv/dt = 30 V/μs)		30		
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Wave Form, Gate open, T_J = 100°C)	dv/dt	50		V/μs

*Indicates JEDEC registered data.

Note 1. Devices should not be operated with a positive bias applied to the gate concurrent with a negative potential applied to the anode.

3

EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – GATE TRIGGER CURRENT

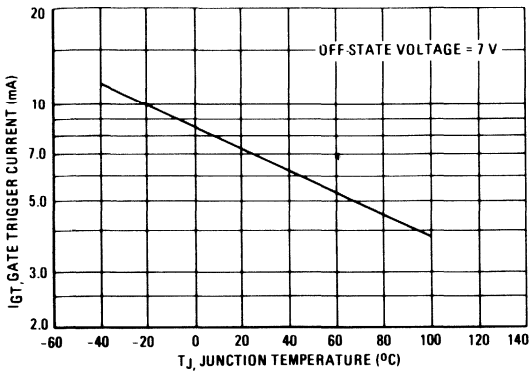
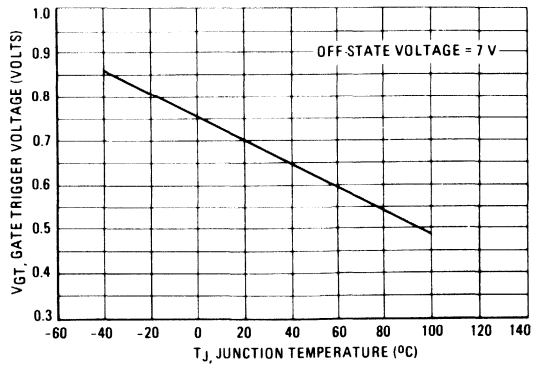


FIGURE 2 – GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-REPETITIVE SURGE CURRENT

FIGURE 3 – 60 Hz SURGES

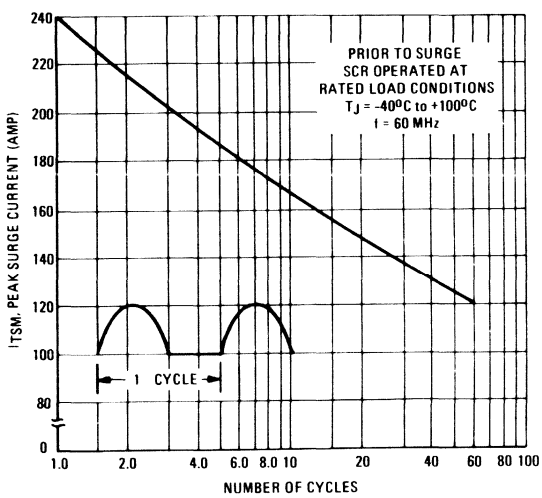


FIGURE 4 – SUB-CYCLE SURGES

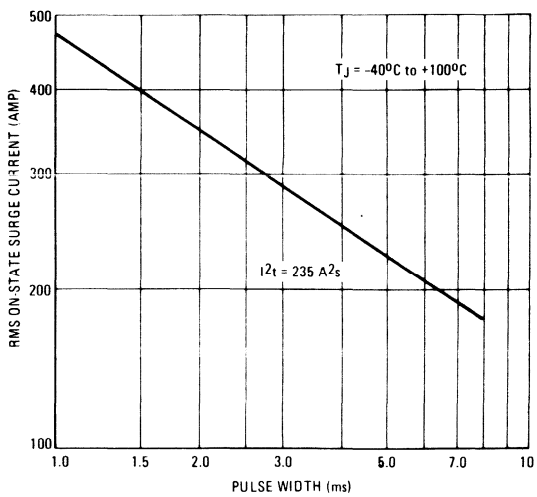


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FIGURE 5 – GATE TRIGGER CHARACTERISTICS

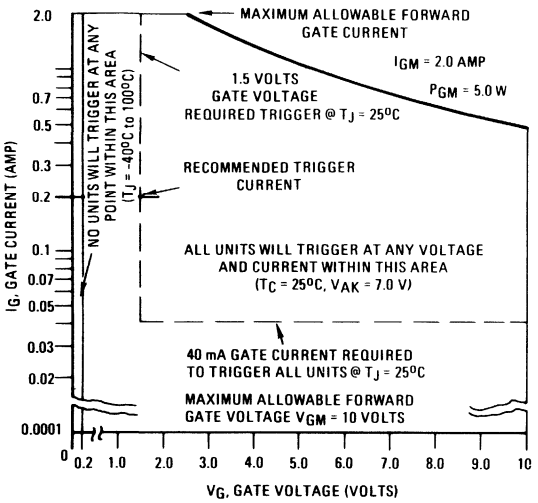
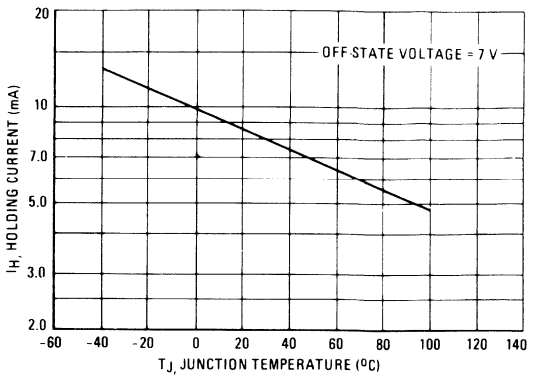


FIGURE 6 – EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT



DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

3

FIGURE 7 – AVERAGE CURRENT DERATING

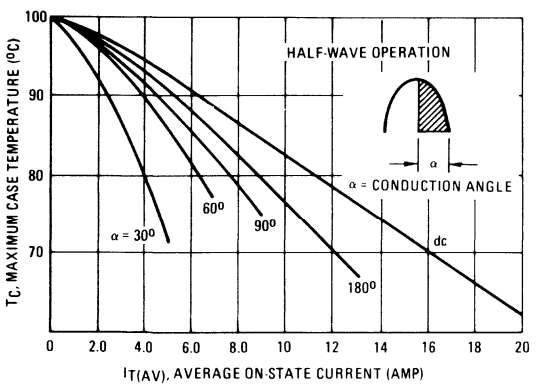


FIGURE 8 – ON-STATE POWER DISSIPATION

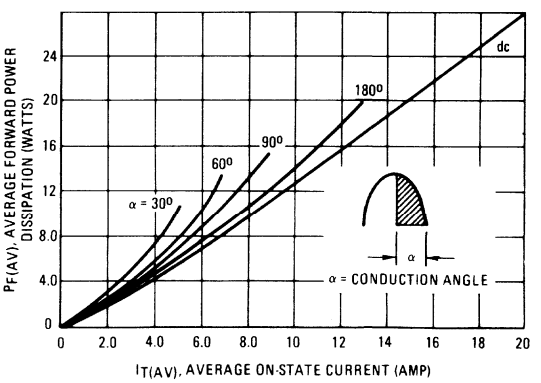


FIGURE 9 – ON-STATE CHARACTERISTICS

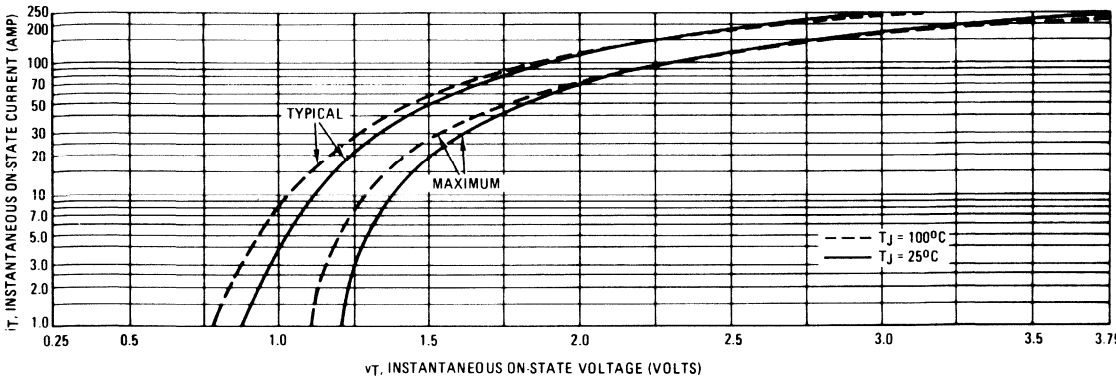


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

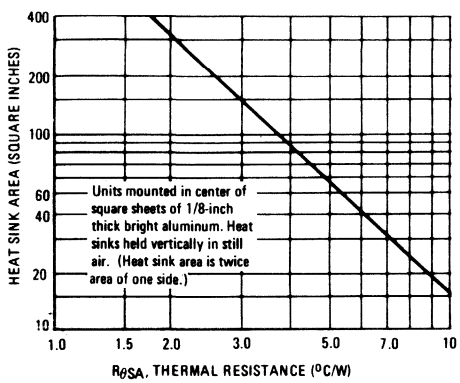
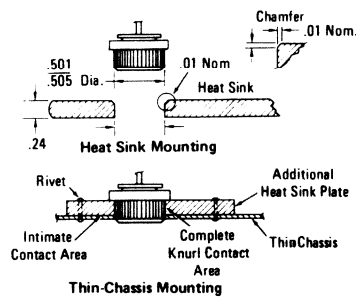


FIGURE 11 – MOUNTING DETAILS FOR PRESSFIT THYRISTORS



3

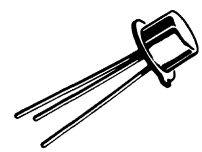
PN Unijunction Transistors
Silicon Annular Unijunction Transistors

2N5431

PN UJTs

. . . characterized primarily for low interbase-voltage operation in sensing, pulse triggering, and timing circuits.

- Low R_{BB} Spread — 6 to 8.5 kΩ
- Low Peak-Point Current — I_P = 4 μA (Max) @ V_{B2B1} = 4 V
- Low Emitter Saturation Voltage — $V_{EB1(sat)}$ = 3 V (Max)
- Narrow Intrinsic Standoff Ratio — η = 0.72 to 0.80



CASE 22A-01
STYLE 1

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Power Dissipation, Note 1	P_D	360	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current, Note 2	i_e	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage, Note 3	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

Notes: 1. Derate 3 mW/°C increase in ambient temperature.
2. Duty Cycle ≤ 1%, PRR = 10 PPS (see Figure 5).
3. Based upon power dissipation at T_A = 25°C.

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
Intrinsic Standoff Ratio, Note 1 (V_{B2B1} = 10 V)	4	η	0.72	0.80	—
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)		R_{BB}	6	8.5	kΩ
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = 0 to 100°C)		αR_{BB}	0.4	0.8	%/°C
Emitter Saturation Voltage, Note 2 (V_{B2B1} = 10 V, I_E = 50 mA)		$V_{EB1(sat)}$	—	3	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	5	30	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		I_{EB2O}	—	10	nA
Peak-Point Emitter Current (V_{B2B1} = 25 V) (V_{B2B1} = 4 V)		I_P	— —	0.4 4	μA
Valley-Point Current (2) (V_{B2B1} = 20 V, R_{B2} = 100 ohms)		I_V	2	—	mA
Base-One Peak Pulse Voltage (V_{BB} = 4 Volts)	3	V_{OB1}	1	—	Volts

Notes: 1. η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.45 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.

2. Use pulse techniques: PW ≈ 300 μs, Duty Cycle ≤ 2% to avoid internal heating, which may result in erroneous readings.

3

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

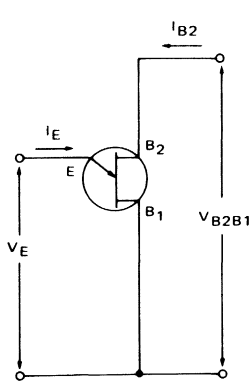


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES

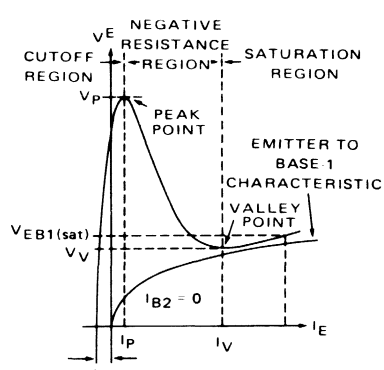


FIGURE 3 – V_{OB1} TEST CIRCUIT

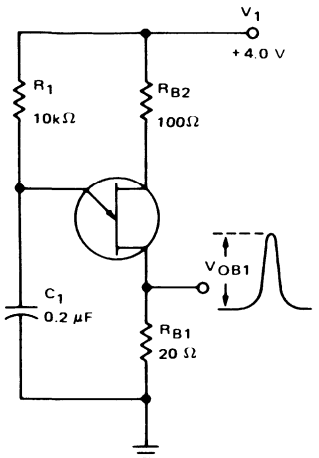


FIGURE 4 – η TEST CIRCUIT

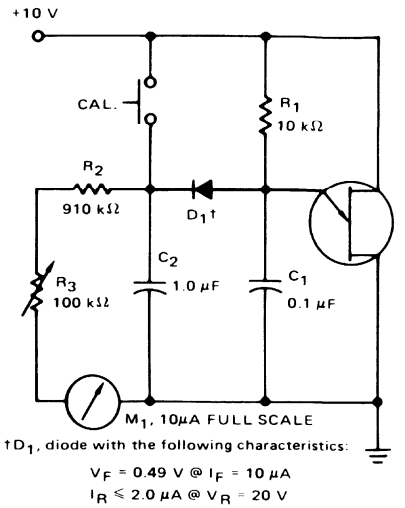


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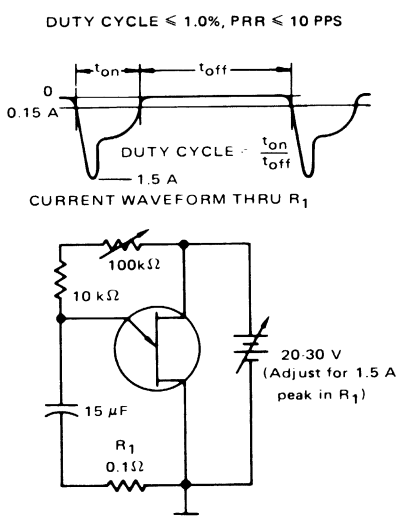
FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM



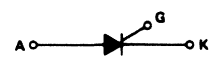
Triacs
Silicon Bidirectional Triode Thyristors

2N5441 thru 2N5446

TRIACs
40 AMPERES RMS
200 thru 600 VOLTS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants



CASE 263-04
STYLE 1
2N5444 thru 2N5446

CASE 310-02
STYLE 1
2N5441 thru 2N5443

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −65 to +110°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
*Peak Principal Voltage 2N5441, 2N5444 2N5442, 2N5445 2N5443, 2N5446		200 400 600	
*RMS On-State Current (T_C per Figure 2) (T_C = +100°C) Full Sine Wave, 50 to 60 Hz	$I_{T(RMS)}$	40 20	Amps
*Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceded and followed by a 40 A RMS current, T_J = +110°C)	I_{TSM}	300	Amps
*Peak Gate Power (Pulse Width = 10 μs Max)	P_{GM}	40	Watts
*Average Gate Power	$P_{G(AV)}$	0.75	Watt
*Peak Gate Current (10 μs Max)	I_{GM}	4	Amps
*Peak Gate Voltage	V_{GM}	30	Volts
*Operating Junction Temperature Range	T_J	−65 to +110	°C
*Storage Temperature Range	T_{stg}	−65 to +150	°C
*Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case 2N5441, 2N5442, 2N5443 2N5444, 2N5445, 2N5446	$R_{\theta JC}$	0.8 0.9 1	°C/W

*Indicates JEDEC Registered Data

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 110°C		—	0.5	4	mA
*Peak On-State Voltage (I_{TM} = 56 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.65	1.85	Volts
Gate Trigger Current (Continuous dc), Note 1 (Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms)	I_{GT}				mA
MT2(+), G(+)		—	—	70	
MT2(+), G(−)		—	—	70	
MT2(−), G(−)		—	—	70	
MT2(−), G(+)		—	—	100	
*MT2(+), G(+); MT2(−), G(−) T_C = −65°C		—	—	125	
*MT2(+), G(−); MT2(−), G(+) T_C = −65°C		—	—	240	
*Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms)	V_{GT}				Volts
MT2(+), G(+)					
MT2(+), G(−)		—	—	2	
MT2(−), G(−)		—	—	2	
MT2(−), G(+)		—	—	2	
*All Quadrants, T_C = −65°C		—	—	2.5	
*Main Terminal Voltage = Rated V_{DRM} = R_L = 10 k ohms,		—	—	3.4	
T_J = +110°C		0.2	—	—	
*Holding Current (Main Terminal Voltage = 12 Vdc, Gate Open) (Initiating Current = 150 mA) T_C = 25°C	I_H	—	—	70	mA
*T_C = −65°C		—	—	100	
*Turn-On Time (Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 56 A, Gate Source Voltage = 12 V, R_S = 12 Ohms, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1	2	μs
*Critical Rate-of-Rise of Commutation Voltage (Rated V_{DRM}, I_{TM} = 40 A, Commutating di/dt = 22 A/ms, gate energized) T_C = 70°C 2N5441, 2N5442, 2N5443	dv/dt(c)	5	30	—	V/μs
= 65°C 2N5444, 2N5445, 2N5446		5	30	—	
		5	30	—	
Critical Rate-of-Rise of Off State Voltage (Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 110°C) 2N5441, 2N5444	dv/dt	50			V/μs
2N5442, 2N5445		30			
2N5443, 2N5446		20			

*Indicates JEDEC Registered Data for 2N5541 thru 2N5446.

Note 1. All voltage polarities referenced to main terminal 1.

3

FIGURE 1 – ON-STATE POWER DISSIPATION

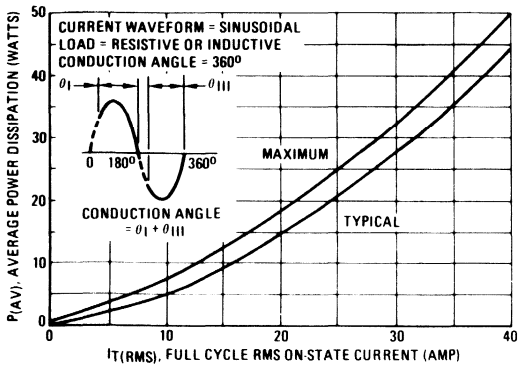


FIGURE 2 – RMS CURRENT DERATING

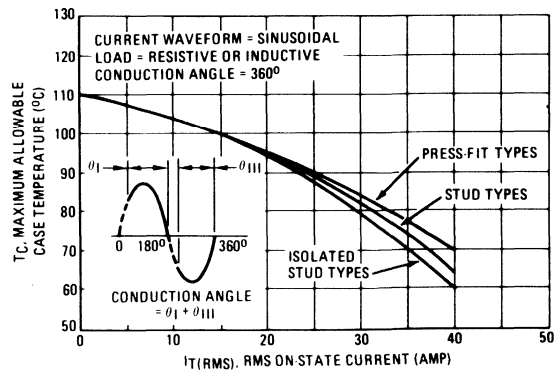


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

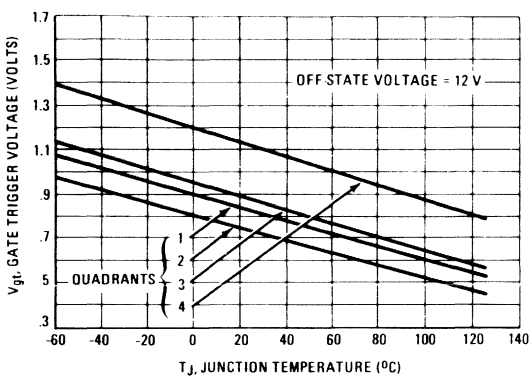


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

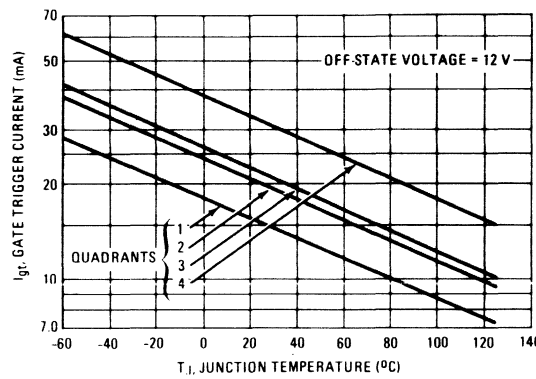


FIGURE 5 – TYPICAL THERMAL RESPONSE

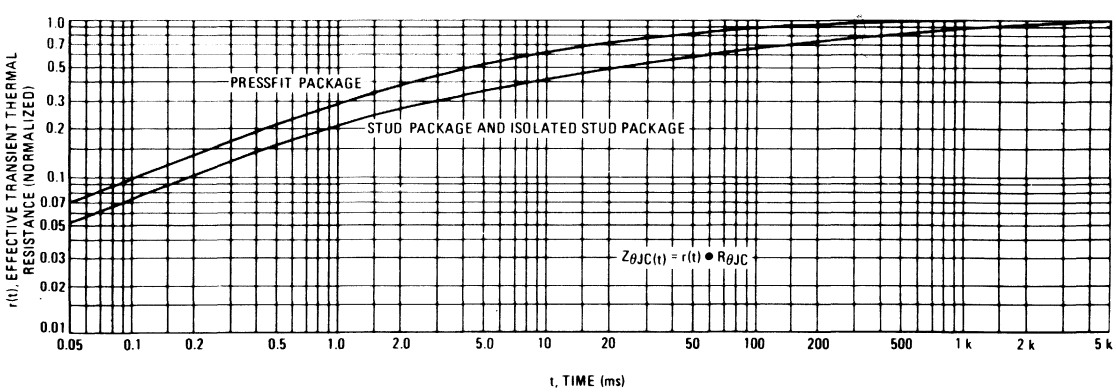


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FIGURE 6 – ON-STATE CHARACTERISTICS

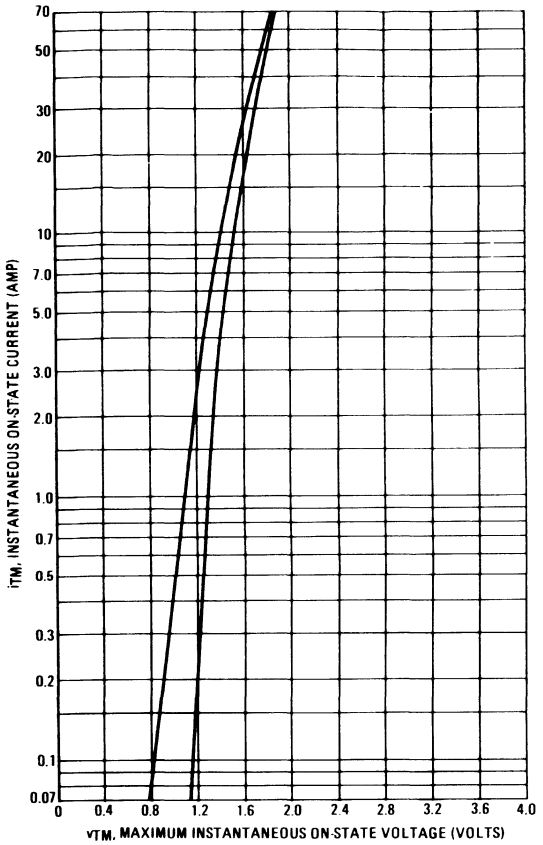


FIGURE 7 – TYPICAL HOLDING CURRENT

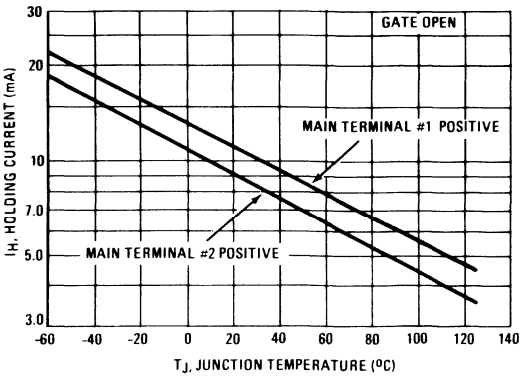
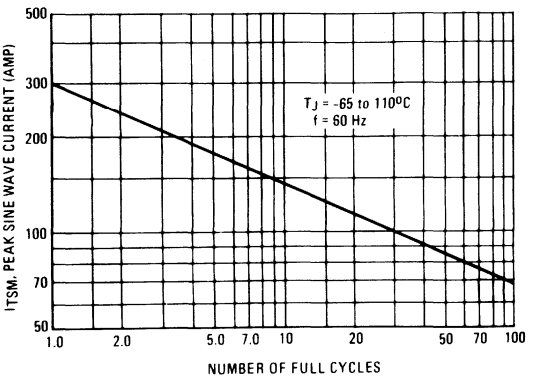


FIGURE 8 – MAXIMUM ALLOWABLE SURGE CURRENT



3

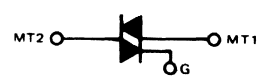
Triacs
Bidirectional Triode Thyristors

. . . designed primarily for industrial and military applications for the fullwave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Quadrants

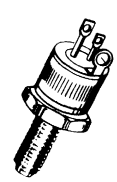
2N5567 thru 2N5570 T4101M T4111M T4121 Series

TRIACs
10 AMPERES RMS
200 thru 600 VOLTS



CASE 174-04
(TO-203)
STYLE 3
2N5667
2N5668
T4101M

CASE 175-03
STYLE 3
2N5569
2N5570
T4111M



CASE 235-03
STYLE 2
T4121 SERIES

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −65 to +100°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N5567, 2N5569, T4121B		200	
2N5568, 2N5570, T4121D		400	
T4101M, T4111M, T4121M		600	
*Peak Gate Voltage	V_{GM}	20	Volts
*RMS On-State Current (T_C = −65 to +85°C)	$I_{T(RMS)}$	10	Amps
(T_C = +90°C) Full cycle, Sine Wave, 50 to 60 Hz		6.7	
*Peak Non-Repetitive Surge Current (One Full cycle of surge current at 60 Hz, preceded and followed by rated current, T_C = 85°C)	I_{TSM}	100	Amps
Circuit Fusing Considerations (T_C = −65 to +85°C, t = 1 to 8.3 ms)	I^2t	40	A^2s
Peak Gate Power *(T_C = 85°C, Pulse Width = 1 μs)	P_{GM}	16	Watts
*Average Gate Power (T_C = 85°C, Pulse Width = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Operating Junction Temperature Range	T_J	−65 to +100	°C
*Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Stud and Pressfit		1	
Isolated Stud		1.1	

*Indicates JEDEC Registered Data.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 100°C		—	—	2	mA
*Peak On-State Voltage (I_{TM} = 14.2 A Peak, Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.3	1.65	Volts
Gate Trigger Current (Continuous dc), Note 1 (V_D = 12 Vdc, R_L = 12 Ohms)	I_{GT}				mA
MT2(+), G(+); MT2(−), G(−)		—	—	25	
MT2(+), G(−); MT2(−), G(+)		—	—	40	
*MT2(+), G(+); MT2(−), G(−), T_C = −65°C		—	—	100	
*MT2(+), G(−); MT2(−), G(+), T_C = −65°C		—	—	150	
Gate Trigger Voltage (Continuous dc) (All Quadrants) (V_D = 12 Vdc, R_L = 12 Ohms T_C = 25°C	V_{GT}	—	—	2.5	Volts
*T_C = −65°C		—	—	4	
(V_D = Rated V_{DRM}, R_L = 125 Ω) T_C = 100°C		0.2	—	—	
Holding Current (V_D = 12 Vdc, Gate Open) T_C = 25°C	I_H	—	—	30	mA
*T_C = −65°C		—	—	200	
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 15 A Peak, I_{GT} = 160 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs) MT2(+), G(+); MT2(−), G(−)	t_{gt}	—	1	2.5	μs
*Critical Rate-of-Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 14.2 A Peak, Commutating di/dt = 5.4 A/ms, gate unenergized) T_C = 85°C	dv/dt(c)	2	10	—	V/μs
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C)	dv/dt				V/μs
*2N5567, *2N5569, T4121B		30	150	—	
*2N5568, *2N5570, T4121D		20	100	—	
T4101M, T4111M, T4121M		10	75	—	

*Indicates JEDEC Registered Data.
Note 1. All Voltage polarities referenced to main terminal 1.

3

FIGURE 1 – RMS CURRENT DERATING (Isolated Stud)

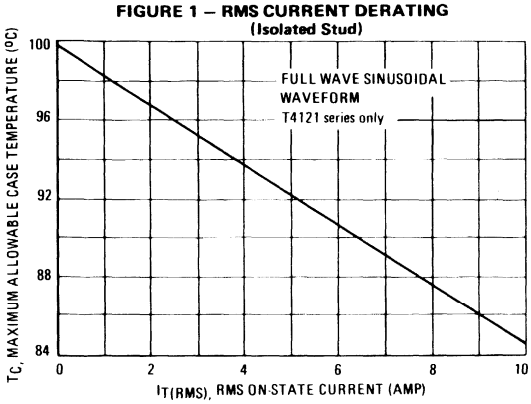


FIGURE 2 – RMS CURRENT DERATING (Pressfit and Stud)

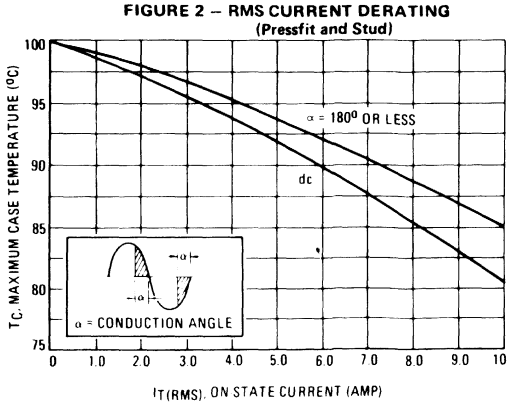


FIGURE 3 – POWER DISSIPATION
(Isolated Stud)

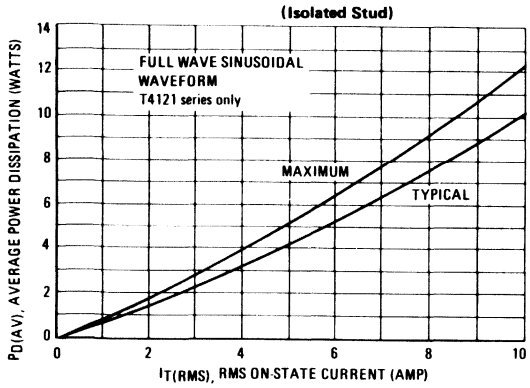


FIGURE 4 – POWER DISSIPATION
(Pressfit and Stud)

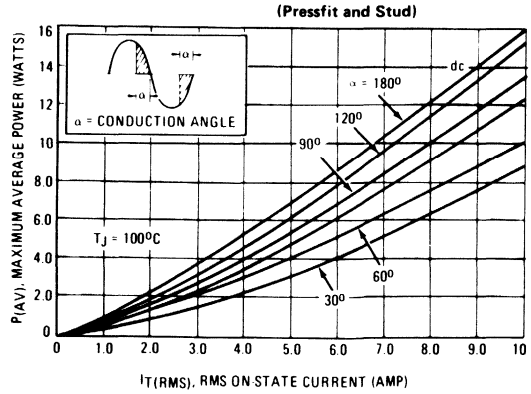


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

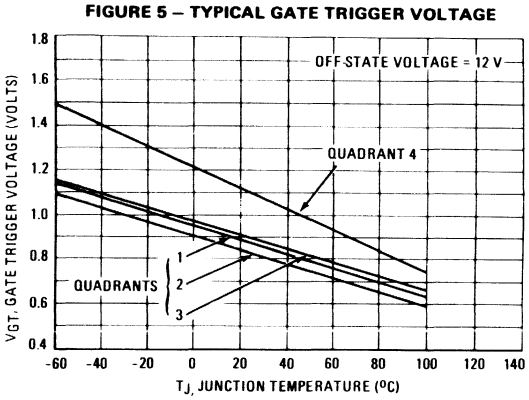


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

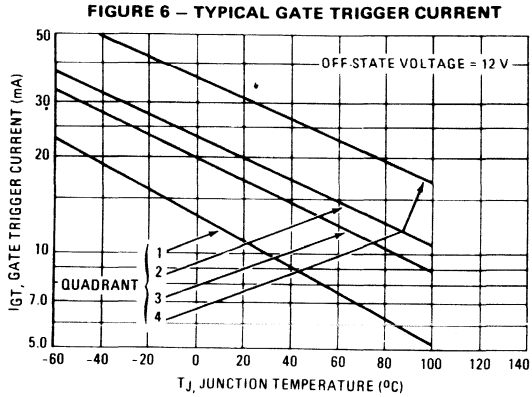


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FIGURE 7 – ON-STATE CHARACTERISTICS

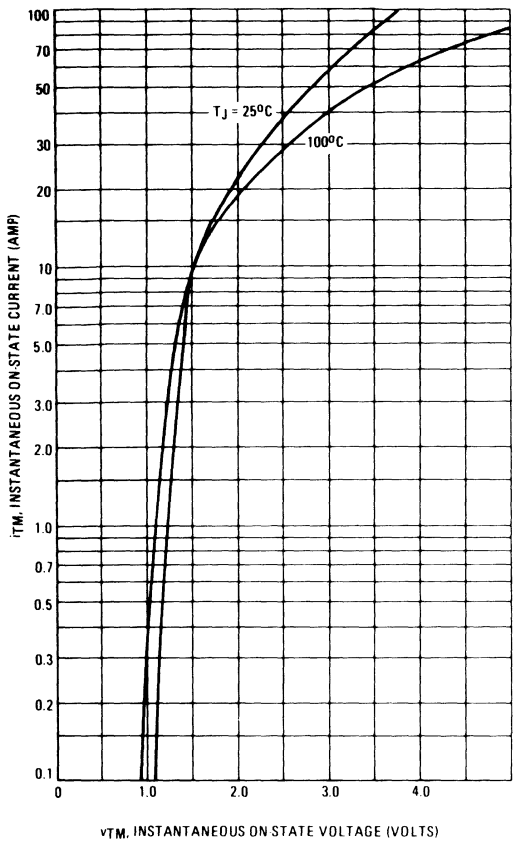


FIGURE 8 – TYPICAL HOLDING CURRENT

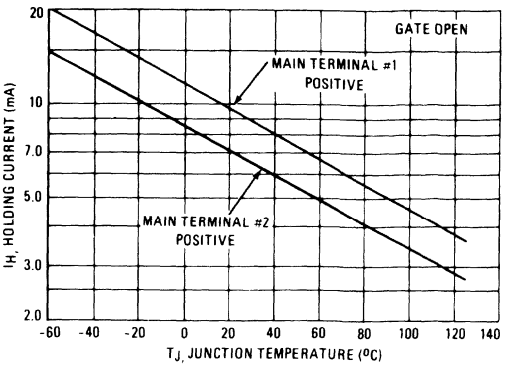


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

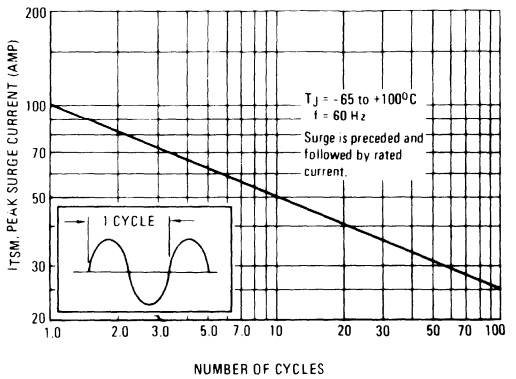
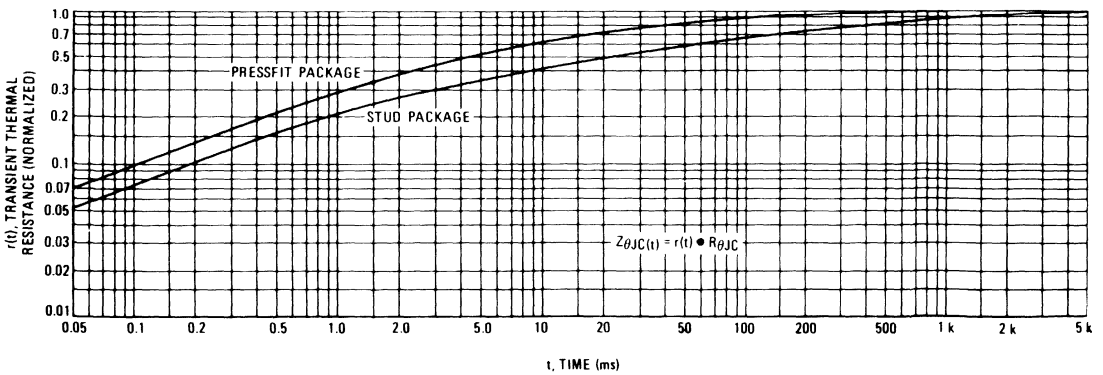


FIGURE 10 – TYPICAL THERMAL RESPONSE



Triacs

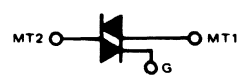
Silicon Bidirectional Triode Thyristors

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Quadrants

2N5571 thru 2N5574 2N6145 thru 2N6147 T4100M T4110M

TRIACs
15 AMPERES RMS
200 thru 600 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −65 to +100°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N5571, 2N5573, 2N6145		200	
2N5572, 2N5574, 2N6146		400	
T4100M, T4110M, 2N6147		600	
*Peak Gate Voltage	V_{GM}	20	Volts
*RMS On-State Current (T_C = −65 to +80°C)	$I_{T(RMS)}$	15	Amps
(T_C = +85°C)		10	
*Peak Non-Repetitive Surge Current (One Full cycle of surge current at 60 Hz, preceded and followed by rated current, T_C = 85°C)	I_{TSM}	100	Amps
Circuit Fusing (T_C = −65 to +80°C, t = 1 to 8.3 ms)	I^2t	40	A^2s
Peak Gate Power *(T_C = 80°C, Pulse Width = 1 μs)	P_{GM}		Watts
2N5571 thru 2N5574		16	
T4100M, T4110M		16	
*(T_C = 80°C, Pulse Width = 2 μs) 2N6145 thru 2N6147		20	
*Average Gate Power (T_C = 80°C, Pulse Width = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2	Amps
*Operating Junction Temperature Range	T_J	−65 to +100	°C
*Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque *2N5573, 2N5574, T4110M *2N6145, 2N6146, 2N6147	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W

*Indicates JEDEC Registered Data.

CASE 174-04 (TO-203) STYLE 3 2N5571 2N5572 T4100M

CASE 175-03 STYLE 3 2N5573 2N5574 T4110M

CASE 311-02 STYLE 2 2N6145 2N6146 2N6147

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = 100°C		—	—	2	mA
*Peak On-State Voltage (I_{TM} = 21 A Peak, Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.3	1.8	Volts
Gate Trigger Current (Continuous dc), Note 1 (V_D = 12 Vdc, R_L = 30 Ohms)	I_{GT}				mA
MT2(+), G(+); MT2(−), G(−)		—	—	50	
MT2(+), G(−); MT2(−), G(+)		—	—	80	
*MT2(+), G(+); MT2(−), G(−), T_C = −65°C		—	—	150	
*MT2(+), G(−); MT2(−), G(+), T_C = −65°C		—	—	200	
Gate Trigger Voltage (Continuous dc) (All Quadrants) (V_D = 12 Vdc, R_L = 30 Ohms) T_C = 25°C	V_{GT}	—	—	2.5	Volts
*T_C = −65°C		—	—	4	
*(V_D = Rated V_{DRM}, R_L = 10 k ohms, T_C = +100°C)		0.2	—	—	
Holding Current (V_D − 12 Vdc, Gate Open) (Initiating Current = 500 mA) T_C = 25°C	I_H	—	—	75	mA
*T_C = −65°C		—	—	300	
Gate Controlled Turn-On Time (Rated V_{DRM}, I_{TM} = 21 A Peak, I_{GT} = 160 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1	2	μs
*Critical Rate-of-Rise of Commutation Voltage (Rated V_{DRM}, I_{TM} = 21 A Peak, Commutating di/dt = 8 A/ms, gate unenergized T_C = 80°C 2N5571 thru 2N5574, T4100M, T4110M	dv/dt(c)	2	10	—	V/μs
T_C = 75°C 2N6145 thru 2N6147		2	10	—	
Critical Rate-of-Rise of Off-State Voltage (Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C) *2N5571, 2N5573, 2N6145	dv/dt	30	150	—	V/μs
*2N5572, 2N5574, 2N6146		20	100	—	
T4100M, T4110M, 2N6147		10	75	—	

*Indicates JEDEC Registered Data.
Note 1. All Voltage polarities referenced to main terminal 1.

3

FIGURE 1 – RMS CURRENT DERATING

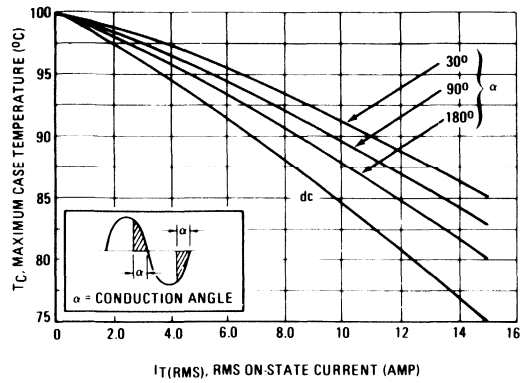


FIGURE 2 – ON-STATE POWER DISSIPATION

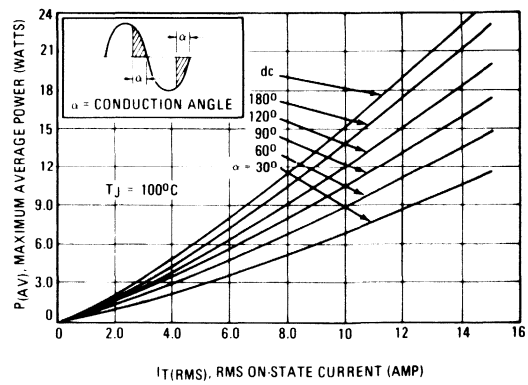


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

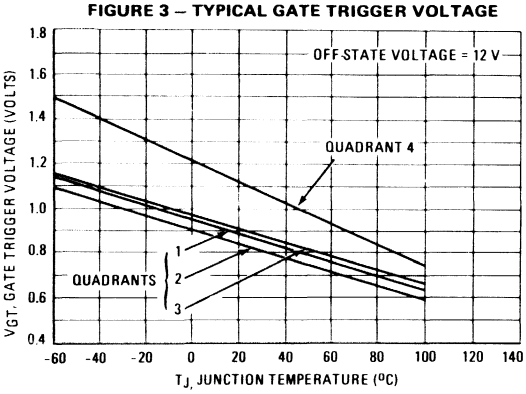


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

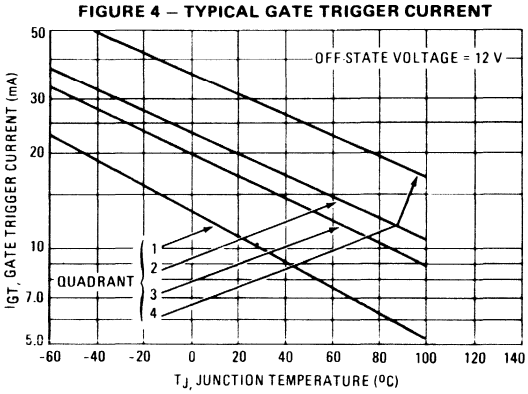


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FIGURE 5 – MAXIMUM ON-STATE CHARACTERISTICS

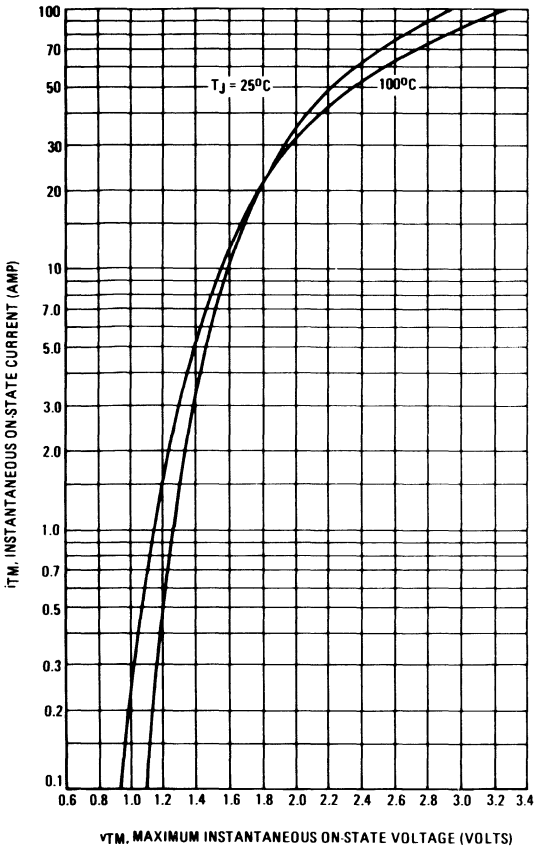


FIGURE 6 – TYPICAL HOLDING CURRENT

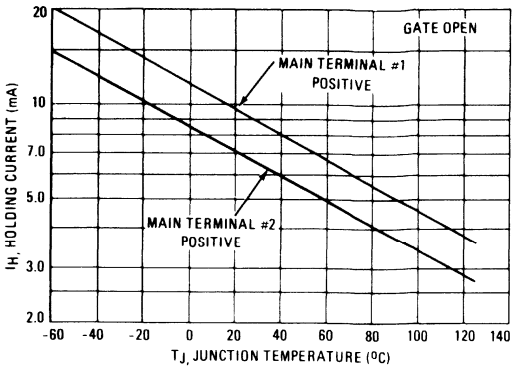


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

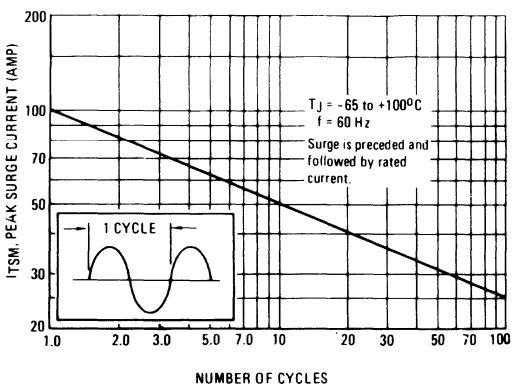
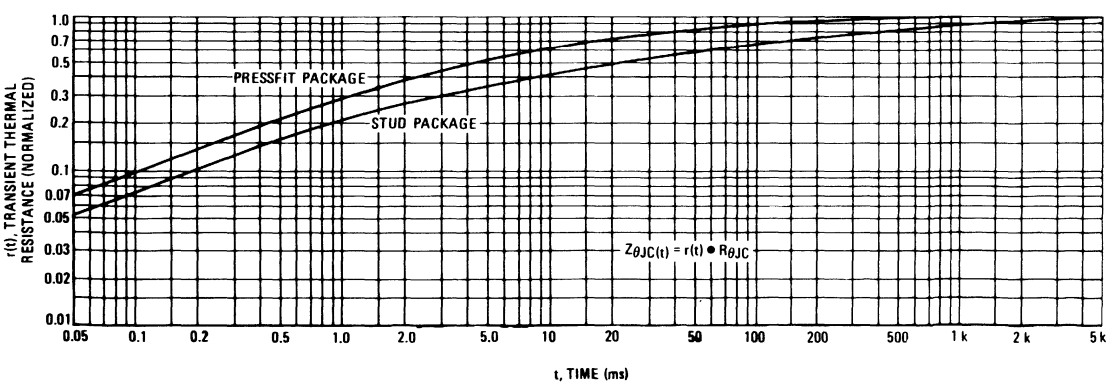


FIGURE 8 – TYPICAL THERMAL RESPONSE



Programmable Unijunction Transistors

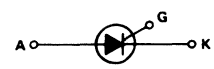
Silicon Programmable Unijunction Transistors

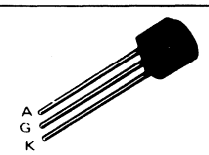
2N6027
2N6028

PUTs
40 VOLTS
375 mW

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable — R_{BB}, η, I_V and I_P.
- Low On-State Voltage — 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current — 10 nA Maximum
- High Peak Output Voltage — 11 Volts Typical
- Low Offset Voltage — 0.35 Volt Typical (R_G = 10 k ohms)





CASE 29-04
(TO-226AA)
STYLE 16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Power Dissipation Derate Above 25°C	P_F $1/\theta_{JA}$	300 4	mW mW/°C
*DC Forward Anode Current Derate Above 25°C	I_T	150 2.67	mA mA/°C
*DC Gate Current	I_G	±50	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1% Duty Cycle *20 μs Pulse Width, 1% Duty Cycle	I_{TRM}	 1 2	Amps
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5	Amps
*Gate to Cathode Forward Voltage	V_{GKF}	40	Volts
*Gate to Cathode Reverse Voltage	V_{GKR}	−5	Volts
*Gate to Anode Reverse Voltage	V_{GAR}	40	Volts
*Anode to Cathode Voltage, Note 1	V_{AK}	±40	Volts
Operating Junction Temperature Range	T_J	−50 to +100	°C
*Storage Temperature Range	T_{stg}	−55 to +150	°C

*Indicates JEDEC Registered Data

Note 1. Anode positive, R_{GA} = 1000 ohms
Anode negative, R_{GA} = open

3

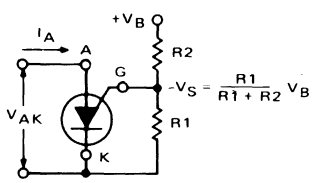
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
*Peak Current		2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1 MΩ)	2N6027			—	1.25	2	
	2N6028			—	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			—	4	5	
	2N6028			—	0.70	1	
*Offset Voltage		1	V_T				Volts
(V_S = 10 Vdc, R_G = 1 MΩ)	2N6027			0.2	0.70	1.6	
	2N6028			0.2	0.50	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	(Both Types)			0.2	0.35	0.6	
*Valley Current		1,4,5	I_V				μA
(V_S = 10 Vdc, R_G = 1 MΩ)	2N6027			—	18	50	
	2N6028			—	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			70	150	—	
	2N6028			25	150	—	
(V_S = 10 Vdc, R_G = 200 ohms)	2N6027			1.5	—	—	mA
	2N6028			1	—	—	
*Gate to Anode Leakage Current		—	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				—	1	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				—	3	—	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		—	I_{GKS}	—	5	50	nAdc
*Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	—	0.8	1.5	Volts
*Peak Output Voltage (V_G = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6	11	—	Volt
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	—	40	80	ns

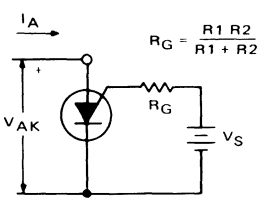
*Indicates JEDEC Registered Data.

3

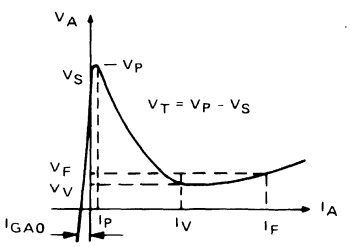
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – Programmable Unijunction with "Program" Resistors R1 and R2



1B – Equivalent Test Circuit for Figure 1A used for electrical characteristics testing (also see Figure 2)



IC – Electrical Characteristics

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

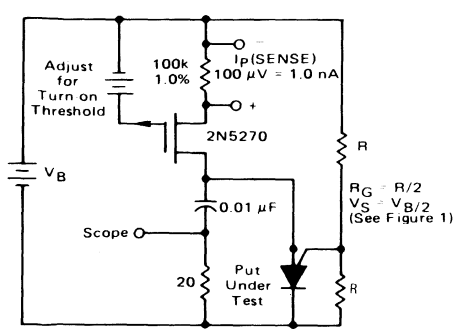
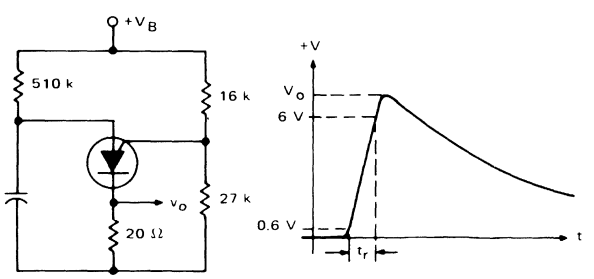


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

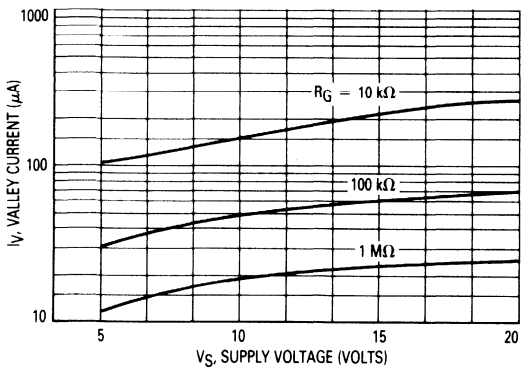


FIGURE 5 – EFFECT OF TEMPERATURE

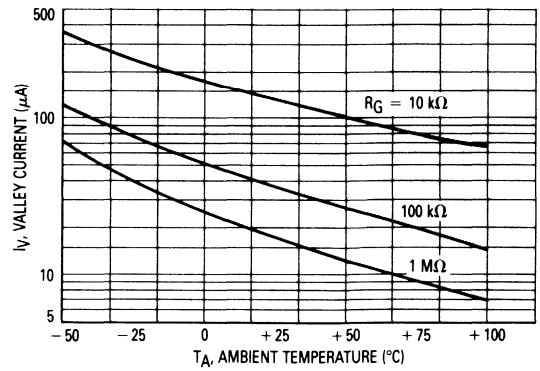


FIGURE 6 – FORWARD VOLTAGE

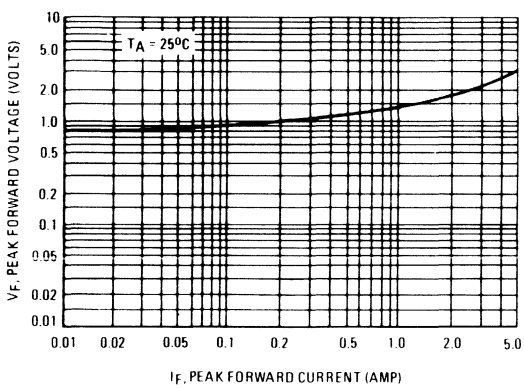


FIGURE 7 – PEAK OUTPUT VOLTAGE

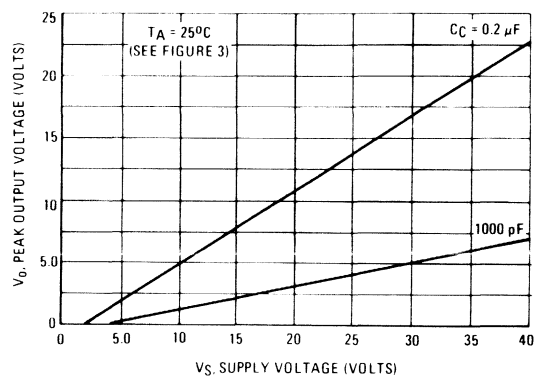
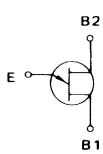
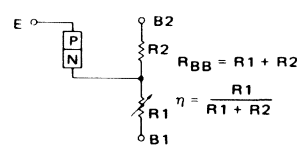


FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION

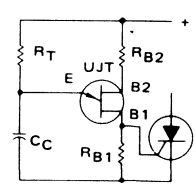
STANDARD UNIJUNCTION



Circuit Symbol

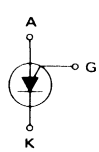


Equivalent Circuit

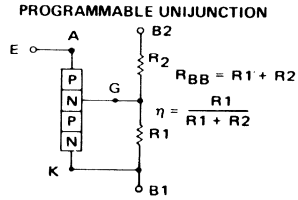


Typical Application

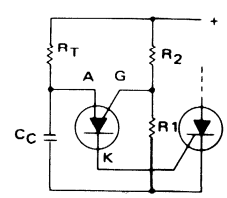
PROGRAMMABLE UNIJUNCTION



Circuit Symbol



Equivalent Circuit with External "Program" Resistors R1 and R2



Typical Application

TYPICAL PEAK CURRENT BEHAVIOR

2N6027

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

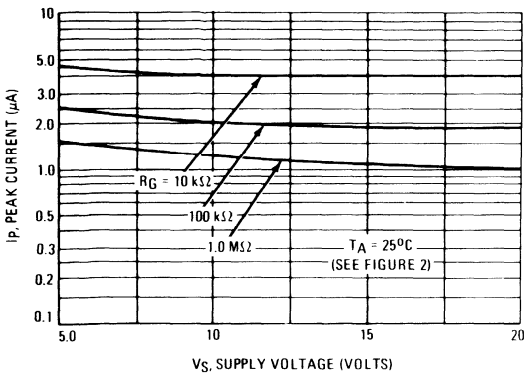
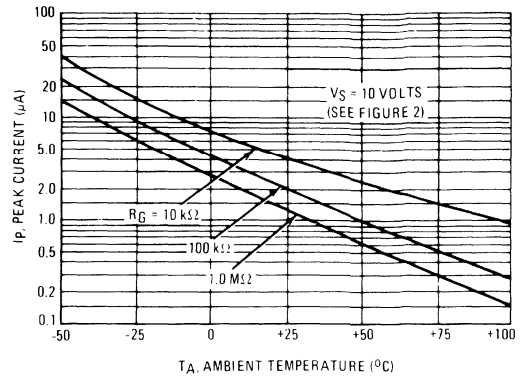


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6028

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

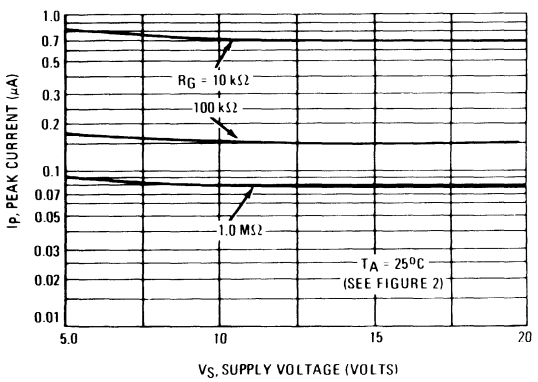
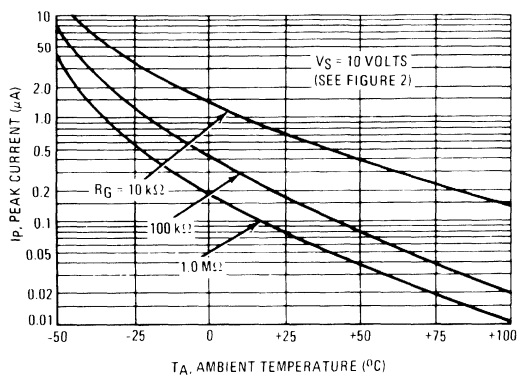


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



3

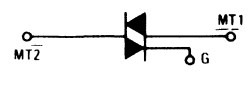
Sensitive Gate Triacs
Silicon Bidirectional Thyristors

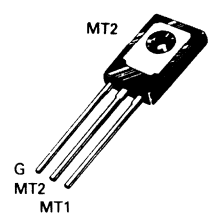
2N6071,A,B thru 2N6075,A,B

TRIACs
4 AMPERES RMS
200 thru 600 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering (A and B versions) Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions
- Gate Triggering 2 Mode — 2N6071 thru 2N6075
  4 Mode — 2N6071A,B thru 2N6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability





CASE 77-05
(TO-225AA)
STYLE 5

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = 110°C) 2N6071,A,B	V_{DRM}	200	Volts
2N6072,A,B		300	
2N6073,A,B		400	
2N6074,A,B		500	
2N6075,A,B		600	
*On-State Current RMS (T_C = 85°C)	$I_{T(RMS)}$	4	Amps
*Peak Surge Current (One Full cycle, 60 Hz, T_J = −40 to +110°C)	I_{TSM}	30	Amps
Circuit Fusing Considerations (T_J = −40 to +110°C, t = 1 to 8.3 ms)	I^2t	3.6	A^2s
*Peak Gate Power	P_{GM}	10	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Voltage	V_{GM}	5	Volts

*Indicates JEDEC Registered Data.

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Operating Junction Temperature Range	T_J	−40 to +110	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque (6-32 Screw), Note 1	—	8	in. lb.

*Indicates JEDEC Registered Data.

Note 1. Torque rating applies with use of compression washer (B52200F006). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	75	°C/W

*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current	I_{DRM}, I_{RRM}				
(Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C		—	—	10	μA
T_J = 110°C		—	—	2	mA
*On-State Voltage (Either Direction)	V_{TM}	—	—	2	Volts
(I_{TM} = 6 A Peak)					
*Peak Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = −40°C)					
MT2(+), G(+); MT2(−), G(−) All Types		—	1.4	2.5	
MT2(+), G(−); MT2(−), G(+) 2N6071A,B thru 2N6075A,B		—	1.4	2.5	
(Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C)					
MT2(+), G(+); MT2(−), G(−) All Types		0.2	—	—	
MT2(+), G(−); MT2(−), G(+) 2N6071A,B thru 2N6075A,B		0.2	—	—	
*Holding Current (Either Direction)	I_H				mA
(Main Terminal Voltage = 12 Vdc, Gate Open, T_J = −40°C)					
(Initiating Current = 1 Adc) 2N6071 thru 2N6075		—	—	70	
2N6071A,B thru 2N6075A,B		—	—	30	
(T_J = 25°C) 2N6071 thru 2N6075		—	—	30	
2N6071A,B thru 2N6075A,B		—	—	15	
Turn-On Time (Either Direction)	t_{on}	—	1.5	—	μs
(I_{TM} = 14 Adc, I_{GT} = 100 mAdc)					
Blocking Voltage Application Rate at Commutation	dv/dt	—	5	—	V/μs
@ V_{DRM}, T_J = 85°C, Gate Open					

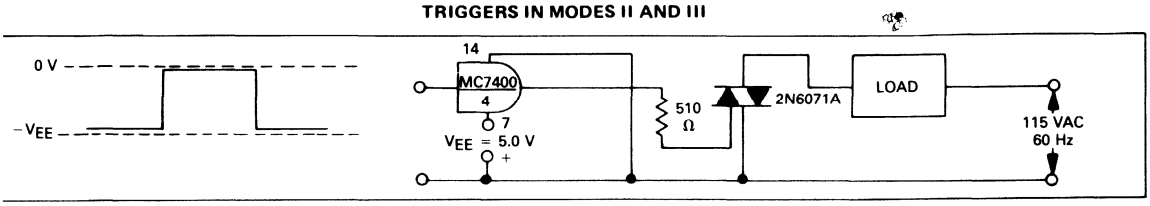
*Indicates JEDEC Registered Data.

3

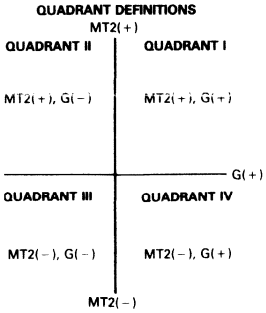
			QUADRANT (See Definition Below)			
	Type	I_{GT} @ T_J	I mA	II mA	III mA	IV mA
Gate Trigger Current (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 ohms)	2N6071 thru 2N6075	+25°C	30	—	30	—
		−40°C	60	—	60	—
Maximum Value	2N6071A thru 2N6075A	+25°C	5	5	5	10
		−40°C	20	20	20	30
	2N6071B thru 2N6075B	+25°C	3	3	3	5
		−40°C	15	15	15	20

*Indicates JEDEC Registered Data.

SAMPLE APPLICATION:
TTL-SENSITIVE GATE 4 AMPERE TRIAC TRIGGERS IN MODES II AND III



QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

For 2N6071 Thru 2N6075
ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

Usage	General		Lamp Dimmer
Part Number	MBS4991	MBS4993	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 μA Max	250 μA Max	100 – 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

SENSITIVE GATE LOGIC REFERENCE

IC Logic Functions	Firing Quadrant			
	I	II	III	IV
TTL		2N6071A Series	2N6071A Series	
HTL		2N6071A Series	2N6071A Series	
CMOS (NAND)	2N6071B Series			2N6071B Series
CMOS (Buffer)		2N6071B Series	2N6071B Series	
Operational Amplifier	2N6071A Series			2N6071A Series
Zero Voltage Switch		2N6071A Series	2N6071A Series	

3

FIGURE 1 – AVERAGE CURRENT DERATING

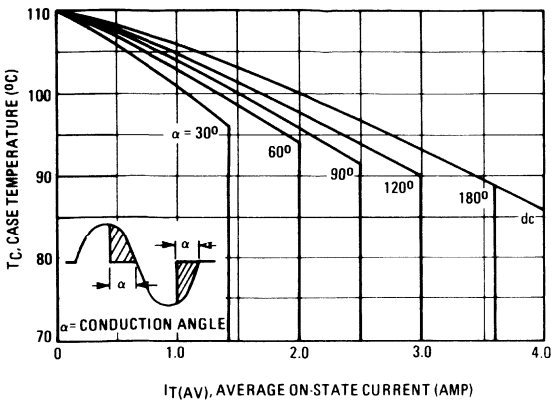


FIGURE 2 – RMS CURRENT DERATING

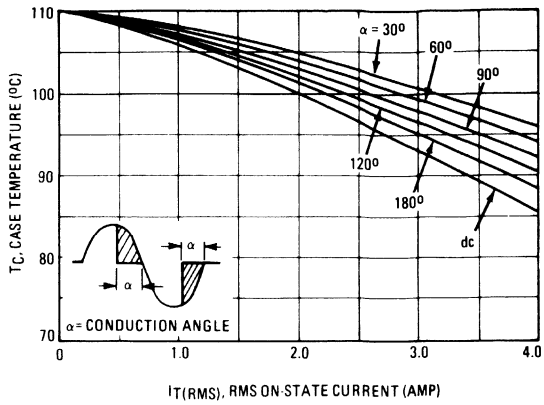


FIGURE 3 – POWER DISSIPATION

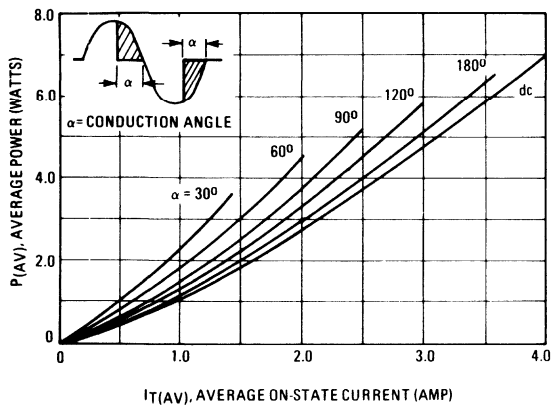


FIGURE 4 – POWER DISSIPATION

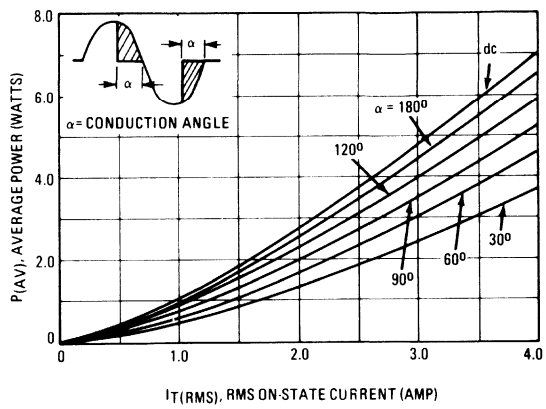


FIGURE 5 – TYPICAL GATE-TRIGGER VOLTAGE

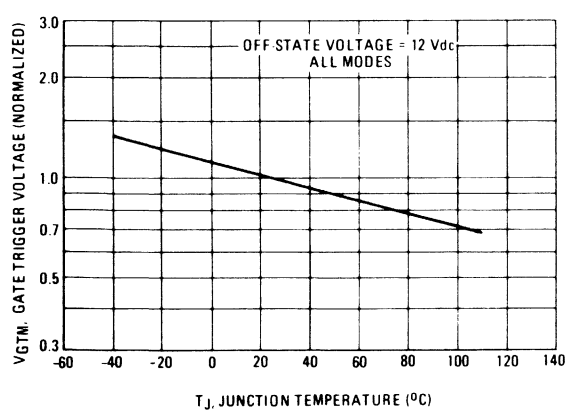


FIGURE 6 – TYPICAL GATE-TRIGGER CURRENT

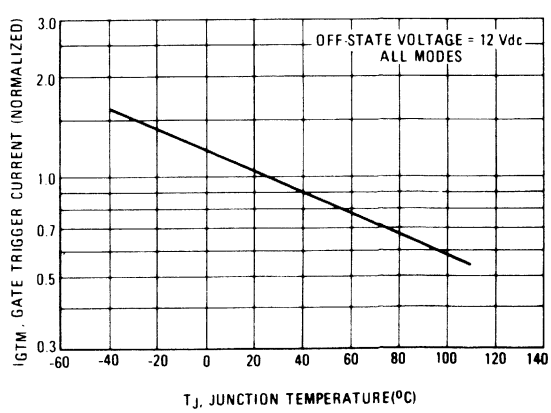


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

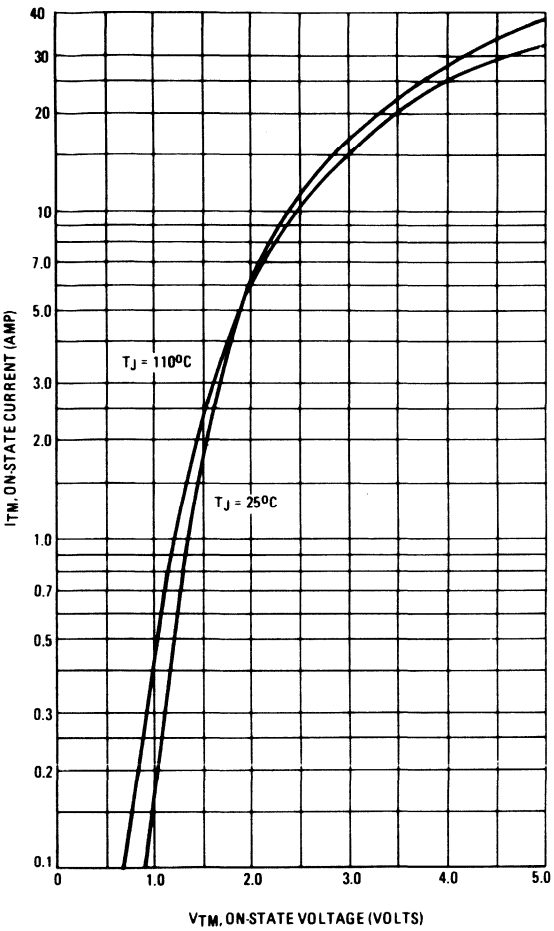


FIGURE 8 – TYPICAL HOLDING CURRENT

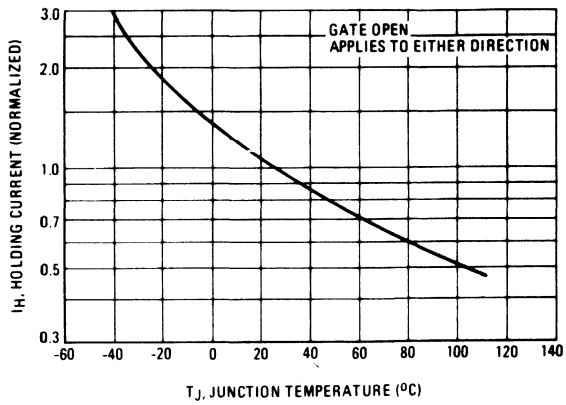


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

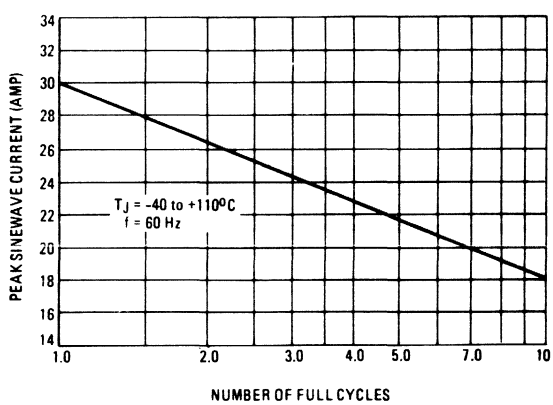
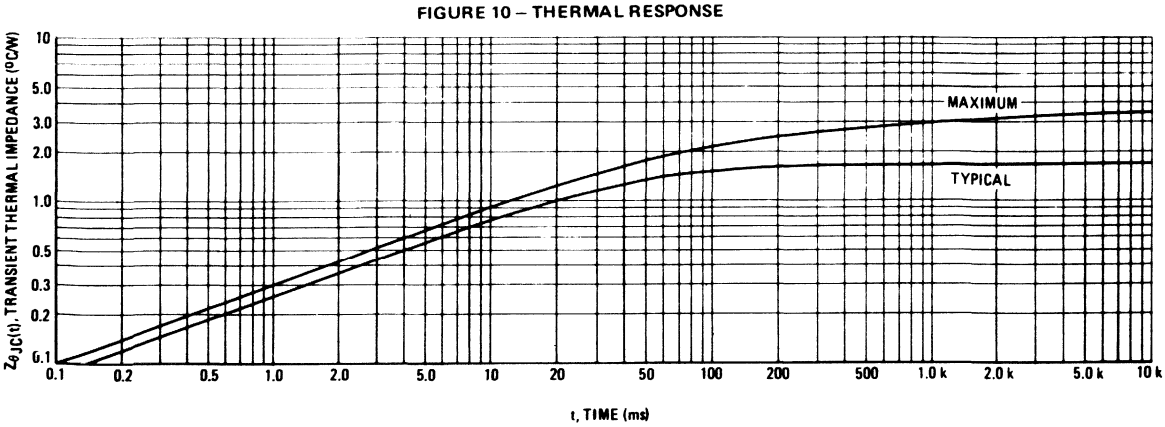


FIGURE 10 – THERMAL RESPONSE



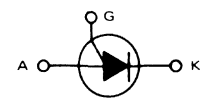
Silicon Programmable Unijunction Transistors

2N6116
2N6117
2N6118

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate.

- Programmable — R_{BB}, η, I_V and I_P
- Hermetic TO-18 Package
- Low On-State Voltage — 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current — 5 nA Maximum
- High Peak Output Voltage — 16 Volts Typical
- Low Offset Voltage — 0.35 Volt Typical (R_G = 10 k ohms)

PUTs
40 VOLTS — 250 mW



CASE 22-03
(TO-18)
STYLE 13

3

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Repetitive Peak Forward Current 100 μs Pulse Width, 1% Duty Cycle 20 μs Pulse Width, 1% Duty Cycle	I_{TRM}	 1 2	Amps
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5	Amps
DC Forward Anode Current Derate Above 25°C	I_T	200 2	mA mA/°C
DC Gate Current	I_G	±20	mA
Gate to Cathode Forward Voltage	V_{GKF}	40	Volts
Gate to Cathode Reverse Voltage	V_{GKR}	5	Volts
Gate to Anode Reverse Voltage	V_{GAR}	40	Volts
Anode to Cathode Voltage	V_{AK}	±40	Volts
Forward Power Dissipation @ T_A = 25°C Derate Above 25°C	P_F $1/\theta_{JA}$	250 2.5	mW mW/°C
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

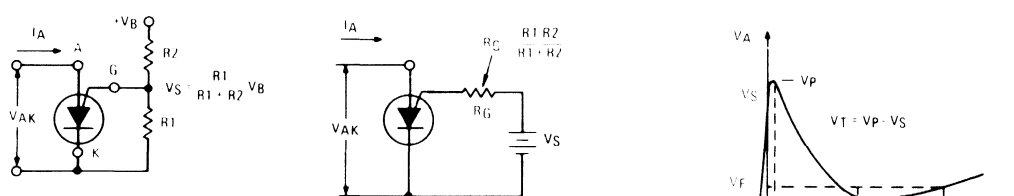
*Indicates JEDEC Registered Data.

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Offset Voltage	2N6116	1	V_T	0.2	0.70	1.6	Volts
(V_S = 10 Vdc, R_G = 1 MΩ)	2N6117			0.2	0.50	0.6	
	2N6118			0.2	0.40	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	All Types			0.2	0.35	0.6	
Gate to Anode Leakage Current		—	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				—	1	5	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				—	30	75	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		—	I_{GKS}	—	5	50	nAdc
Peak Current	2N6116	2,9,14	I_P	—	1.25	2	μA
(V_S = 10 Vdc, R_G = 1 MΩ)	2N6117			—	0.19	0.3	
	2N6118			—	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6116			—	4	5	
	2N6117			—	1.20	2	
	2N6118			—	0.70	1	
Valley Current		1,4,5	I_V				μA
(V_S = 10 Vdc, R_G = 1 MΩ)	2N6116, 2N6117			—	18	50	
	2N6118			—	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6116			70	270	—	
	2N6117, 2N6118			50	270	—	
Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	—	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_O	6	16	—	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	—	40	80	ns

*Indicates JEDEC Registered Data.

FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2

1B EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)

1C ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

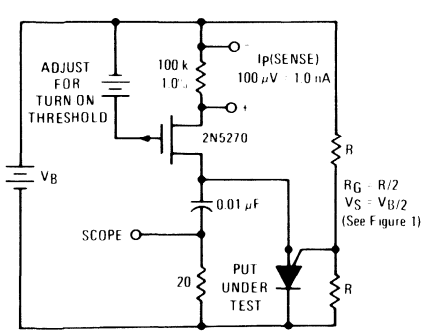
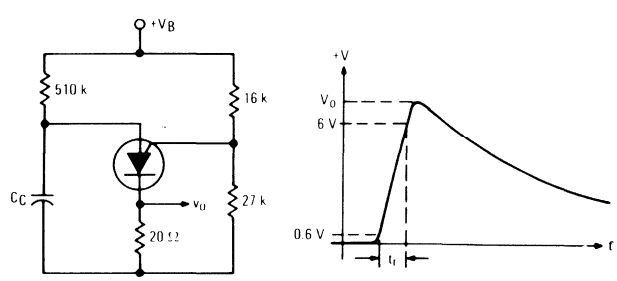


FIGURE 3 – V_O AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

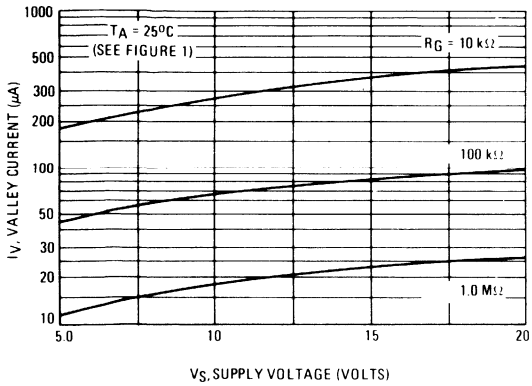


FIGURE 5 – EFFECT OF TEMPERATURE

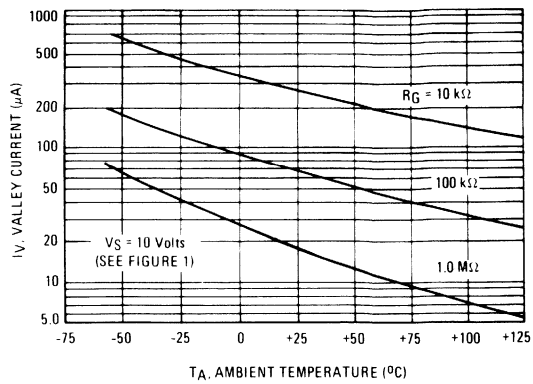


FIGURE 6 – FORWARD VOLTAGE

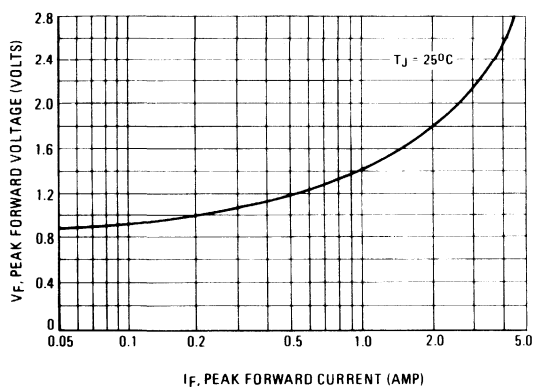


FIGURE 7 – PEAK OUTPUT VOLTAGE

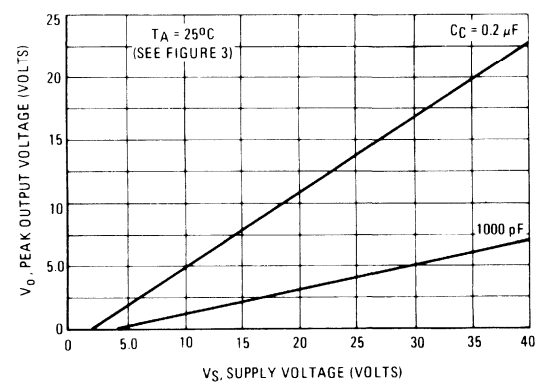
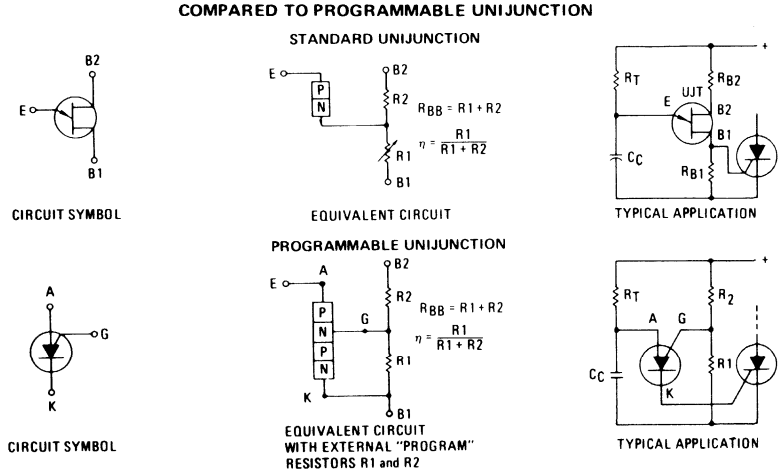


FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION



TYPICAL PEAK CURRENT BEHAVIOR

2N6116

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

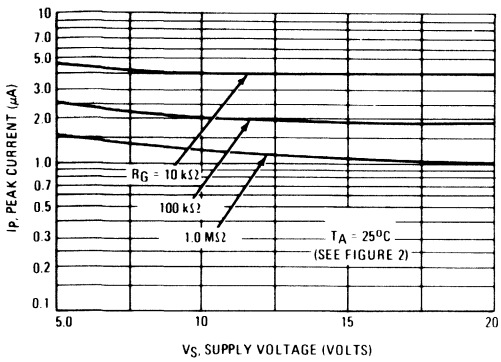
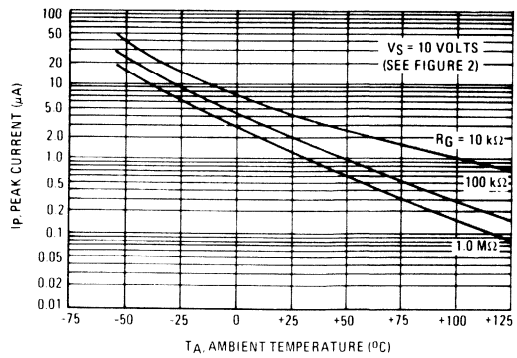


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6117

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

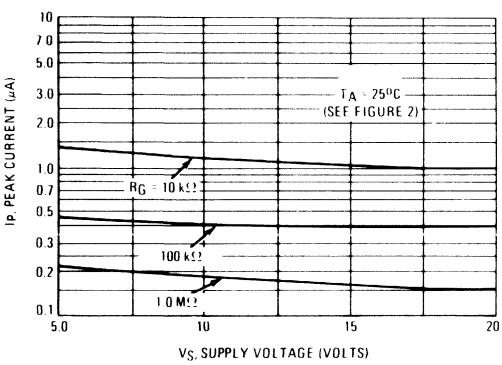
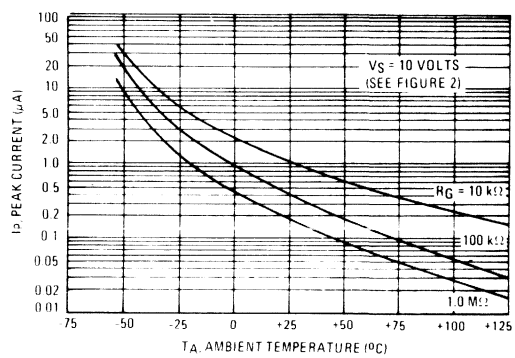


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



2N6118

FIGURE 13 – EFFECT OF SUPPLY VOLTAGE AND R_G

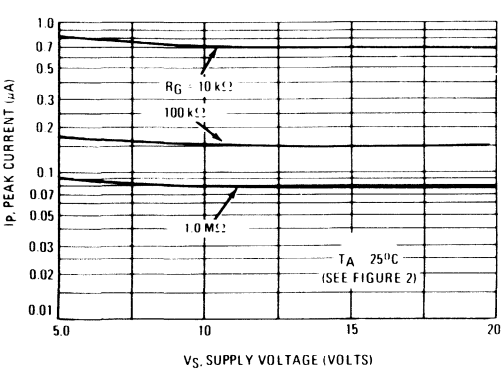
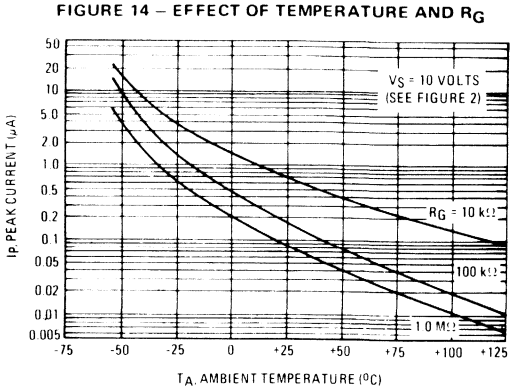


FIGURE 14 – EFFECT OF TEMPERATURE AND R_G



3

Triacs
Silicon Bidirectional Triode Thyristors

2N6157 thru 2N6165

TRIACs
30 AMPERES RMS
200 thru 600 VOLTS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants

CASE 174-04
STYLE 3
2N6157-59

CASE 263-04
STYLE 2
2N6160-62

CASE 311-02
STYLE 2
2N6163-65

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −65 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open *Peak Principal Voltage	V_{DRM}		Volts
2N6157, 2N6160, 2N6163		200	
2N6158, 2N6161, 2N6164		400	
2N6159, 2N6162, 2N6165		600	
*Peak Gate Voltage	V_{GM}	10	Volts
*RMS On-State Current (T_C = −65 to +85°C)	$I_{T(RMS)}$	30	Amps
(T_C = +100°C) Full Sine Wave, 50 to 60 Hz		20	
*Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceded and followed by a 30 A RMS current, T_J = +125°C)	I_{TSM}	250	Amps
Circuit Fusing Considerations (T_J = −65 to +125°C, t = 1 to 8.3 ms)	I^2t	210	A^2s
*Peak Gate Power (T_J = +80°C, Pulse Width = 2 μs)	P_{GM}	20	Watts
*Average Gate Power (T_J = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2	Amps
*Operating Junction Temperature Range	T_J	−65 to +125	°C
*Storage Temperature Range	T_{stg}	−65 to +150	°C
*Stud Torque 2N6160 thru 2N6165	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W

*Indicates JEDEC Registered Data.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
*Peak On-State Voltage (Either Direction) (I_{TM} = 42 A Peak, Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.5	2	Volts
Gate Trigger Current (Continuous dc), Note 1 (Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms)	I_{GT}				mA
MT2(+), G(+)		—	15	60	
MT2(+), G(−)		—	20	70	
MT2(−), G(−)		—	20	70	
MT2(−), G(+)		—	30	100	
*MT2(+), G(+); MT2(−), G(−) T_C = −65°C		—	—	200	
*MT2(+), G(−); MT2(−), G(+) T_C = −65°C		—	—	250	
Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms)	V_{GT}				Volts
MT2(+), G(+)		—	0.8	2	
MT2(+), G(−)		—	0.7	2.1	
MT2(−), G(−)		—	0.85	2.1	
MT2(−), G(+)		—	1.1	2.5	
*All Quadrants, T_C = −65°C		—	—	3.4	
*Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = +125°C		0.2	—	—	
Holding Current (Main Terminal Voltage = 12 Vdc, Gate Open) (Initiating Current = 500 mA)	I_H				mA
MT2(+)		—	8	70	
MT2(−)		—	10	80	
*Either Direction, T_C = −65°C		—	—	200	
*Turn-On Time (Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 42 A, Gate Source Voltage = 12 V, R_S = 50 Ohms, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1	2	μs
Blocking Voltage Application Rate at Commutation, f = 60 Hz, T_C = 85°C On-State Conditions: (I_{TM} = 42 A, Pulse Width = 4 ms, di/dt = 17.5 A/ms) Off-State Conditions: (Main Terminal Voltage = Rated V_{DRM} (200 μs min), Gate Source Voltage = 0 V, R_S = 50 Ω)	dv/dt(c)	—	5	—	V/μs

*Indicates JEDEC Registered Data.
Note 1. All voltage polarities referenced to main terminal 1.

FIGURE 1 — RMS CURRENT DERATING

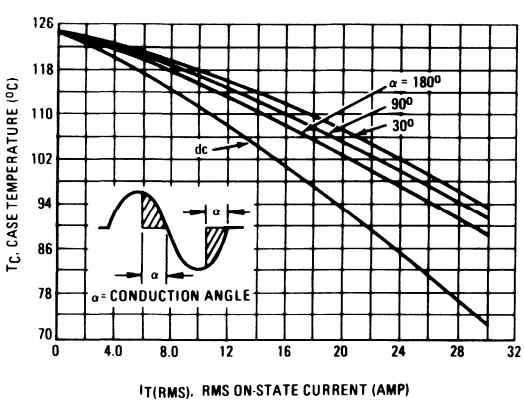


FIGURE 2 — POWER DISSIPATION

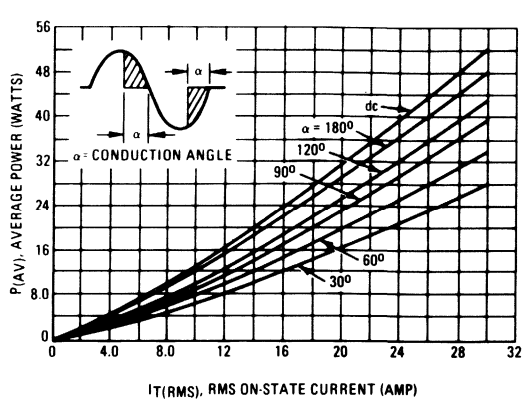


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

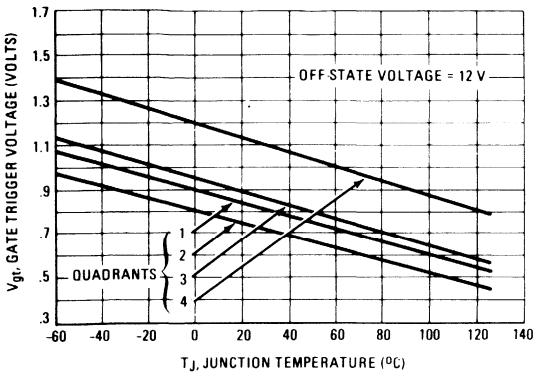


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

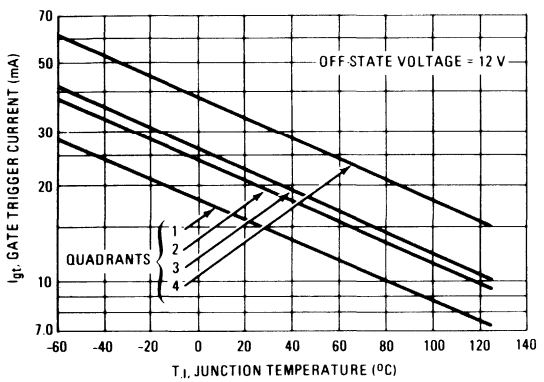


FIGURE 5 – MAXIMUM ON-STATE CHARACTERISTICS

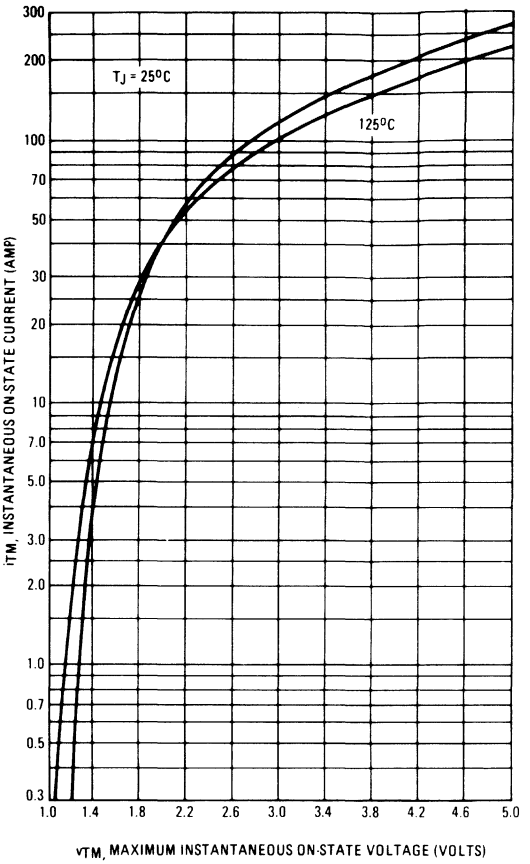


FIGURE 6 – TYPICAL HOLDING CURRENT

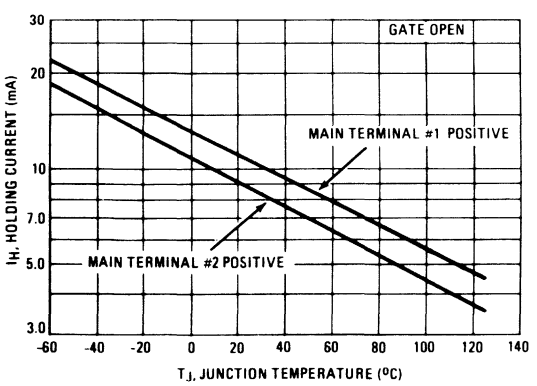


FIGURE 7 – MAXIMUM ALLOWABLE SURGE CURRENT

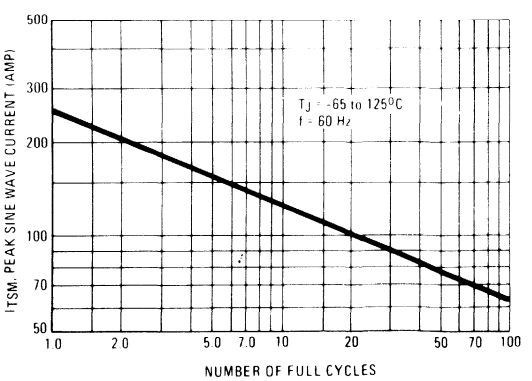
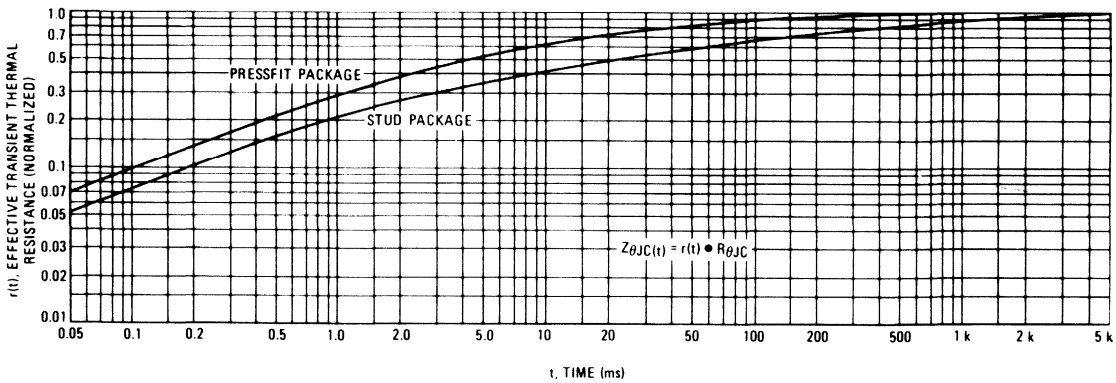


FIGURE 8 – TYPICAL THERMAL RESPONSE



3

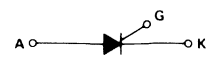
Silicon Controlled Rectifier
Reverse Blocking Triode Thyristor

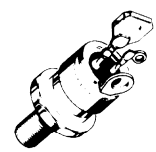
2N6167 thru 2N6170

SCRs
20 AMPERES RMS
100 thru 600 VOLTS

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 240 Amps
- Rugged Construction in Isolated Stud Package





CASE 311-02
STYLE 1

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Forward and Reverse Blocking Voltage, Note 1 (T_J = −40°C to +100°C) 2N6167	V_{DRM} or V_{RRM}	100	Volts
2N6168		200	
2N6169		400	
2N6170		600	
*Non-Repetitive Peak Reverse Blocking Voltage (t ≤ 5 ms) 2N6167	V_{RSM}	150	Volts
2N6168		250	
2N6169		450	
2N6170		650	
*Average Forward Current (T_C = −40 to +65°C)	$I_{T(AV)}$	13	Amps
(+85°C)		6.5	
*Peak Surge Current (One cycle, 60 Hz) (T_C = +65°C)	I_{TSM}	240	Amps
(1.5 ms pulse @ T_J = 100°C) Preceded and followed by no current or Voltage		560	
Circuit Fusing (T_J = −40 to +100°C) (t = 1 to 8.3 ms)	I^2t	235	A^2s
*Peak Gate Power	P_{GM}	5	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt

*Indicates JEDEC Registered Data. (cont.)

Note 1. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
*Peak Forward Gate Current	I_{GFM}	2	Amps
*Operating Junction Temperature Range	T_J	−40 to +100	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
*Stud Torque	—	30	in. lb.

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open, T_C = 100°C)	I_{DRM}, I_{RRM}				mA
2N6167		—	1	2	
2N6168		—	1	2.5	
2N6169		—	1	3	
2N6170		—	1	4	
(Rated V_{DRM} or V_{RRM}, gate open, T_C = 25°C) All Devices		—	—	10	μA
*Peak Forward "On" Voltage (I_{TM} = 41 A Peak)	V_{TM}	—	1.5	1.7	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 24 Ω) *T_C = −40°C	I_{GT}	—	—	75	mA
T_C = 25°C		—	2.1	40	
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 24 Ω) *T_C = −40°C	V_{GT}	—	0.8	2.5	Volts
T_C = 25°C		—	0.63	1.6	
Holding Current (V_D = 12 V, gate open, I_T = 200 mA) *T_C = −40°C	I_H	—	—	90	mA
T_C = 25°C		—	3.5	50	
*Turn-On Time (t_d + t_r) (I_{TM} = 41 Adc, V_D = Rated V_{DRM}, I_{GT} = 200 mAdc, Rise Time ≤ 0.05 μs, Pulse Width = 10 μs)	t_{on}	—	—	1	μs
Turn-Off Time	t_{off}				μs
(I_{TM} = 10 A, I_R = 10 A)		—	25	—	
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C)		—	40	—	
Forward Voltage Application Rate (T_J = 100°C, V_D = Rated V_{DRM})	dv/dt	—	50	—	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

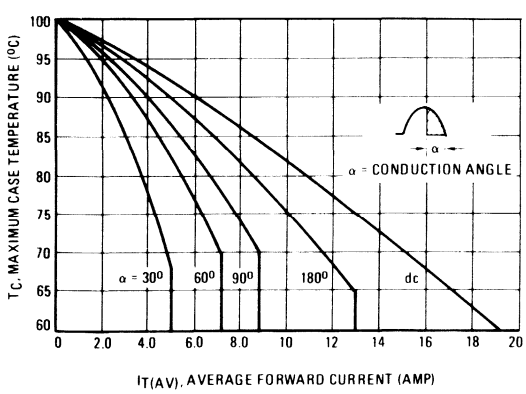


FIGURE 2 – POWER DISSIPATION

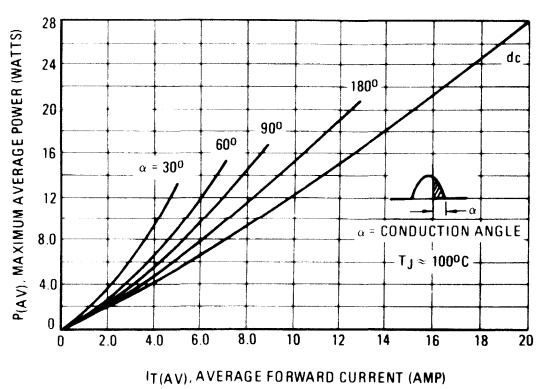


FIGURE 3 – MAXIMUM ON-STATE CHARACTERISTICS

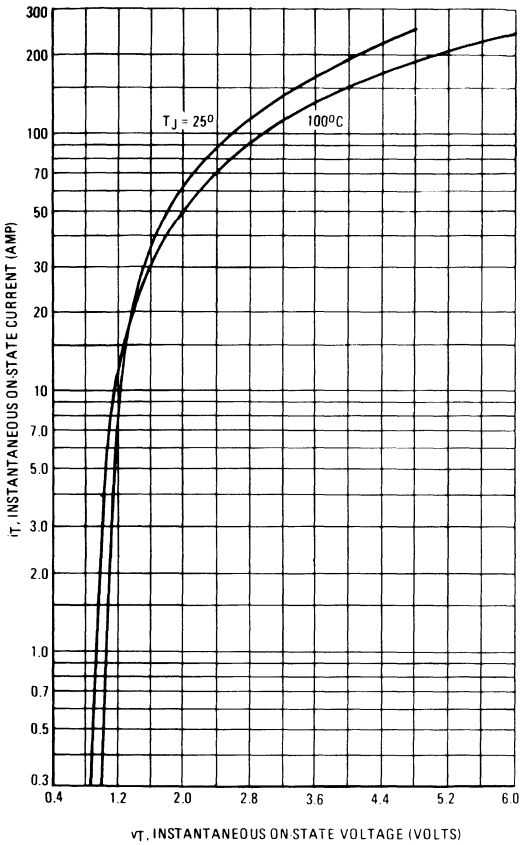


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

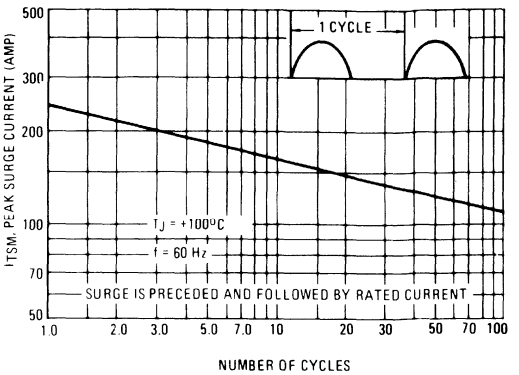


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

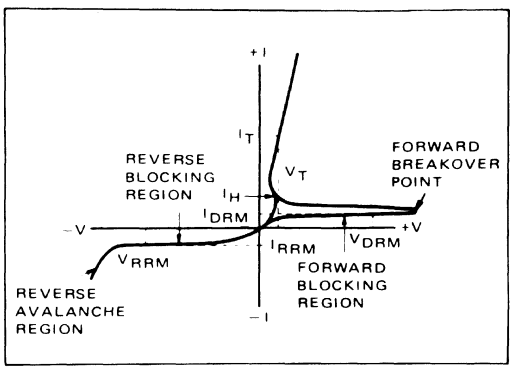


FIGURE 6 – THERMAL RESPONSE

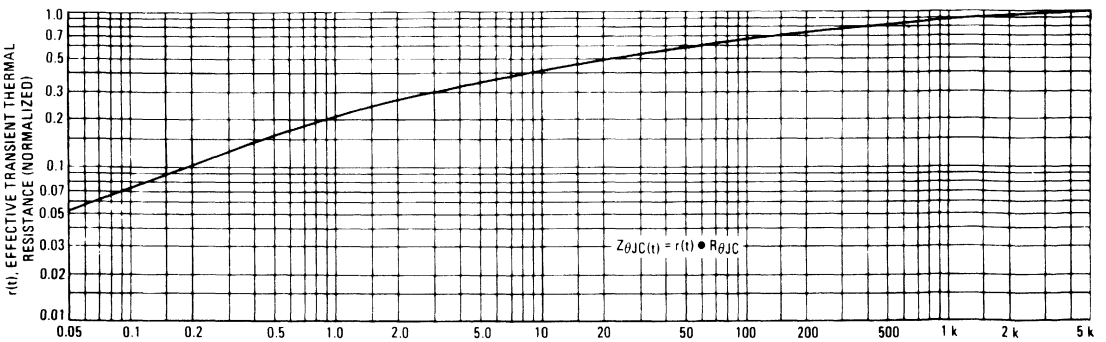


FIGURE 7 – TYPICAL GATE TRIGGER CURRENT

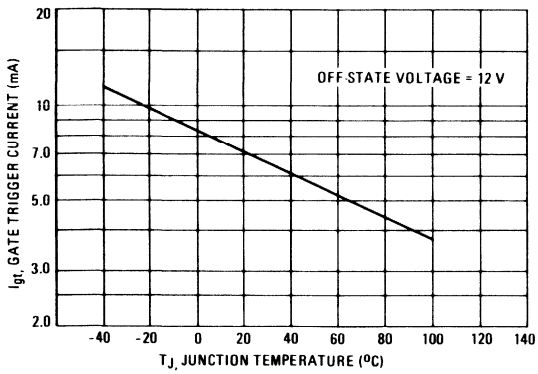


FIGURE 8 – TYPICAL GATE TRIGGER VOLTAGE

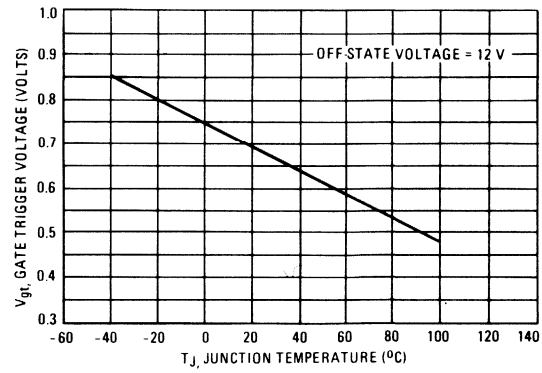
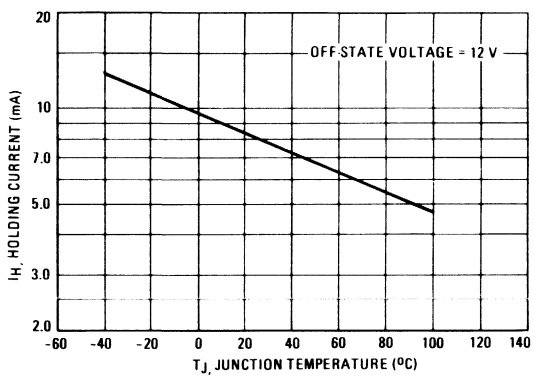


FIGURE 9 – TYPICAL HOLDING CURRENT



3

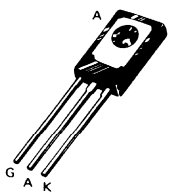
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristors

2N6237 thru 2N6241

SCRs
4 AMPERES RMS
50 thru 600 VOLTS

. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Recommended Electrical Replacement for C 106



CASE 77-05
(TO-225AA)
STYLE 2

3

MAXIMUM RATINGS (T_C = 110°C unless otherwise noted.)

Rating		Symbol	Value	Unit
*Repetitive Peak Forward and Reverse Blocking Voltage, Note 1		V_{DRM}		Volts
(1/2 Sine Wave)	2N6237	or	50	
(R_{GK} = 1000 ohms, T_C = −40 to +110°C)	2N6238	V_{RRM}	100	
	2N6239		200	
	2N6240		400	
	2N6241		600	
*Non-Repetitive Peak Reverse Blocking Voltage		V_{RSM}		Volts
(1/2 Sine Wave, R_{GK} = 1000 ohms,	2N6237		100	
T_C = −40 to +110°C)	2N6238		150	
	2N6239		250	
	2N6240		450	
	2N6241		650	
*Average On-State Current		$I_{T(AV)}$		Amps
(T_C = −40 to +90°C)			2.6	
(T_C = +100°C)			1.6	
*Surge On-State Current		I_{TSM}		Amps
(1/2 Sine Wave, 60 Hz, T_C = +90°C)			25	
(1/2 Sine Wave, 1.5 ms, T_C = +90°C)			35	
Circuit Fusing (T_C = −40 to +110°C, t = 1 to 8.3 ms)		I^2t	2.6	A^2s
*Peak Gate Power (Pulse Width = 10 μs, T_C = 90°C)		P_{GM}	0.5	Watt

*Indicates JEDEC Registered Data.

(cont.)

Note 1. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

MAXIMUM RATINGS — continued (T_C = 110°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Average Gate Power (t = 8.3 ms, T_C = 90°C)	$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current	I_{GM}	0.2	Amp
Peak Reverse Gate Voltage	V_{RGM}	6	Volts
*Operating Junction Temperature Range	T_J	−40 to +110	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque, Note 1	—	6	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	3	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	—	75	°C/W

*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C and R_{GK} = 1000 ohms unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_C = 25°C T_C = 110°C	I_{DRM}, I_{RRM}	— —	— —	10 200	μA μA
*Peak Forward "On" Voltage (I_{TM} = 8.2 A Peak, Pulse Width = 1 to 2 ms, 2% Duty Cycle)	V_{TM}	—	—	2.2	Volts
Gate Trigger Current (Continuous dc), Note 2 (V_{AK} = 12 Vdc, R_L = 24 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = −40°C)	I_{GT}	— —	— —	200 500	μA
Gate Trigger Voltage (Continuous dc) (Source Voltage = 12 V, R_S = 50 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = −40°C)	V_{GT}	—	—	1	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 Ohms, T_C = 110°C)	V_{GD}	0.2	—	—	Volts
Holding Current (V_{AK} = 12 Vdc, I_{GT} = 2 mA) T_C = 25°C *(Initiating On-State Current = 200 mA) T_C = −40°C	I_H	— —	— —	5 10	mA
*Total Turn-On Time (Source Voltage = 12 V, R_S = 6 k Ohms) (I_{TM} = 8.2 A, I_{GT} = 2 mA, Rated V_{DRM}) (Rise Time = 20 ns, Pulse Width = 10 μs)	t_{gt}	—	2	—	μs
Forward Voltage Application Rate (V_D = Rated V_{DRM}, T_C = 110°C)	dv/dt	—	10	—	V/μs

*Indicates JEDEC Registered Data.

Notes: 1. Torque rating applies with use of compression washer (B52200F006 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-209 B)

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C. For optimum results an activated flux (oxide removing) is recommended.

2. Measurement does not include R_{GK} current.

3

FIGURE 1 – MAXIMUM CASE TEMPERATURE

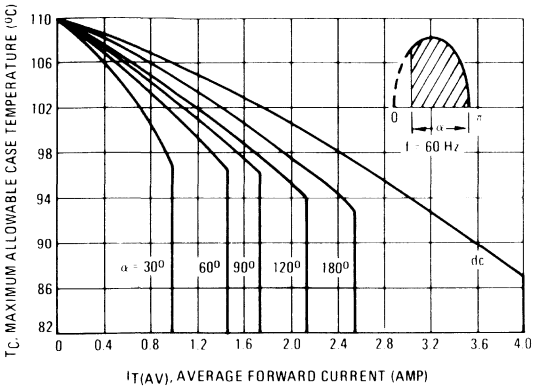
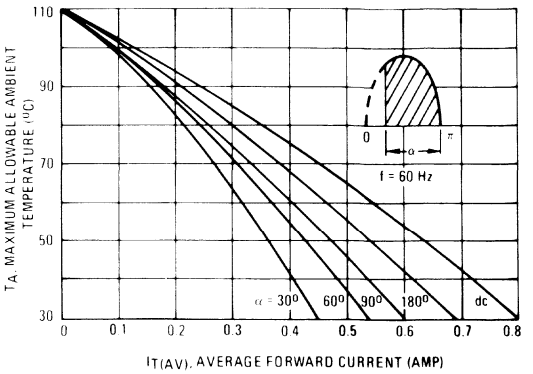


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE



3

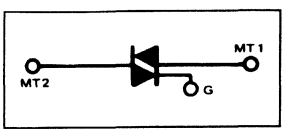
Triacs
Silicon Bidirectional Triode Thyristors

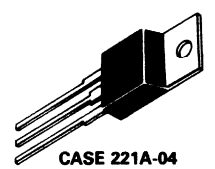
2N6342 thru 2N6349

TRIACs
8 AMPERES RMS
50 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342, 2N6343, 2N6344, 2N6345) or Four Modes (2N6346, 2N6347, 2N6348, 2N6349)
- For 400 Hz Operation, Consult Factory
- 12 Ampere Devices Available as 2N6342A thru 2N6349A





CASE 221A-04
(TO-220AB)
STYLE 4

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −40 to +100°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	2N6342, 2N6346 2N6343, 2N6347 2N6344, 2N6348 2N6345, 2N6349	V_{DRM}	200 400 600 800	Volts
*RMS On-State Current Full Cycle Sine Wave 50 to 60 Hz	(T_C = +80°C) (T_C = +90°C)	$I_{T(RMS)}$	8 4	Amps
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C) Preceded and followed by 10 Rated Current		I_{TSM}	100	Amps
Circuit Fusing (T_J = −40 to +100°C, t = 1 to 8.3 ms)		I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)		P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)		$P_{G(AV)}$	0.5	Watt
*Peak Gate Current		I_{GM}	2	Amps
*Peak Gate Voltage		V_{GM}	10	Volts
*Operating Junction Temperature Range		T_J	−40 to +125	°C
*Storage Temperature Range		T_{stg}	−40 to +150	°C

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 100°C		—	—	2	mA
*Peak On-State Voltage (I_{TM} = 11 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.3	1.55	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms) (Minimum Gate Pulse Width = 2 μs)	I_{GT}				mA
MT2(+), G(+) All Types		—	12	50	
MT2(+), G(−) 2N6346 thru 49		—	12	75	
MT2(−), G(−) All Types		—	20	50	
MT2(−), G(+) 2N6346 thru 49		—	35	75	
*MT2(+), G(+); MT2(−), G(−) T_C = −40°C All Types		—	—	100	
*MT2(+), G(−); MT2(−), G(+) T_C = −40°C 2N6346 thru 49		—	—	125	
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms) (Minimum Gate Pulse Width = 2 μs)	V_{GT}				Volts
MT2(+), G(+) All Types		—	0.9	2	
MT2(+), G(−) 2N6346 thru 49		—	0.9	2.5	
MT2(−), G(−) All Types		—	1.1	2	
MT2(−), G(+) 2N6346 thru 49		—	1.4	2.5	
*MT2(+), G(+); MT2(−), G(−) T_C = −40°C All Types		—	—	2.5	
*MT2(+), G(−); MT2(−), G(+) T_C = −40°C 2N6346 thru 49		—	—	3	
(V_D = Rated V_{DRM}, R_L = 10 k Ohms, T_J = 100°C)					
*MT2(+), G(+); MT2(−), G(−) All Types		0.2	—	—	
*MT2(+), G(−); MT2(−), G(−) 2N6346 thru 49		0.2	—	—	
*Holding Current (V_D = 12 Vdc, Gate Open) T_C = 25°C	I_H	—	6	40	mA
(I_T = 200 mA) *T_C = −40°C		—	—	75	
*Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 11 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1.5	2	μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 11 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs

*Indicates JEDEC Registered Data.

3

FIGURE 1 – RMS CURRENT DERATING

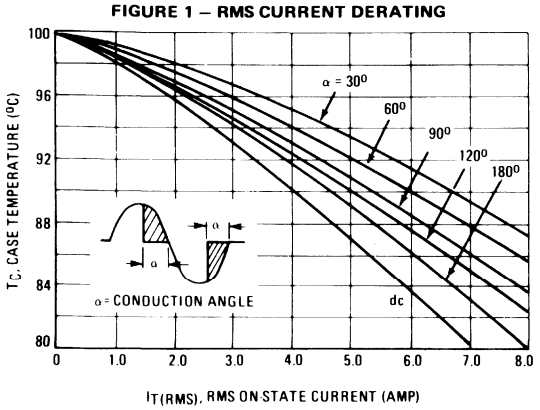


FIGURE 2 – ON-STATE POWER DISSIPATION

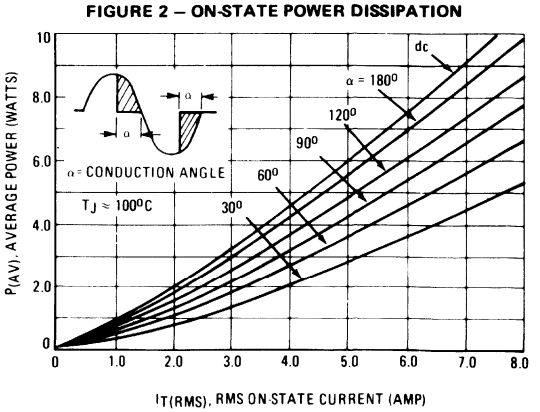


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

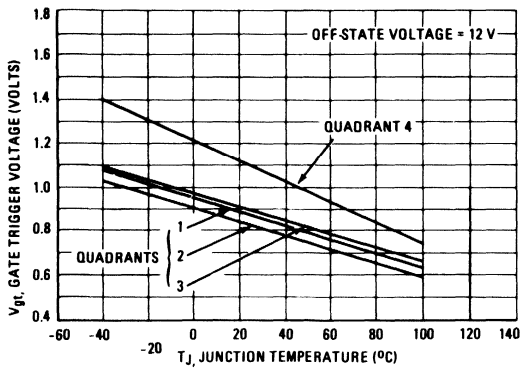


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

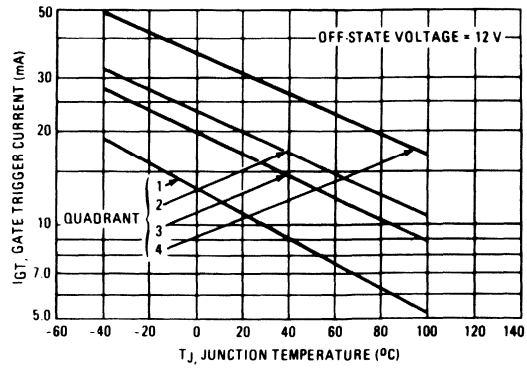


FIGURE 5 – ON-STATE CHARACTERISTICS

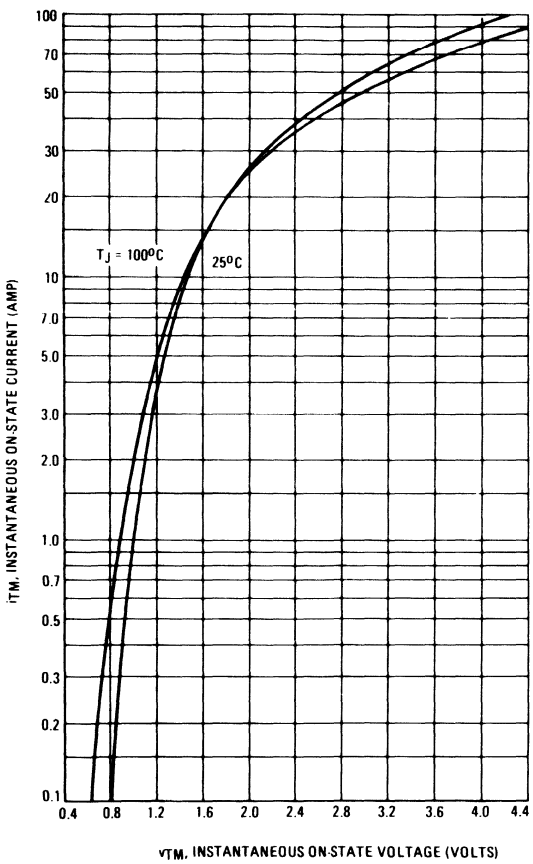


FIGURE 6 – TYPICAL HOLDING CURRENT

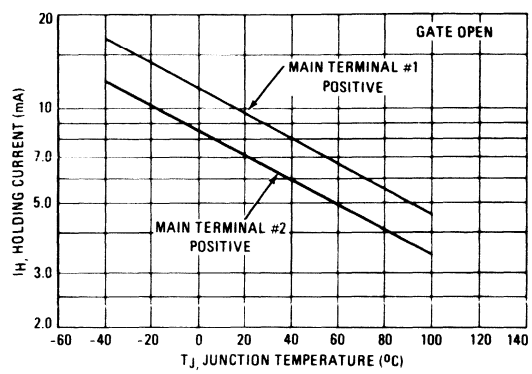


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

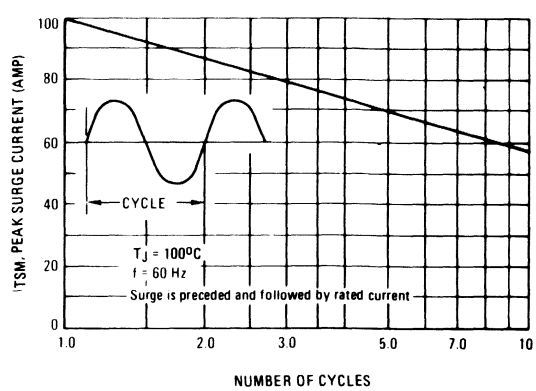


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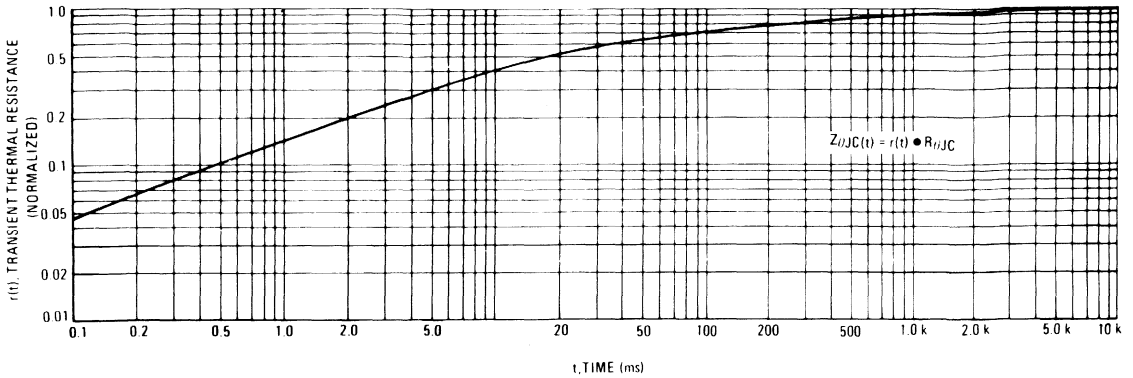
FIGURE 8 – TYPICAL THERMAL RESPONSE



3

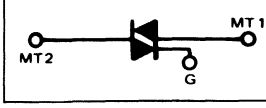
Triacs
Silicon Bidirectional Triode Thyristors

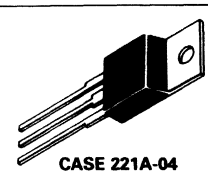
2N6342A thru 2N6349A

TRIACs
12 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342A, 2N6343A, 2N6344A, 2N6345A) or Four Modes (2N6346A, 2N6347A, 2N6348A, 2N6349A)
- For 400 Hz Operation, Consult Factory
- 8 Ampere Devices Available as 2N6342 thru 2N6349





CASE 221A-04
(TO-220AB)
STYLE 4

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −40 to +110°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	2N6342A, 2N6346A 2N6343A, 2N6347A 2N6344A, 2N6348A 2N6345A, 2N6349A	V_{DRM}	 200 400 600 800	Volts
*RMS On-State Current (Full Cycle Sine Wave 50 to 60 Hz)	(T_C = +80°C) (T_C = +95°C)	$I_{T(RMS)}$	12 6	Amps
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C) Preceded and Followed by Rated Current		I_{TSM}	120	Amps
Circuit Fusing (T_J = −40 to +110°C, t = 1 to 8.3 ms)		I^2t	59	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)		P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)		$P_{G(AV)}$	0.5	Watt
*Peak Gate Current		I_{GM}	2	Amps
*Peak Gate Voltage		V_{GM}	±10	Volts
*Operating Junction Temperature Range		T_J	−40 to +125	°C
*Storage Temperature Range		T_{stg}	−40 to +150	°C

*Indicates JEDEC Registered Data.

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 110°C		—	—	2	mA
*Peak On-State Voltage (Either Direction) (I_{TM} = 17 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.3	1.75	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	I_{GT}				mA
MT2(+), G(+) All Types		—	6	50	
MT2(+), G(−) 2N6346A thru 2N6349A		—	6	75	
MT2(−), G(−) All Types		—	10	50	
MT2(−), G(+) 2N6346A thru 2N6349A		—	25	75	
*MT2(+), G(+); MT2(−), G(−) T_C = −40°C All Types		—	—	100	
*MT2(+), G(−); MT2(−), G(+) T_C = −40°C 2N6346A thru 2N6349A		—	—	125	
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 ohms)	V_{GT}				Volts
MT2(+), G(+) All Types		—	0.9	2	
MT2(+), G(−) 2N6346A thru 2N6349A		—	0.9	2.5	
MT2(−), G(−) All Types		—	1.1	2	
MT2(−), G(+) 2N6346A thru 2N6349A		—	1.4	2.5	
*MT2(+), G(+); MT2(−), G(−) T_C = −40°C All Types		—	—	2.5	
*MT2(+), G(−); MT2(−), G(+) T_C = −40°C 2N6346A thru 2N6349A		—	—	3	
(V_D = Rated V_{DRM}, R_L = 10 k ohms, T_J = 100°C)					
*MT2(+), G(+); MT2(−), G(−) All Types		0.2	—	—	
*MT2(+), G(−); MT2(−), G(−) 2N6346A thru 2N6349A		0.2	—	—	
Holding Current (Either Direction) (V_D = 12 Vdc, Gate Open) T_C = 25°C	I_H	—	6	40	mA
(I_T = 200 mA) *T_C = −40°C		—	—	75	
*Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 17 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1.5	2	μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 17 A, Commutating di/dt = 6.5 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs

*Indicates JEDEC Registered Data.

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FIGURE 1 – RMS CURRENT DERATING

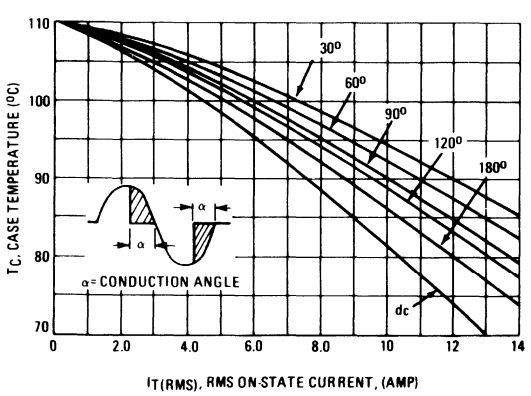

FIGURE 2 – ON-STATE POWER DISSIPATION

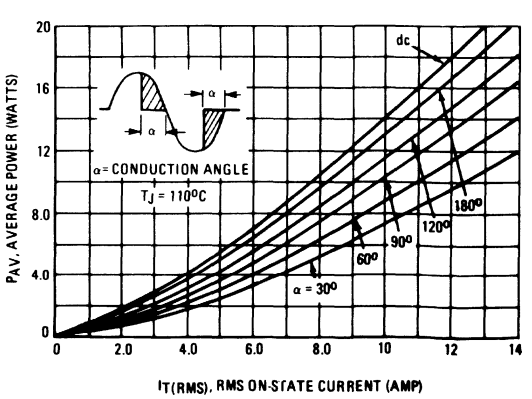

FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

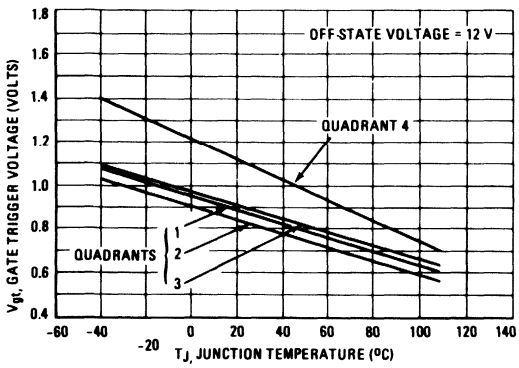

FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

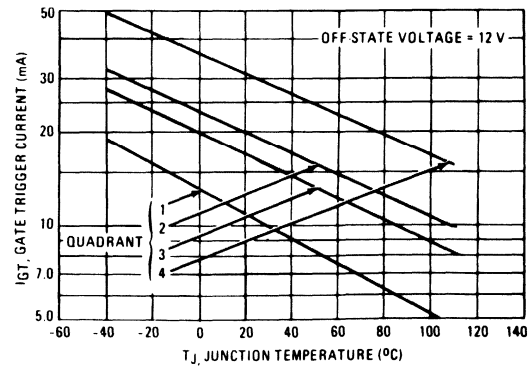

FIGURE 5 – ON-STATE CHARACTERISTICS

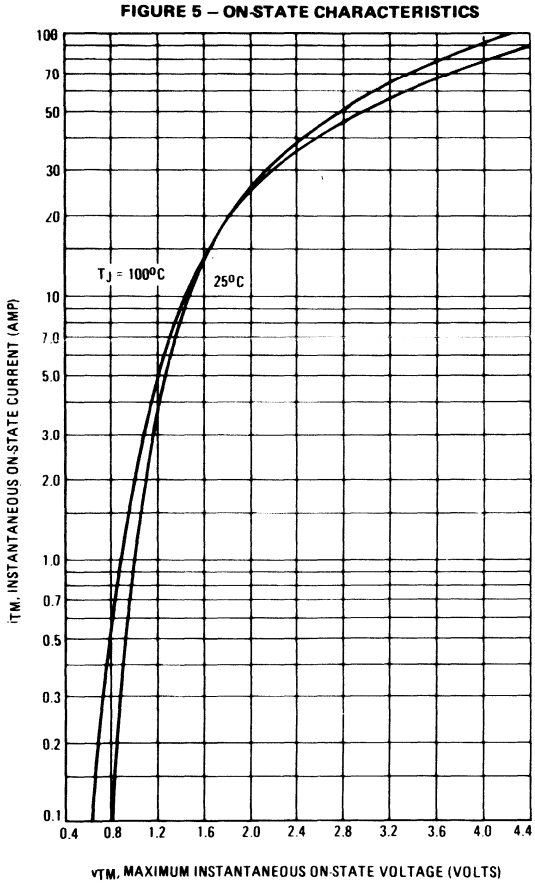

FIGURE 6 – TYPICAL HOLDING CURRENT

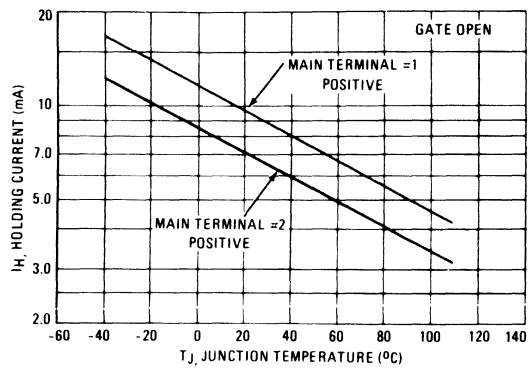

FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

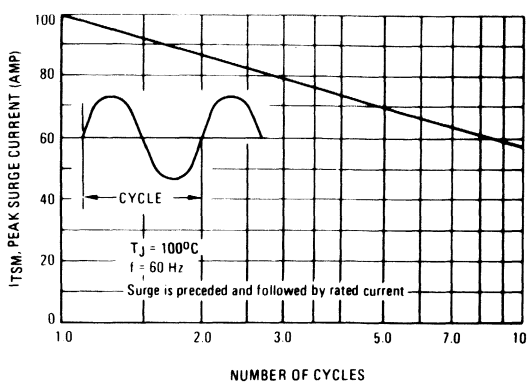

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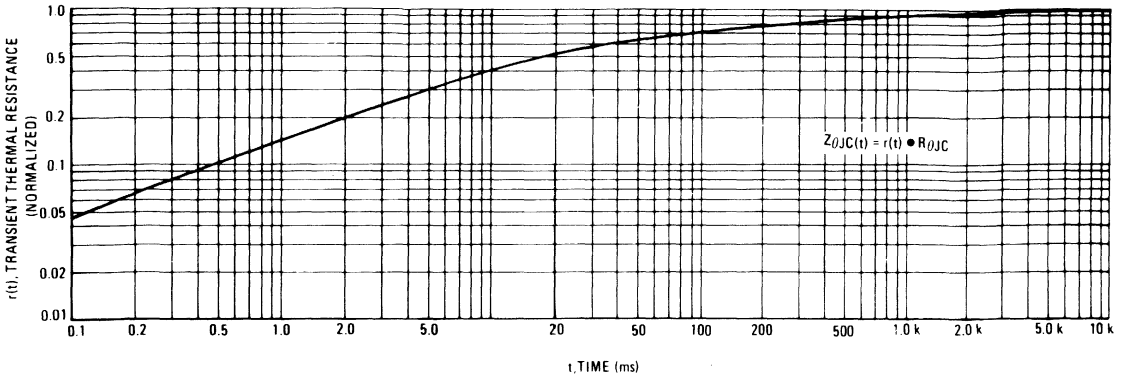
FIGURE 8 – TYPICAL THERMAL RESPONSE



3

Silicon Controlled Rectifiers

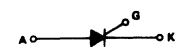
Reverse Blocking Triode Thyristors

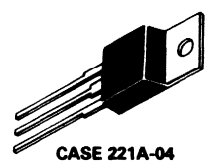
2N6394 thru 2N6399

SCRs
12 AMPERES RMS
50 thru 800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts





CASE 221A-04
(TO-220AB)
STYLE 3

***MAXIMUM RATINGS**

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (T_J = −40 to 125°C)	2N6394 2N6395 2N6396 2N6397 2N6398 2N6399	V_{RRM} or V_{DRM}	50 100 200 400 600 800	Volts
RMS On-State Current (All Conduction Angles)	T_C = 90°C	$I_{T(RMS)}$	12	Amps
Peak Non-Repetitive Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = 125°C)		I_{TSM}	100	Amps
Circuit Fusing (T_J = −40 to +125°C, t = 1 to 8.3 ms)		I^2t	40	A^2s
Forward Peak Power		P_{GM}	20	Watts
Forward Average Gate Power		$P_{G(AV)}$	0.5	Watt

*Indicates JEDEC Registered Data.

(cont.)

3

***MAXIMUM RATINGS — continued**

Rating	Symbol	Value	Unit
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	— —	— —	10 2	μA mA
*Forward "On" Voltage (I_{TM} = 24 A Peak)	V_{TM}	—	1.7	2.2	Volts
*Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	I_{GT}	—	5	30	mA
*Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms) (V_D = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GT} V_{GD}	— 0.2	0.7 —	1.5 —	Volts
*Holding Current (V_D = 12 Vdc)	I_H	—	6	40	mA
Turn-On Time (I_{TM} = 12 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	—	1	2	μs
Turn-Off Time (V_D = Rated V_{DRM}) (I_{TM} = 12 A, I_R = 12 A) (I_{TM} = 12 A, I_R = 12 A, T_J = 125°C)	t_q	— —	15 35	— —	μs
Critical Rate-of-Rise of Off-State Voltage Exponential (V_D = Rated V_{DRM}, T_J = 125°C)	dv/dt	—	50	—	V/μs

*Indicates JEDEC Registered Data.

3

FIGURE 1 – CURRENT DERATING

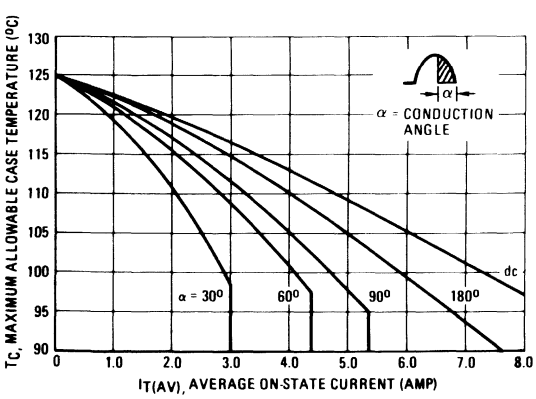


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

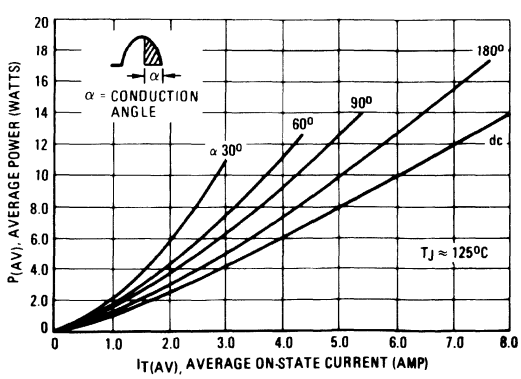


FIGURE 3 – ON-STATE CHARACTERISTICS

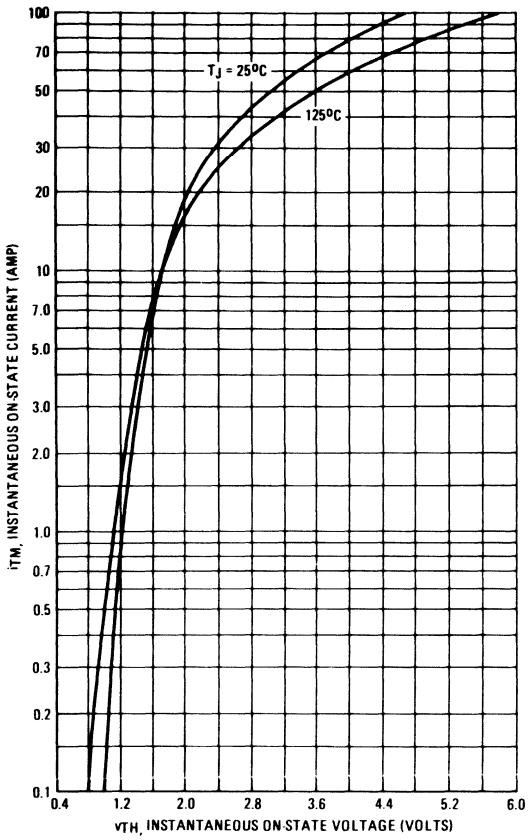


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

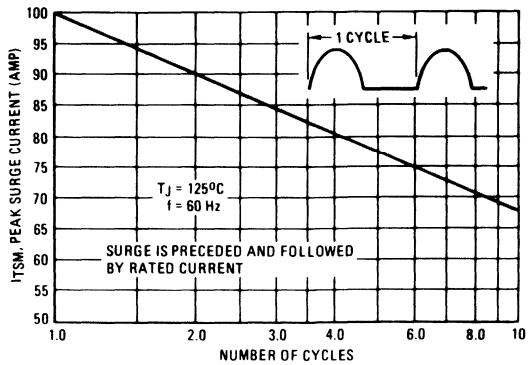
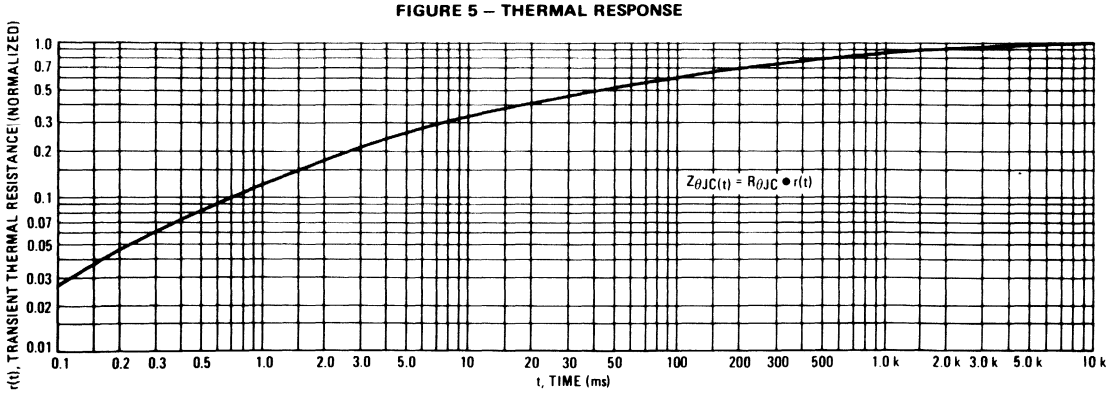


FIGURE 5 – THERMAL RESPONSE



3

TYPICAL CHARACTERISTICS

FIGURE 6 – PULSE TRIGGER CURRENT

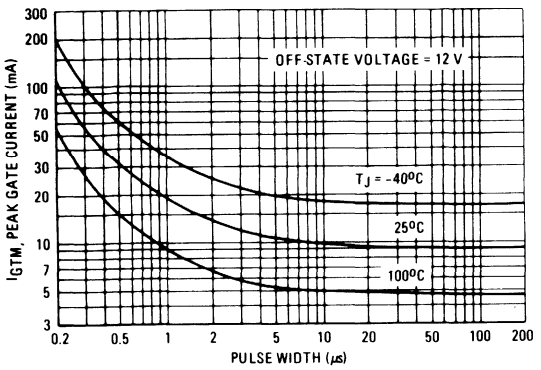


FIGURE 7 – GATE TRIGGER CURRENT

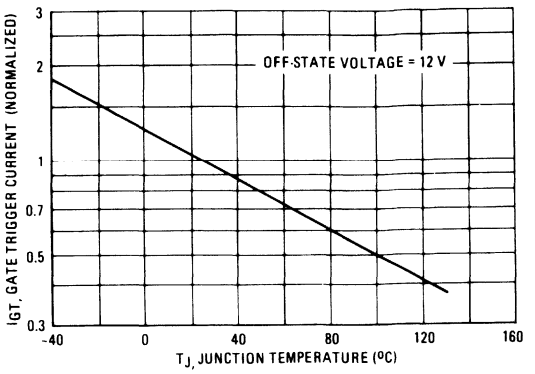


FIGURE 8 – GATE TRIGGER VOLTAGE

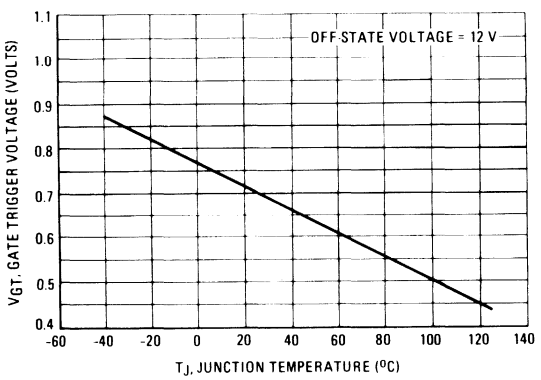
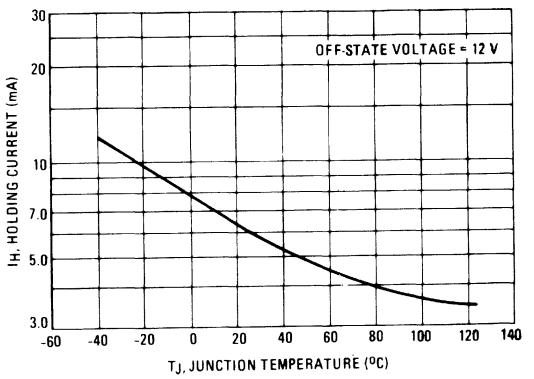


FIGURE 9 – HOLDING CURRENT



3

Silicon Controlled Rectifiers

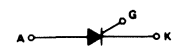
Reverse Blocking Triode Thyristors

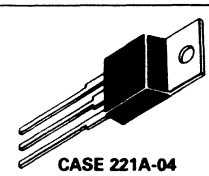
2N6400 thru 2N6405

SCRs
16 AMPERES RMS
50 thru 800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts





CASE 221A-04
(TO-220AB)
STYLE 3

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage	V_{RRM} or V_{DRM}		Volts
2N6400		50	
2N6401		100	
2N6402		200	
2N6403		400	
2N6404		600	
2N6405		800	
RMS On-State Current, T_C = 90°C	$I_{T(RMS)}$	16	Amps
Average On-State Current	$I_{T(AV)}$	10	Amps
Peak Non-Repetitive Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	160	Amps
Circuit Fusing (T_J = −40 to +125°C, t = 1 to 8.3 ms)	I^2t	100	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt

*Indicates JEDEC Registered Data.

(cont.)

***MAXIMUM RATINGS — continued**

Rating	Symbol	Value	Unit
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
*Peak On-State Voltage (I_{TM} = 32 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.7	Volts
*Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 50 Ohms)	I_{GT}	—	5	30	mA
*Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 50 Ohms) T_C = 25°C	V_{GT}	—	0.7	1.5	Volts
T_C = −40°C		—	—	2.5	
(V_D = Rated V_{DRM}, R_L = 50 Ohms) T_C = +125°C		0.2	—	—	
*Holding Current (V_D = 12 Vdc) T_C = 25°C	I_H	—	6	40	mA
*T_C = −40°C		—	—	60	
Turn-On Time (I_{TM} = 16 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	—	1	—	μs
Turn-Off Time (I_{TM} = 16 A, I_R = 16 A, V_D = Rated V_{DRM}) T_C = 25°C	t_q	—	15	—	μs
T_J = +125°C		—	35	—	
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform) T_J = +125°C	dv/dt	—	50	—	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

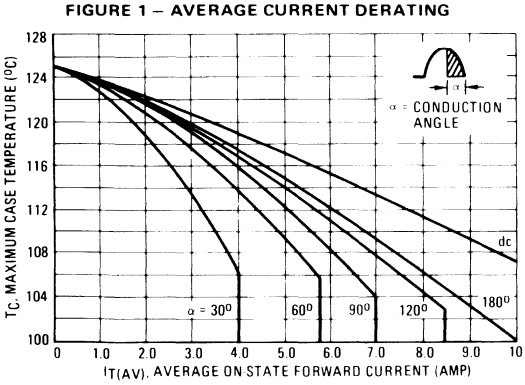


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

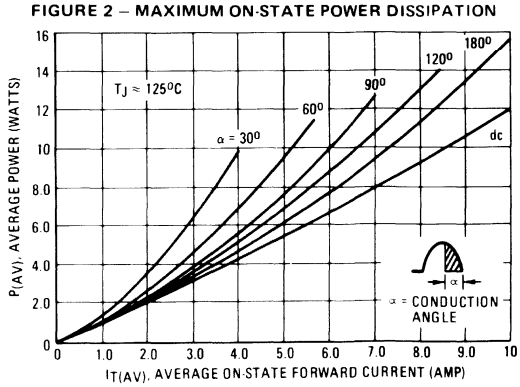


FIGURE 3 – ON-STATE CHARACTERISTICS

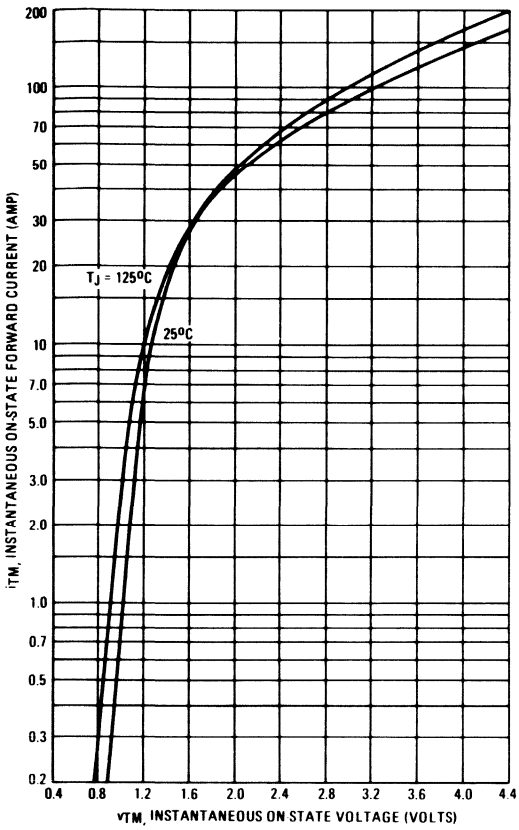


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

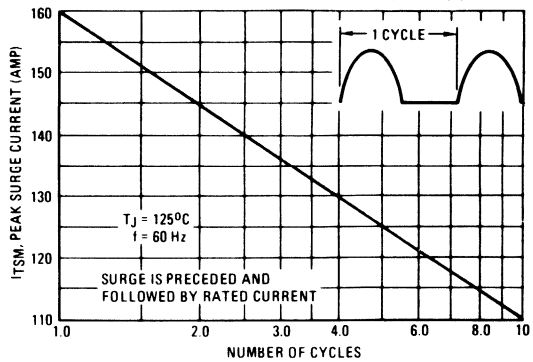


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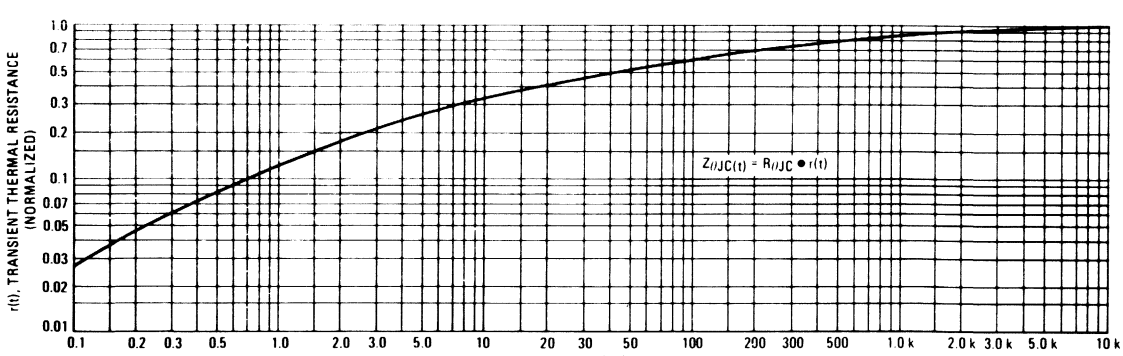
FIGURE 5 – THERMAL RESPONSE



TYPICAL TRIGGER CHARACTERISTICS

FIGURE 6 – PULSE TRIGGER CURRENT

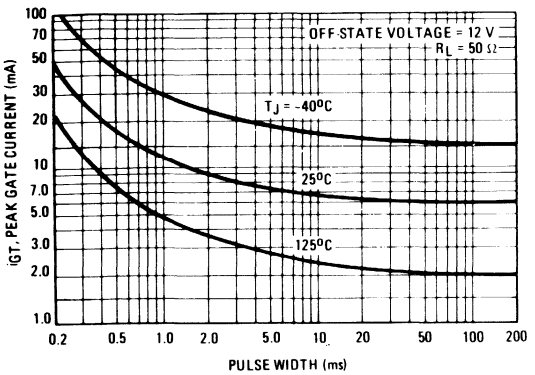


FIGURE 7 – GATE TRIGGER CURRENT

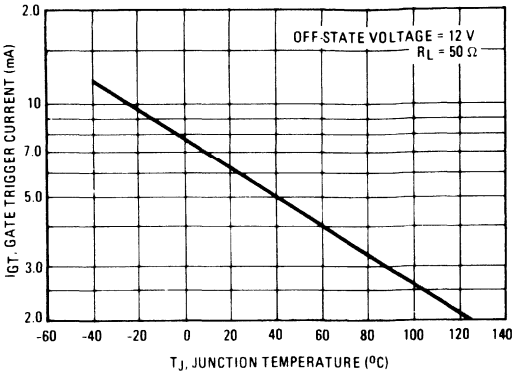


FIGURE 8 – GATE TRIGGER VOLTAGE

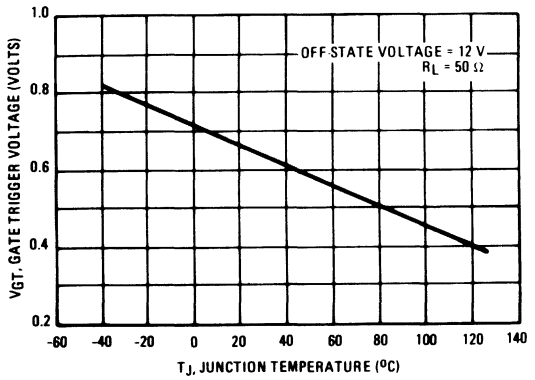
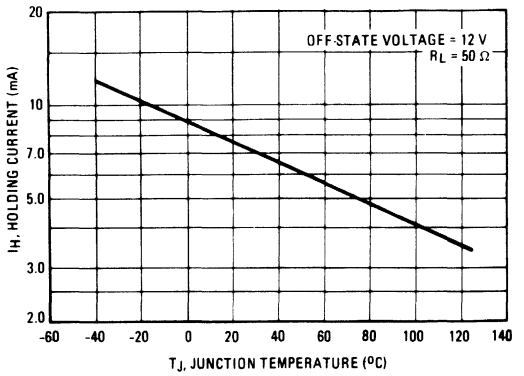


FIGURE 9 – HOLDING CURRENT



3

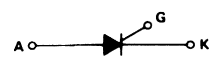
Thyristors
Silicon Controlled Rectifiers

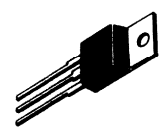
2N6504 thru 2N6509

SCRs
25 AMPERES RMS
50 thru 800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supply crowbar circuits.

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts
- 300 A Surge Current Capability





CASE 221A-04
(TO-220AB)
STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Reverse Blocking Voltage, Note 1	V_{RRM}		Volts
2N6504		50	
2N6505		100	
2N6506		200	
2N6507		400	
2N6508		600	
2N6509		800	
Forward Current (T_C = 85°C)	$I_{T(RMS)}$	25	Amps
(All Conduction Angles)	$I_{T(AV)}$	16	
Peak Non-Repetitive Surge Current — 8.3 ms	I_{TSM}	300	Amps
(1/2 Cycle, Sine Wave) 1.5 ms		350	

*Indicates JEDEC Registered Data.

(cont.)

Note 1. V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

3

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (T_J = 125°C)		V_{DRM}				Volts
	2N6504		50	—	—	
	2N6505		100	—	—	
	2N6506		200	—	—	
	2N6507		400	—	—	
	2N6508		600	—	—	
	2N6509		800	—	—	
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM})	T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
	T_J = 125°C		—	—	2	mA
*Forward "On" Voltage, Note 1 (I_{TM} = 50 A)		V_{TM}	—	—	1.8	Volts
*Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	—	—	40	mA
	T_C = −40°C		—	25	75	
*Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms, T_C = −40°C)		V_{GT}	—	1	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	—	—	Volts
*Holding Current (Anode Voltage = 12 Vdc, T_C = −40°C)		I_H	—	35	40	mA
*Turn-On Time (I_{TM} = 25 A, I_{GT} = 50 mAdc)		t_{gt}	—	1.5	2	μs
Turn-Off Time (V_{DRM} = rated voltage)		t_q				μs
(I_{TM} = 25 A, I_R = 25 A)			—	15	—	
(I_{TM} = 25 A, I_R = 25 A, T_J = 125°C)			—	35	—	
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)		dv/dt	—	50	—	V/μs

*Indicates JEDEC Registered Data.
Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 — AVERAGE CURRENT DERATING

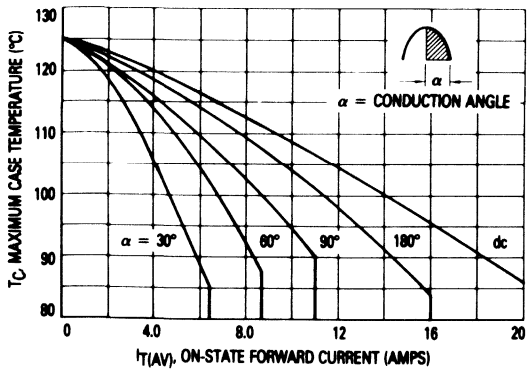


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION

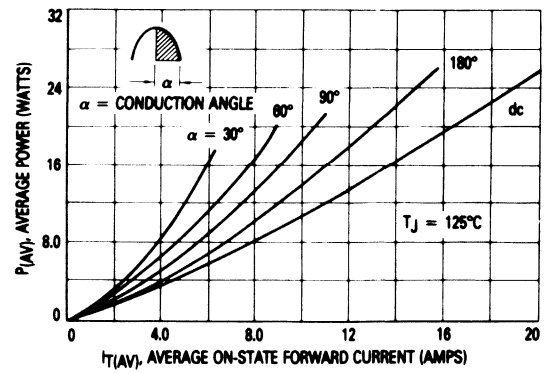


FIGURE 3 — MAXIMUM FORWARD VOLTAGE

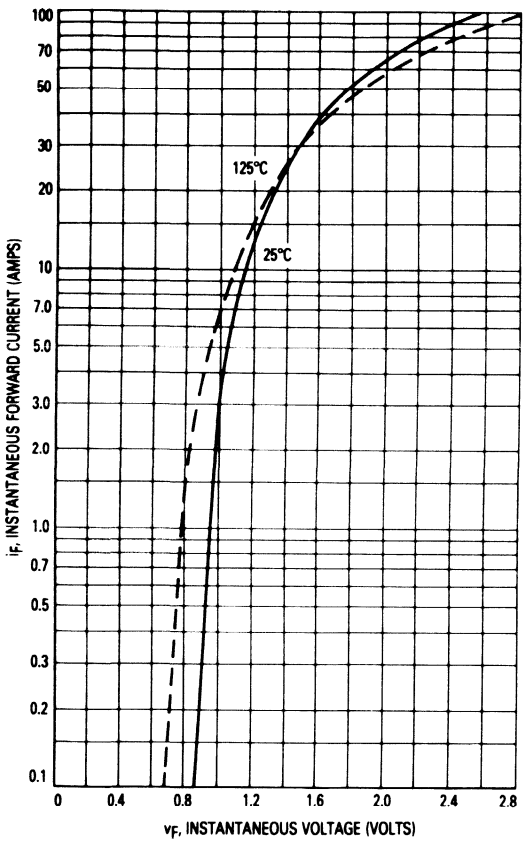


FIGURE 4 — MAXIMUM NON-REPETITIVE SURGE CURRENT

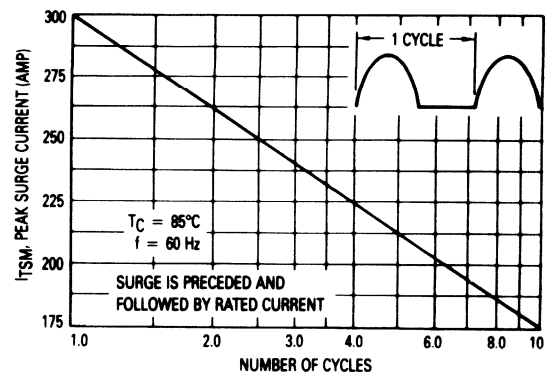


FIGURE 5 — CHARACTERISTICS AND SYMBOLS

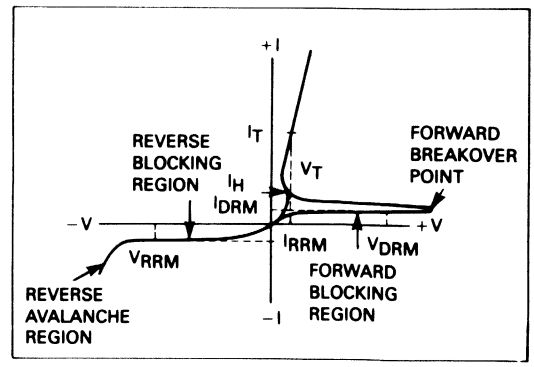


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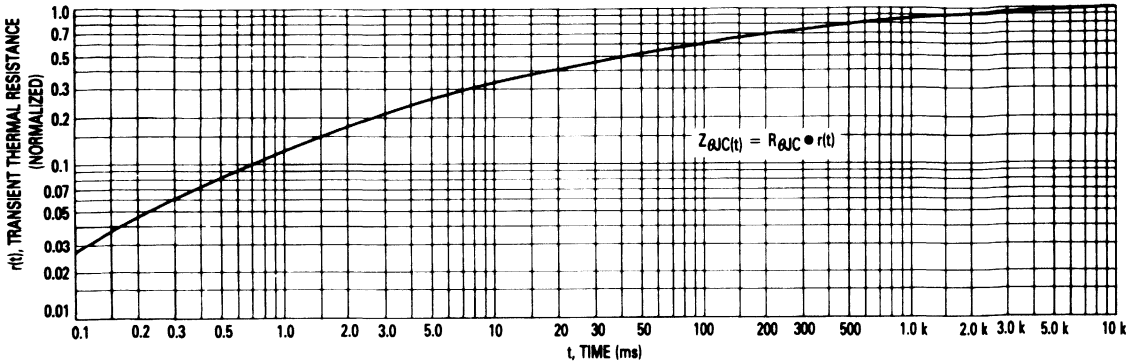
FIGURE 6 — THERMAL RESPONSE



TYPICAL TRIGGER CHARACTERISTICS

FIGURE 7 — GATE TRIGGER CURRENT

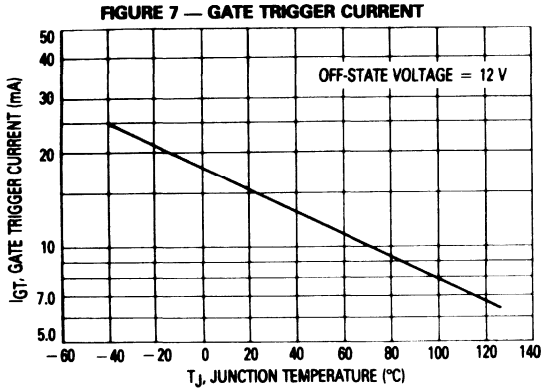


FIGURE 8 — GATE TRIGGER VOLTAGE

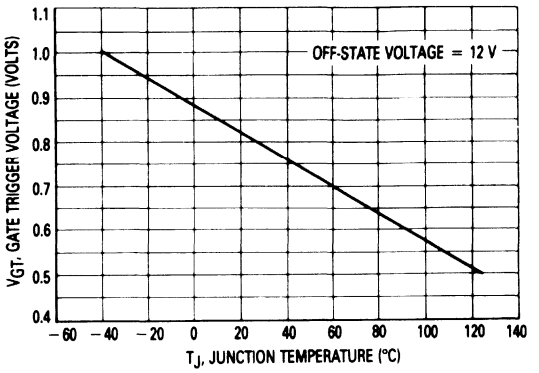
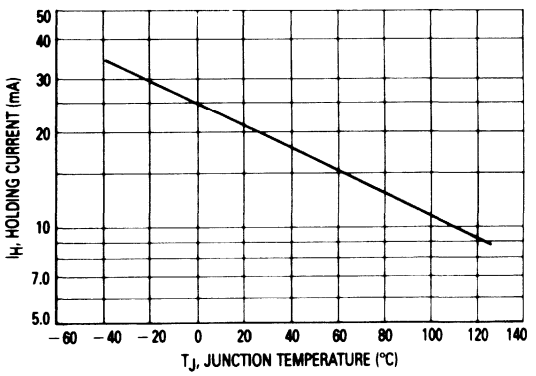


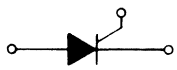
FIGURE 9 — HOLDING CURRENT



3

MOTOROLA

BRX 44 thru 49



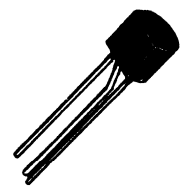
PLASTIC SILICON CONTROLLED RECTIFIERS

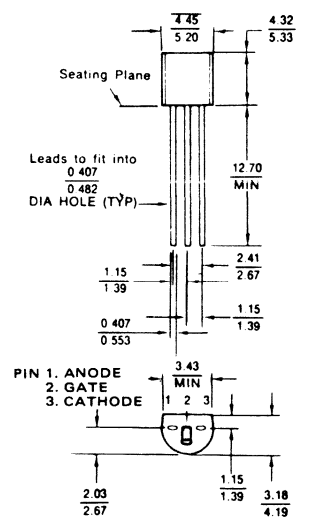
PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Glass-Passivated Surface for Reliability and Uniformity

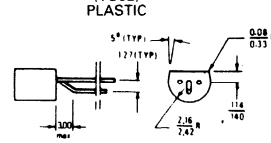
PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
30 TO 400 VOLTS





CASE 29-02 STYLE 3
(TO92)
PLASTIC



TO-18 configuration
Dimensions in millimeters

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage	V_{RRM}		Volts
BRX44		30	
BRX45		60	
BRX46		100	
BRX47		200	
BRX48		300	
BRX49		400	
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	8.0	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
Peak Gate Power – Forward, T_A = 25°C	P_{GM}	0.1	Watt
Peak Gate Current Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage – Reverse	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Lead Solder Temperature (<1.5mm from case, 10 s max.)		+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

3

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)	BRX44	V_{RRM}	30		Volts]
	BRX45		60		
	BRX46		100		
	BRX47		200		
	BRX48		300		
	BRX49		400		
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 1) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 2) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–	0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = –40C		–	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C		0.1	–	
Holding Current	T_C = 25°C	I_H	–	5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = –40°C		–	10	

NOTE:
1. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
2. R_{GK} current is not included in measurement.

3

FIGURE 1 – CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

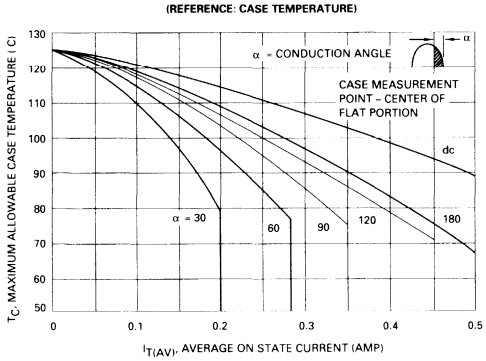
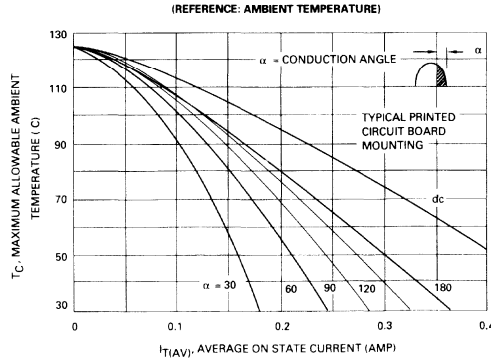
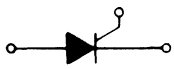


FIGURE 2 – CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)



MOTOROLA

BRY 55-30 thru 600



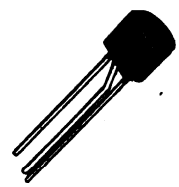
PLASTIC SILICON CONTROLLED RECTIFIERS

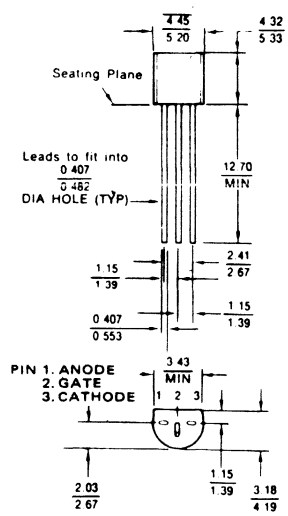
PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Glass-Passivated Surface for Reliability and Uniformity

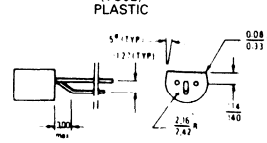
PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
30 TO 400 VOLTS





CASE 29-02 STYLE 3
(TO92)
PLASTIC



TO-18 configuration
Dimensions in millimeters

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage	V_{RRM}		Volts
Marking: BRY55-1 . . . BRY55-30		30	
-2 . . . BRY55-60		60	
-3 . . . BRY55-100		100	
-4 . . . BRY55-200		200	
-5 . . . BRY55-300		300	
-6 . . . BRY55-400		400	
-7 . . . BRY55-500		500	
-8 . . . BRY55-600		600	
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	8.0	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
Peak Gate Power – Forward, T_A = 25°C	P_{GM}	0.1	Watt
Peak Gate Current Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage – Reverse	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rated VRRM and VDRM	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C
Lead Solder Temperature (<1.5mm from case, 10 s max.)		+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

3

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)		V_{RRM}			Volts
	BRY55-30		30		
	BRY55-60		60		
	BRY55-100		100		
	BRY55-200		200		
	BRY55-300		300		
	BRY55-400		400		
	BRY55-500		500		
	BRY55-600		600		
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 1) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 2) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–	0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = –40C		–	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C		0.1	–	
Holding Current	T_C = 25°C	I_H	–	5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = –40°C		–	10	

NOTE:
1. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
2. R_{GK} current is not included in measurement.
3. MARKING: BRY55-30 = BRY55-1
   BRY55-60 = BRY55-2
   BRY55-100 = BRY55-3
   BRY55-200 = BRY55-4
   BRY55-300 = BRY55-5
   BRY55-400 = BRY55-6
   BRY55-500 = BRY55-7
   BRY55-600 = BRY55-8

3

FIGURE 1 – CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

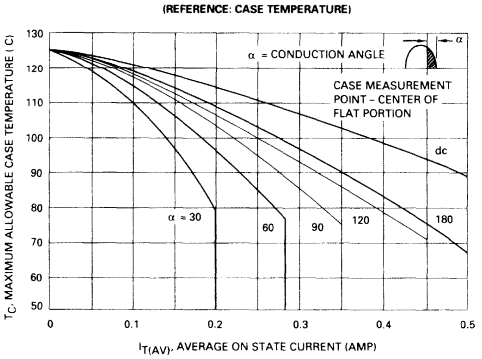
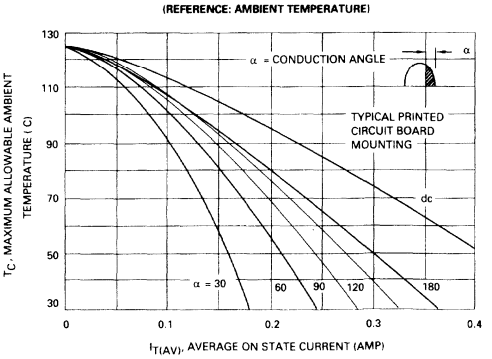


FIGURE 2 – CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)



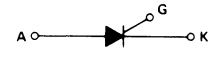
Silicon Controlled Rectifier
Reverse Blocking Triode Thyristors

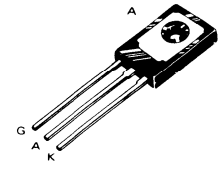
C106 Series

SCRs
4 AMPERES RMS
50 thru 600 VOLTS

. . . Glassivated PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Glassivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability





CASE 77-05
(TO-225AA)
STYLE 2

3

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (R_{GK} = 1 kΩ) (T_C = −40° to 110°C)	C106F C106A C106B C106D C106M	V_{DRM} or V_{RRM}	50 100 200 400 600	Volts
RMS Forward Current (All Conduction Angles)		$I_{T(RMS)}$	4	Amps
Average Forward Current (T_A = 30°C)		$I_{T(AV)}$	2.55	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, 60 Hz, T_J = −40 to +110°C)		I_{TSM}	20	Amps
Circuit Fusing t > 1.5 ms		I^2t	0.5	A^2s
Peak Gate Power		P_{GM}	0.5	Watt
Average Gate Power		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GFM}	0.2	Amp

(cont.)

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Peak Reverse Gate Voltage	V_{GRM}	6	Volts
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque, Note 1	—	6	in. lb.

Note 1. Torque rating applies with use of compression washer (B52200F006). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C. For optimum results, an activated flux (oxide removing) is recommended.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, R_{GK} = 1000 Ohms) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 110°C		—	—	100	μA
Forward "On" Voltage (I_{FM} = 1 A Peak)	V_{TM}	—	—	2.2	Volts
Gate Trigger Current (Continuous dc)	I_{GT}				μA
(V_{AK} = 6 Vdc, R_L = 100 Ohms)		—	30	200	
(V_{AK} = 6 Vdc, R_L = 100 Ohms, T_C = −40°C)		—	75	500	
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_{AK} = 6 Vdc, R_L = 100 Ohms, R_{GK} = 1000 Ohms) T_J = 25°C		0.4	—	0.8	
(V_{AK} = Rated V_{DRM}, R_L = 3000 Ohms,		0.5	—	1	
R_{GK} = 1000 Ohms, T_J = 110°C) T_J = −40°C		0.2	—	—	
Holding Current (T_J = 25°C	I_{HX}	0.3	—	3	mA
(V_D = 12 Vdc, R_{GK} = 1000 Ohms) T_J = −40°C		0.4	—	6	
T_J = +110°C		0.14	—	2	
Forward Voltage Application Rate (T_J = 110°C, R_{GK} = 1000 Ohms, V_D = Rated V_{DRM})	dv/dt	—	8	—	V/μs
Turn-On Time	t_{gt}	—	1.2	—	μs
Turn-Off Time	t_q	—	40	—	μs

3

FIGURE 1 – AVERAGE CURRENT DERATING

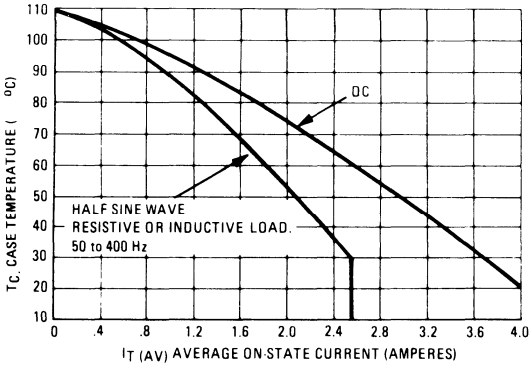
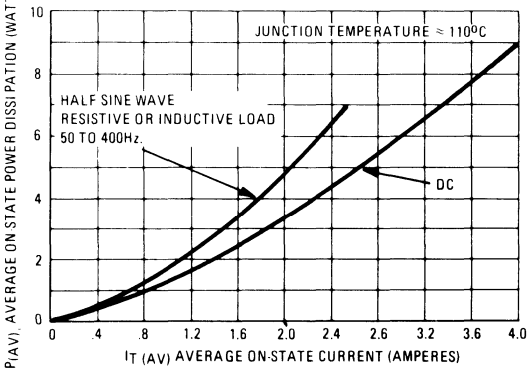
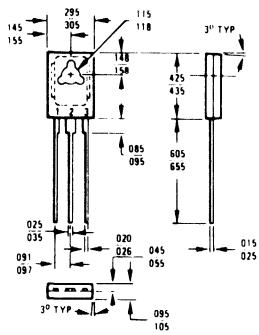


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

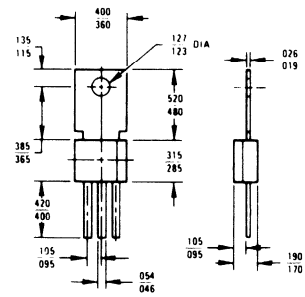


Package Interchangeability

The dimensional diagrams below compare the critical dimensions of the Motorola C-106 package with competitive devices. It has been demonstrated that the smaller dimensions of the Motorola package make it compatible in most lead-mount and chassis-mount applications. The user is advised to compare all critical dimensions for mounting compatibility.



Motorola C-106 Package



Competitive C-106 Package

3

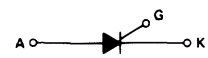
Silicon Controlled Rectifier
Reverse Blocking Triode Thyristor

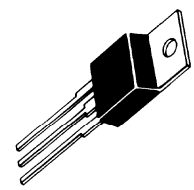
C122 Series

SCRs
8 AMPERES RMS
50 thru 800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 600 Volts
- Different Lead Form Configurations, Suffix (2) thru (6) available, see Thyristor Selection Guide for Information





CASE 221A-04
(TO-220AB)
STYLE 3

3

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 Repetitive Peak Reverse Voltage		V_{DRM} V_{RRM}		Volts
	C122F		50	
	C122A		100	
	C122B		200	
	C122D		400	
	C122M		600	
	C122N		800	
Non-Repetitive Peak Reverse Voltage		V_{RSM}		Volts
	C122F		75	
	C122A		200	
	C122B		300	
	C122D		500	
	C122M		700	
	C122N		800	
Forward Current RMS (All Conduction Angles)	$T_C \leq 75°C$	$I_{T(RMS)}$	8	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)		I_{TSM}	90	Amps
Circuit Fusing Considerations (t = 8.3 ms)		I^2t	34	A^2s

Note 1. V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. (cont.) Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Forward Peak Gate Power (t = 10 μs)	P_{GM}	5	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = 100°C		—	—	0.5	mA
Peak On-State Voltage, Note 1 (I_{TM} = 16 A Peak, T_C = 25°C)	V_{TM}	—	—	1.83	Volts
Gate Trigger Current (Continuous dc)	I_{GT}				mA
(V_D = 6 V, R_L = 91 Ohms, T_C = 25°C)		—	—	25	
(V_D = 6 V, R_L = 45 Ohms, T_C = −40°C)		—	—	40	
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_D = 6 V, R_L = 91 Ohms, T_C = 25°C)		—	—	1.5	
(V_D = 6 V, R_L = 45 Ohms, T_C = −40°C)		—	—	2	
(V_D = Rated V_{DRM}, R_L = 1000 Ohms, T_C = 100°C)		0.2	—	—	
Holding Current (V_D = 24 Vdc, I_T = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7 V, 20 Ohms)	I_H				mA
T_C = 25°C		—	—	30	
T_C = −40°C		—	—	60	
Turn-Off Time (V_D = Rated V_{DRM}) (I_{TM} = 8 A, I_R = 8 A)	t_q	—	50	—	μs
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Linear, T_C = 100°C)	dv/dt	—	50	—	V/μs

Note 1. Pulse Test: Pulse Width = 1 ms, Duty Cycle ≤ 2%.

3

FIGURE 1 – CURRENT DERATING (HALF-WAVE)

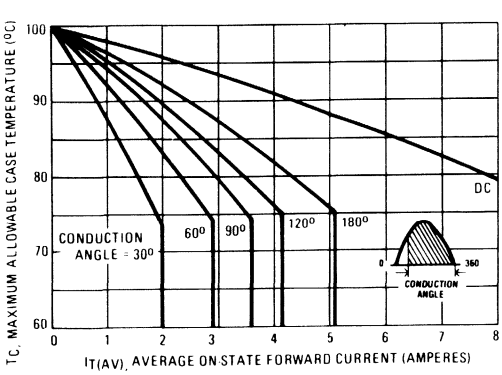


FIGURE 2 – CURRENT DERATING (FULL-WAVE)

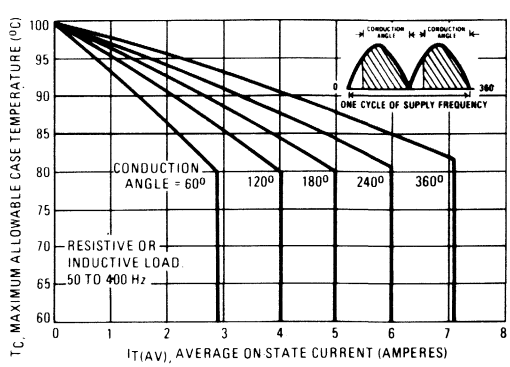


FIGURE 3 – MAXIMUM POWER DISSIPATION (HALF-WAVE)

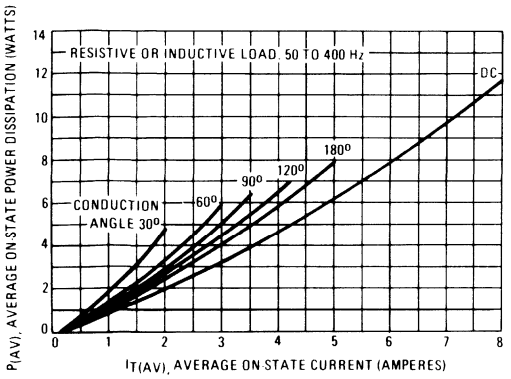
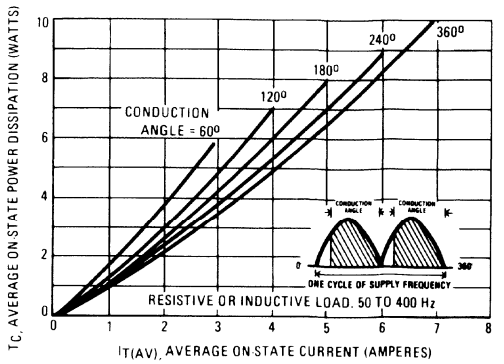


FIGURE 4 – MAXIMUM POWER DISSIPATION (FULL-WAVE)



3

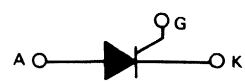
Plastic Silicon Controlled Rectifiers

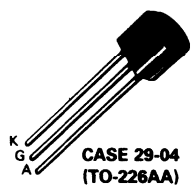
C205 Series

. . . designed and tested for repetitive peak operation required for CD ignition, fuel ignitors, flash circuits, motor controls and low-power switching applications.

- 150 Amperes for 2 μs Safe Area
- High dv/dt
- Very Low VF at High Current
- Low-Cost TO-92

SCRs
1.2 AMPERES RMS
30 thru 400 VOLTS





CASE 29-04
(TO-226AA)
STYLE 10

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 Repetitive Peak Reverse Voltage	V_{RRM} V_{DRM}		Volts
C205Y		30	
C205YY		60	
C205A		100	
C205B		200	
C205D		400	
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	1.2	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)	ITSM	10	Amps
Forward Peak Gate Power T_A = 25°C	P_{GM}	0.5	Watts
Forward Average Gate Power T_A = 25°C	$P_{G(AV)}$	0.1	Watt
Forward Peak Gate Current T_A = 25°C	I_{GM}	0.2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R_θ	75	°C/W

Note 1. V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted. R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM})	T_C = 25°C T_C = 125°C	I_{DRM}	— —	— —	10 200	μA
Peak Reverse Blocking Current (Rated V_{RRM}	T_C = 25°C T_C = 125°C	I_{RRM}	— —	— —	10 200	μA
Peak On-State Voltage, Note 1 (I_{TM} = 1 A Peak, T_C = 25°C)		V_{TM}	—	—	1.6	Volts
Gate Trigger Current (Continuous dc) (V_D = 6 V, R_L = 100 Ohms, T_C = 25°C T_C = −40°C		I_{GT}	— —	— —	200 500	μA
Gate Trigger Voltage (Continuous dc) (V_D = 7 V, R_L = 100 Ohms, T_C = 25°C)		V_{GT}	—	—	0.8	Volts
Holding Current Anode Voltage = 12 Vdc	T_C = 25°C T_C = −40°C	I_H	— —	— —	5 10	mA
Turn-Off Time (V_{DRM} = Rated Voltage) T_J = +125°C		tq	—	15	—	μs
Forward Voltage Application Rate (T_C = 100°C)		dv/dt	—	20	—	V/μs

Note 1. Pulse Test: Pulse Width = 1 ms, Duty Cycle ≤ 2%.

3

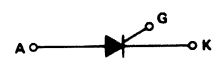
Silicon Controlled Rectifier
Reverse Blocking Triode Thyristor

C230, 231
C230( )3,
231( )3
C232, 233
Series

SCRs
25 AMPERES RMS
50 thru 600 VOLTS

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 300 Amps
- Low Forward "On" Voltage −1.2 V (Typ) @ I_{TM} = 25 Amps
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud, or Isolated Stud
- Glass Passivated Junctions for Maximum Reliability



MAXIMUM RATINGS

Rating	Suffix	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 (T_C = −40 to +100°C) All Types	F A B D M	V_{DRM} and V_{RRM}	50 100 200 400 600	Volts
Non-Repetitive Reverse Voltage (T_C = −40 to 100°C) All Types	F A B D M	V_{RSM}	75 150 300 500 720	Volts
Forward Current RMS		$I_{T(RMS)}$	25	Amps
Peak Surge Current (One Cycle, 60 Hz, T_C = −40 to 100°C)		I_{TSM}	250	Amps
Circuit Fusing (T_C = −40 to 100°C, t = 1 to 8.3 ms)		I^2t	260	A^2s
Peak Gate Power		P_{GM}	5	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current		I_{GM}	2	Amps
Operating Junction Temperature Range		T_J	−40 to +100	°C
Storage Temperature Range		T_{stg}	−40 to +125	°C
Stud Torque		—	30	in. lb.

CASE 174-04
(TO-203)
STYLE 1
C232 and C233 Series

CASE 175-03
STYLE 1
C230 and 231 Series

CASE 235-03
STYLE 1
C230( )3 and C231( )3 Series

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit and Stud Isolated Stud		$R_{\theta JC}$	 1 1.15	°C/W

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

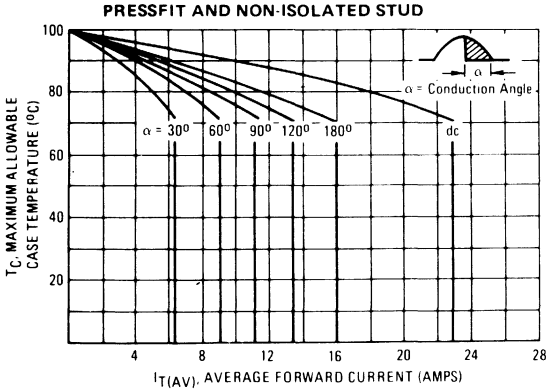
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = 100°C		—	—	1	mA
Forward "On" Voltage (I_{TM} = 100 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.9	Volts
Gate Trigger Current, C230, C230( )3, C232 series (V_D = 12 Vdc, R_L = 120 Ohms)	I_{GT}	—	—	25	mA
(V_D = 12 Vdc, R_L = 60 Ohms) T_C = −40°C		—	—	40	
Gate Trigger Current, C231, C231( )3, C233 (Continuous dc) (V_D = 12 Vdc, R_L = 120 Ohms)	I_{GT}	—	—	9	mA
(V_D = 12 Vdc, R_L = 60 Ohms) T_C = −40°C		—	—	20	
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 120 Ohms)	V_{GT}	—	—	1.5	Volts
(V_D = 12 Vdc, R_L = 60 Ohms) T_C = −40°C		—	—	2	
(V_D = Rated V_{DRM}, R_L = 1000 Ohms) T_C = +100°C		0.2	—	—	
Holding Current (V_D = 24 V, gate open, I_T = 0.5 A)	I_H	—	—	50	mA
T_C = −40°C		—	—	100	
Turn-On Time (t_d + t_r) (I_{TM} = 25 Adc, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	—	1	—	μs
Turn-Off Time (I_{TM} = 10 A, I_R = 10 A, Pulse Width = 50 μs, dv/dt = 20 V/μs, V_D = Rated V_{DRM})	t_q	—	25	—	μs
T_C = 100°C		—	35	—	
Forward Voltage Application Rate (V_D = Rated V_{DRM}) T_C = 100°C	dv/dt	—	100	—	V/μs

3

FIGURE 1 – CURRENT DERATING FOR PRESSFIT AND NON-ISOLATED STUD



NOTE: Derating is for Pressfit and Stud Devices. Isolated stud devices must be derated an additional 15%. For example, the max T_C @ 16 A (180° conduction angle) is 70°C, a derating of 30°C. Isolated stud devices must be derated 34.5°C, therefore, the maximum T_C is 65.5°C.

FIGURE 2 – ON-STATE POWER DISSIPATION versus ON-STATE CURRENT

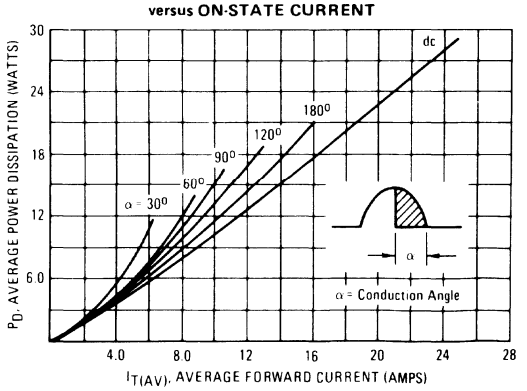


FIGURE 3 – GATE CURRENT VARIATION WITH TEMPERATURE

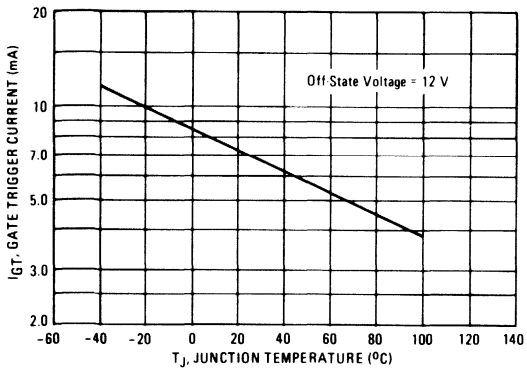
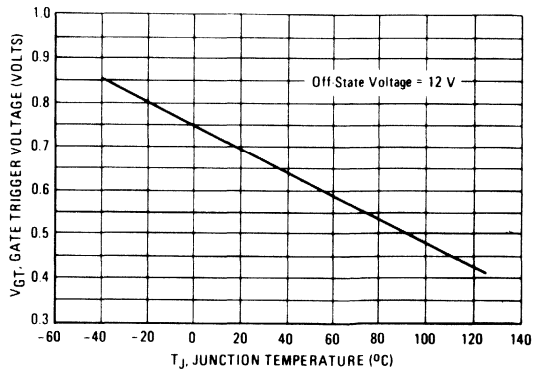


FIGURE 4 – GATE VOLTAGE VARIATION WITH TEMPERATURE



3

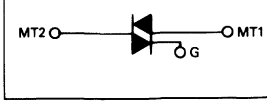
MAC15A Series

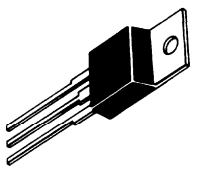
Triacs
Silicon Bidirectional Triode Thyristors

TRIACs
15 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Four Modes





CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = −40 to 125°C) MAC15A4	V_{DRM}	200	Volts
MAC15A6		400	
MAC15A8		600	
MAC15A10		800	
Peak Gate Voltage	V_{GM}	10	Volts
On-State Current RMS Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	15	Amps
Circuit Fusing	I^2t	93	A^2s
Peak Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) Preceded and followed by rated current)	I_{TSM}	150	Amps
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 Voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
Peak On-State Voltage (I_{TM} = 21 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.3	1.6	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	I_{GT}				mA
MT2(+), G(+)		—	—	50	
MT2(+), G(−)		—	—	50	
MT2(−), G(−)		—	—	50	
MT2(−), G(+)		—	—	80	
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
(V_D = Rated V_{DRM}, R_L = 10 k Ohms, T_J = 110°C) MT2(+), G(+); MT2(−), G(−); MT2(+), G(−); MT2(−), G(+)		0.2	—	—	
Holding Current (Either Direction) (V_D = 12 Vdc, Gate Open) (I_T = 200 mA)	I_H	—	6	40	mA
Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 17 A) (I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs

3

FIGURE 1 – RMS CURRENT DERATING

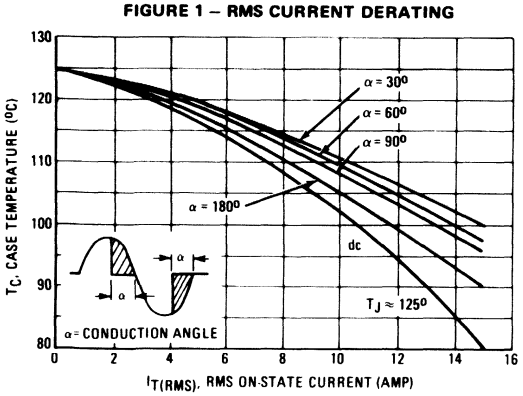


FIGURE 2 – ON-STATE POWER DISSIPATION

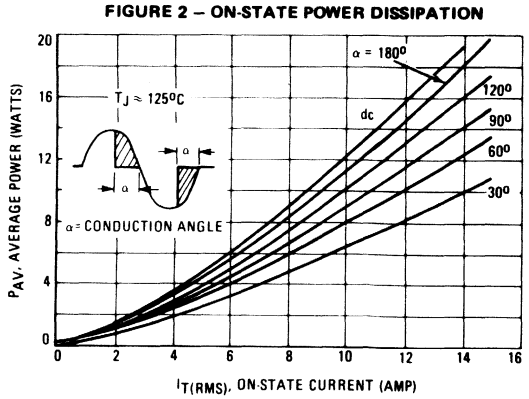


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

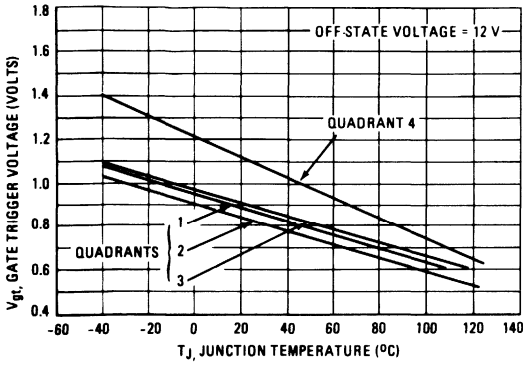


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

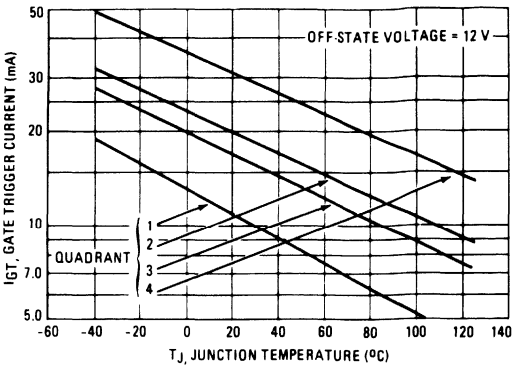


FIGURE 5 – ON-STATE CHARACTERISTICS

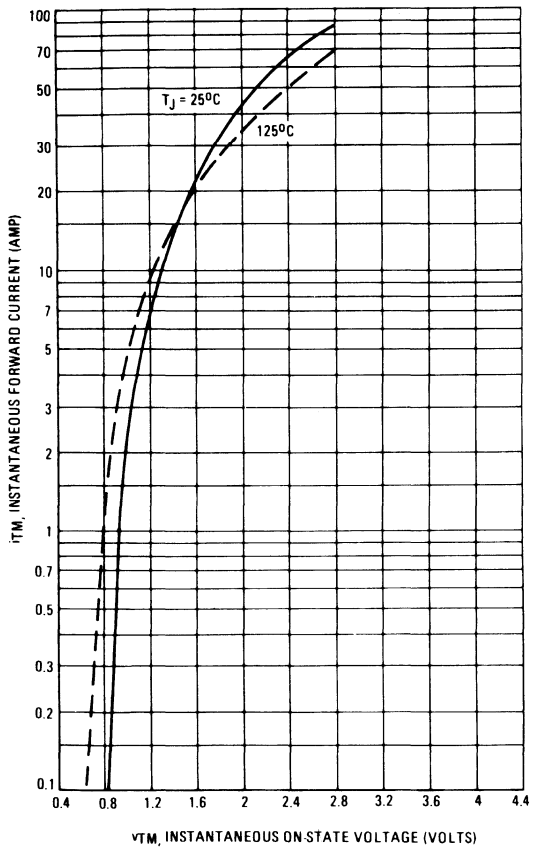


FIGURE 6 – TYPICAL HOLDING CURRENT

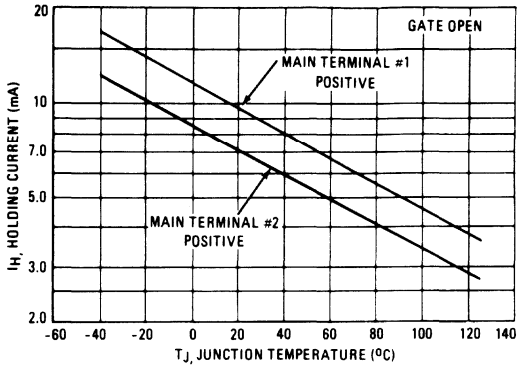


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

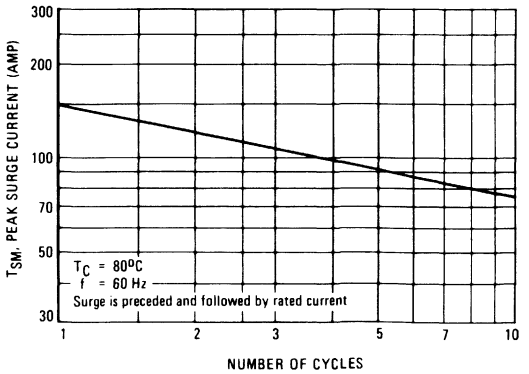


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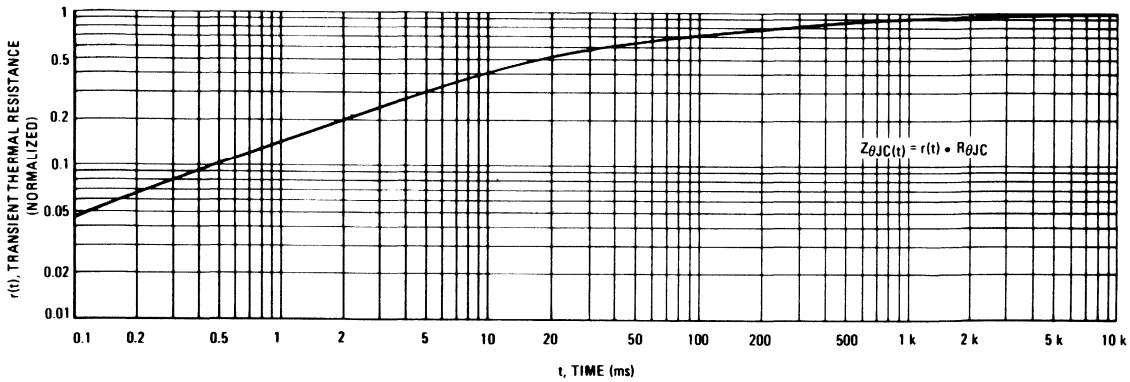
FIGURE 8 – THERMAL RESPONSE



3

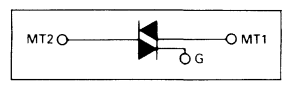
MAC15AFP Series

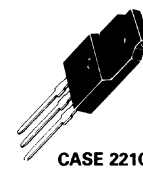
Triacs
Silicon Bidirectional Thyristors

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Four Modes

ISOLATED TRIACs
THYRISTORS
15 AMPERES RMS
200–800 VOLTS





CASE 221C-02
STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC15A4FP MAC15A6FP MAC15A8FP MAC15A10FP	V_{DRM}	 200 400 600 800	Volts
On-State RMS Current (T_C = +80°C), Note 2 Full Cycle Sine Wave 50 to 60 Hz (T_C = +95°C)	$I_{T(RMS)}$	15 12	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) preceded and followed by rated current	I_{TSM}	150	Amps
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amps
Peak Gate Voltage	V_{GM}	10	Volts
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

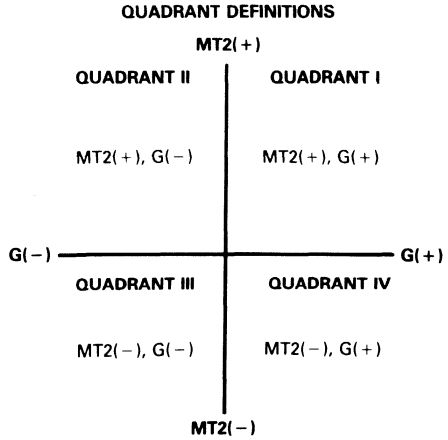
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W
Thermal Resistance, Case to Sink	$R_{\theta CS}$	2.2 (typ)	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) T_J = 25°C	I_{DRM}	—	—	10	μA
Rated V_{DRM} @ T_J = +125°C, Gate Open		—	—	2	mA
Peak On-State Voltage (Either Direction) I_{TM} = 21 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	—	1.3	1.6	Volts
Gate Trigger Current (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms	I_{GT}				mA
MT2(+), G(+)		—	—	50	
MT2(+), G(−)		—	—	50	
MT2(−), G(−)		—	—	50	
MT2(−), G(+)		—	—	80	
Gate Trigger Voltage (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J = +110°C All Trigger Modes		0.2	—	—	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H	—	6	40	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 17 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = +80°C	dv/dt(c)	—	5	—	V/μs

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

Usage	General	
Part Number	MBS4991	MBS4992
V_S	6–10 V	7.5–9 V
I_S	350 μA Max	120 μA Max
V_{S1}–V_{S2}	0.5 V Max	0.2 V Max
Temperature Coefficient	0.02%/°C Typ	

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

TYPICAL CHARACTERISTICS

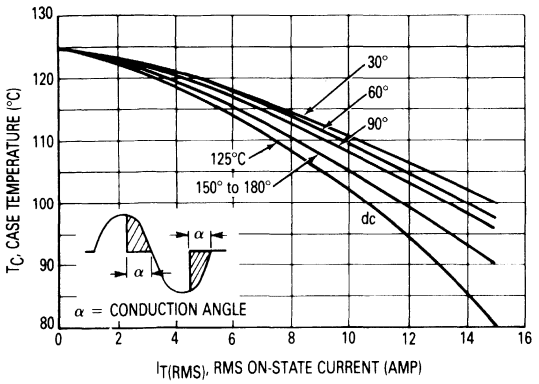


Figure 1. RMS Current Derating

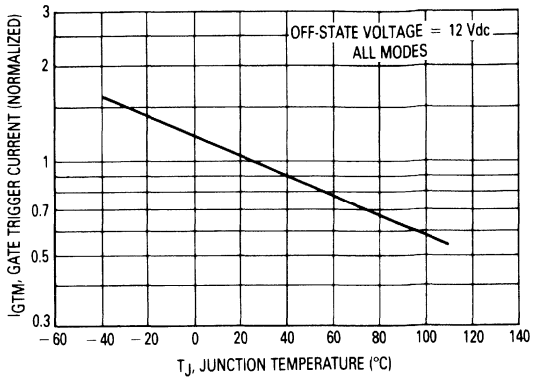


Figure 4. Typical Gate Trigger Current

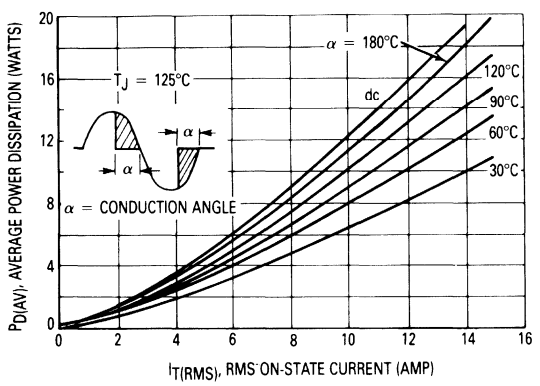


Figure 2. On-State Power Dissipation

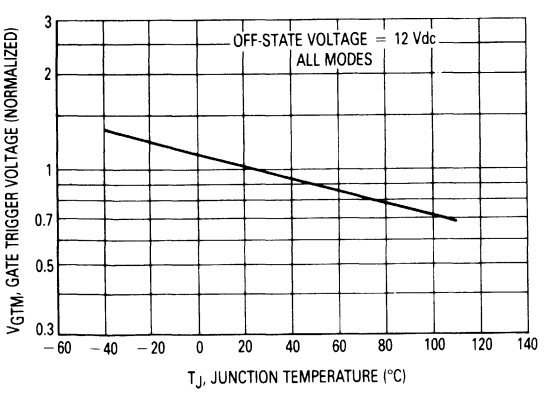


Figure 3. Typical Gate Trigger Voltage

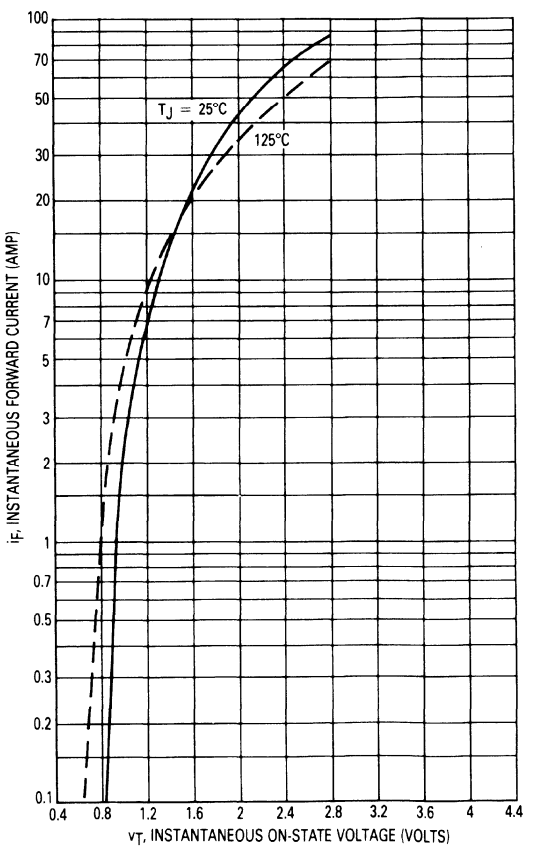


Figure 5. Maximum On-State Characteristics

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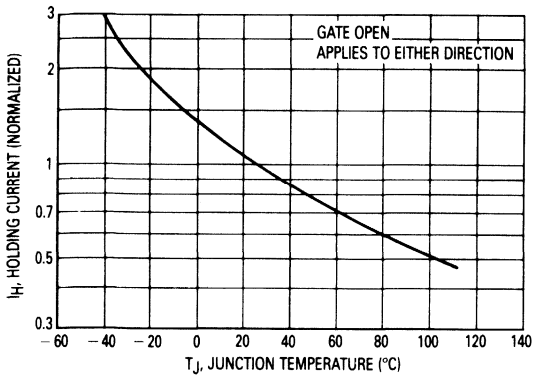


Figure 6. Typical Holding Current

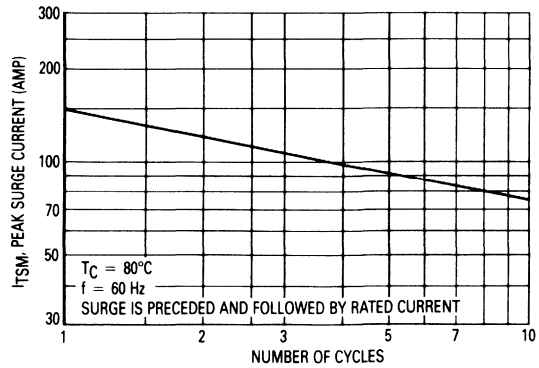


Figure 7. Maximum Nonrepetitive Surge Current

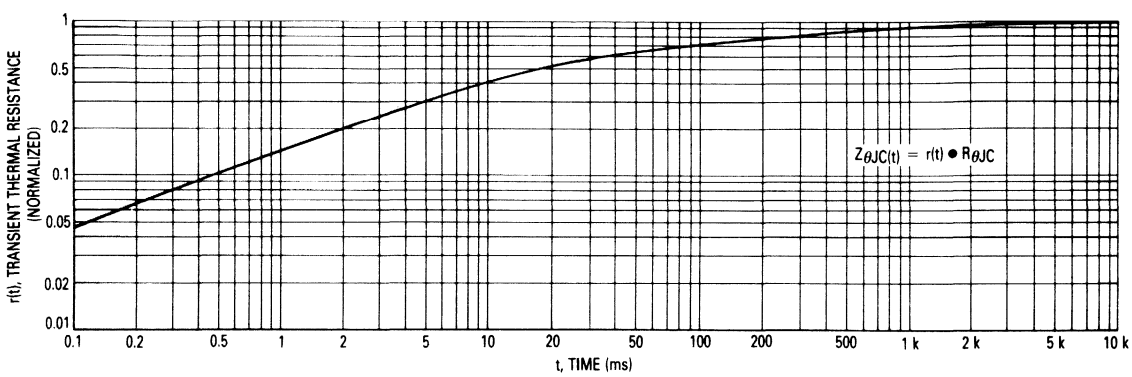


Figure 8. Thermal Response

3

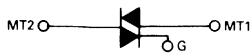
Triacs
Silicon Bidirectional Triode Thyristors

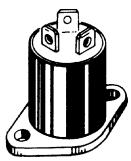
MAC20A
MAC25A
MAC50A

TRIACs
15, 25 and 40
AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for industrial and consumer applications for full-wave control of ac loads such as appliance controls, power supplies, solid-state relays, heating controls, motor controls, welding equipment, and power switching systems.

- Electrically Isolated From Mounting Base
- Isolation Voltage of 2500 Volts RMS
- Quick Connect/Disconnect Terminals
- Glass Passivated and Center Gate Geometry
- Gate Triggering Guaranteed in Four Modes





CASE 326-01
STYLE 2

3

MAXIMUM RATINGS (T_J = −40 to +125°C unless otherwise noted.)

Rating	Symbol	MAC series 20A	MAC series 25A	MAC series 50A	Unit
Repetitive Peak Off-State Voltage 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC20A/25A/50A4 MAC20A/25A/50A6 MAC20A/25A/50A8 MAC20A/25A/50A10	V_{DRM}	 200 400 600 800			Volts
RMS On-State Current (T_C = 100°C for MAC20A) (T_C = 90°C for MAC25A) (T_C = 70°C for MAC50A)	$I_{T(RMS)}$	 15 — —	 — 25 —	 — — 40	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	150	250	300	Amps
Circuit Fusing (t = 1 to 8.3 ms)	I^2t	90	260	375	A^2s
Average Gate Power	$P_{G(AV)}$	0.5	0.5	0.75	Watt
Peak Gate Current (10 μs)	I_{GM}	2	2	4	Amps
Operating Junction Temperature Range	T_J	0 to +125			°C
Storage Temperature Range	T_{stg}	−40 to +125			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Maximum Value			Unit
Thermal Resistance, Junction to Case (DC)	$R_{\theta JC}$	1.6	1.5	1.4	°C/W
(Apparent) Note 1		1.3	1	0.95	

Note 1. Defined as: $\frac{(125°C - T_C)}{P_{AV}}$ for a 60 Hz full sine wave.

ELECTRICAL CHARACTERISTICS

(All voltage polarity reference to MT1; applies to either polarity of MT2 to MT1; T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	MAC20A			MAC25A			MAC50A			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Peak Forward or Reverse Blocking Current		I_{DRM},										
(Rated V_{DRM} or V_{RRM}, gate open) T_C = 25°C		I_{RRM}	—	—	10	—	—	10	—	—	10	μA
T_C = 125°C			—	—	2	—	—	2	—	—	2	mA
Peak On-State Voltage		V_{TM}										Volts
(Pulse Width = 1 ms, Duty Cycle 2%)												
(I_{TM} = 21 A Peak)	MAC20A		—	1.3	1.6	—	—	—	—	—	—	
(I_{TM} = 35 A Peak)	MAC25A		—	—	—	—	1.4	1.7	—	—	—	
(I_{TM} = 56 A Peak)	MAC20A		—	—	—	—	—	—	—	1.65	1.75	
Gate Trigger Current (Continuous dc)		I_{GT}										mA
(V_D = 12 Vdc, R_L = 50 Ohms)												
MT2(+), G(+); MT2(−), G(−); MT2(+), G(−)			—	15	50	—	20	70	—	20	70	
MT2(−), G(+)			—	30	75	—	35	100	—	35	100	
Gate Trigger Voltage (Continuous dc)		V_{GT}										Volts
(V_D = 12 Vdc, R_L = 50 Ohms)												
MT2(+), G(+); MT2(−), G(−); MT2(+), G(−)			—	0.9	2	—	1.1	2	—	1.1	2	
MT2(−), G(+)			—	1.4	2.5	—	1.3	2.5	—	1.3	2.5	
(V_D = Rated V_{DRM}, R_L = 10 kΩ, T_C = 125°C)			0.2	—	—	0.2	—	—	0.2	—	—	
Holding Current		I_H	—	6	40	—	10	75	—	10	75	mA
(V_D = 12 Vdc, Gate Open, R_L = 40 Ohms)												
Turn-On Time		t_{gt}										μs
(V_D = Rated V_{DRM})												
(I_{TM} = 21 A, I_G = 120 mA)	MAC20A		—	1.5	—	—	—	—	—	—	—	
(I_{TM} = 35 A, I_G = 200 mA)	MAC25A		—	—	—	—	1.5	—	—	—	—	
(I_{TM} = 56 A, I_G = 200 mA)	MAC50A		—	—	—	—	—	—	—	1.5	—	
Critical Rate-of-Rise of Commutation Voltage		dv/dt(c)										V/μs
(V_D = Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, T_C = 100°C)	MAC20A		5	30	—	—	—	—	—	—	—	
(V_D = Rated V_{DRM}, I_{TM} = 35 A, Commutating di/dt = 16 A/ms, T_C = 90°C)	MAC25A		—	—	—	5	30	—	—	—	—	
(V_D = Rated V_{DRM}, I_{TM} = 56 A, Commutating di/dt = 22 A/ms, T_C = 70°C)	MAC50A		—	—	—	—	—	—	5	30	—	
Critical Rate-of-Rise of Off-State Voltage (Exponential Rise) (V_D = Rated V_{DRM}, Gate Open, T_C = 125°C)		dv/dt	—	100	—	—	100	—	—	75	—	V/μs

3

FIGURE 1 – CURRENT DERATING

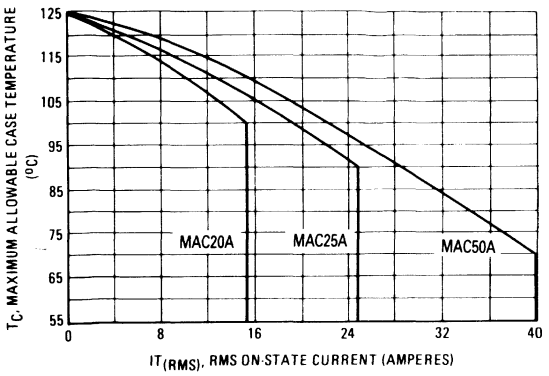
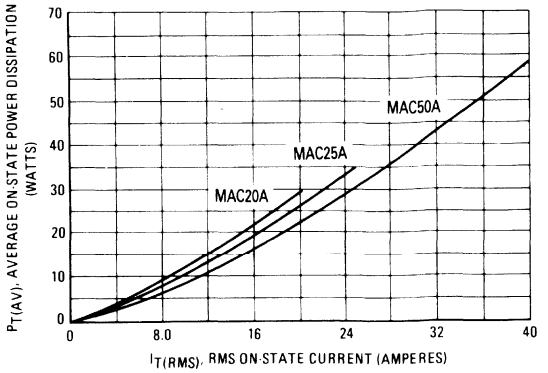


FIGURE 2 – MAXIMUM POWER DISSIPATION



3

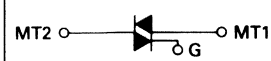
Triacs
Silicon Bidirectional Triode Thyristors

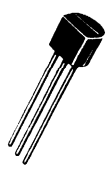
MAC97,A,B Series

. . . designed for use in solid state relays, MPU interface, TTL logic and any other light industrial or consumer application. Supplied in an inexpensive TO-92 package which is readily adaptable for use in automatic insertion equipment.

- One-Piece, Injection-Molded Unibloc Package
- Sensitive Gate Triggering in Four Trigger Modes for all possible Combinations of Trigger Sources, and Especially Suitable for Circuits that Source Gate Drives.
- All Diffused and Glassivated Junctions for Maximum Uniformity of Parameters and Reliability
- Available in TO-5 or TO-18 Leadforms

TRIACs
0.6 AMPERE RMS
200 thru 600 VOLTS





CASE 29-04
(TO-226AA)
STYLE 12

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = −40 to +110°C) Note 1 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC97- 4 or MAC97A- 6 or MAC97B- 8	V_{DRM}	 200 400 600	Volts
On-State RMS Current (Full Cycle Sine Wave 50 to 60 Hz, T_C = +50°C)	$I_{T(RMS)}$	0.6	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = 110°C)	I_{TSM}	8	Amps
Circuit Fusing Considerations (T_J = −40 to +110°C, t = 8.3 ms)	I^2t	0.26	A^2s
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	5	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	5	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.1	Watt
Peak Gate Current (t ≤ 2 μs)	I_{GM}	1	Amp
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 110°C		—	8	0.1	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 0.85 A Peak; Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.9	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	I_{GT}	See Table 1			mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	V_{GT}				Volts
MT2(+), G(+) All Types		—	—	2	
MT2(+), G(−) All Types		—	—	2	
MT2(−), G(−) All Types		—	—	2	
MT2(−), G(+) All Types		—	—	2.5	
(V_D = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C)					
MT2(+), G(+); MT2(−), G(−); MT2(+), G(−) All Types		0.1	—	—	
MT2(−), G(+) All Types		0.1	—	—	
Holding Current (V_D = 12 Vdc, I_{TM} = 200 mA, Gate Open)	I_H	—	—	10	mA
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 1 A pk, I_G = 25 mA)	t_{gt}	—	2	—	μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 0.84 μA pk) (Commutating di/dt = 0.32 A/ms, Gate Unenergized, T_C = 50°C)	dv/dt(c)	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM} Exponential Waveform, T_C = 110°C)	dv/dt	—	25	—	V/μs

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

3

QUADRANT DEFINITIONS

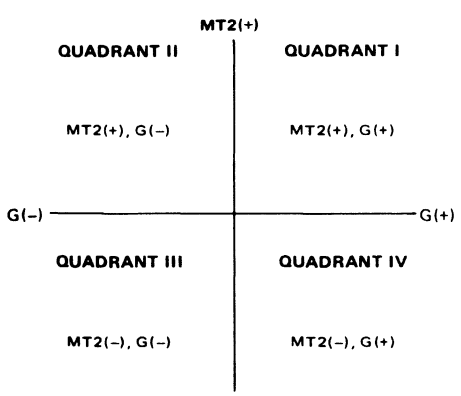


TABLE 1 — MAXIMUM GATE TRIGGER CURRENTS (V_D = 12 V, R_L = 100 Ω)

Quadrant and Polarity	MAC Series 97	MAC Series 97A	MAC Series 97B	Unit
I MT2(+), G(+)	10	5.0	3.0	mA
II MT2(+), G(−)	10	5.0	3.0	mA
III MT2(−), G(−)	10	5.0	3.0	mA
IV MT2(−), G(+)	10	7.0	5.0	mA

FIGURE 1 – RMS CURRENT DERATING
(Reference: Case Temperature)

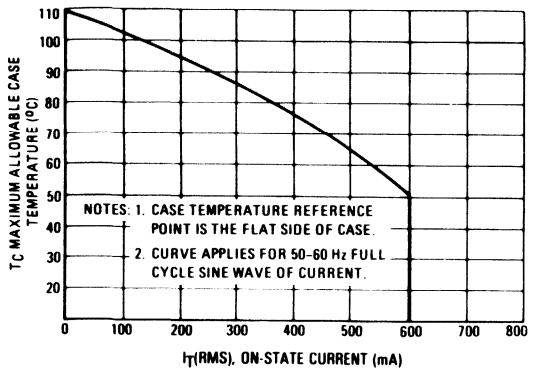


FIGURE 2 – ON-STATE CHARACTERISTICS

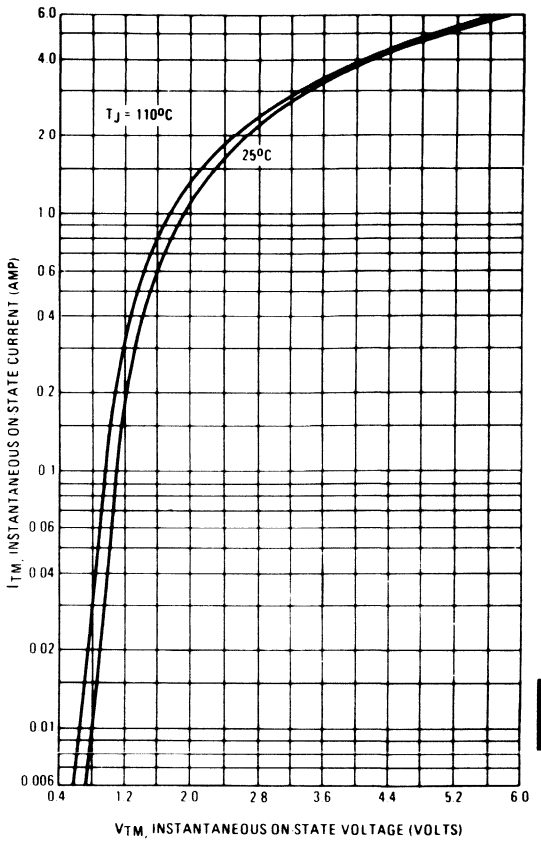


FIGURE 3 – RMS CURRENT DERATING
(Reference: Ambient Temperature)

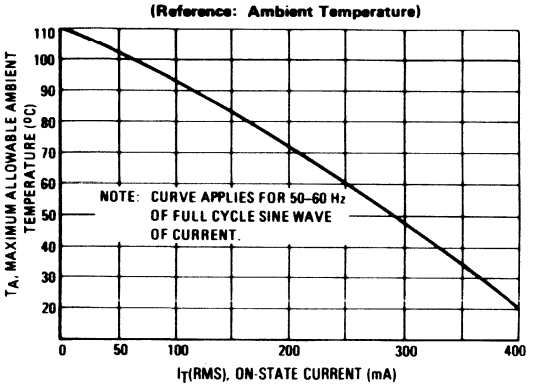


FIGURE 4 – ON-STATE POWER DISSIPATION

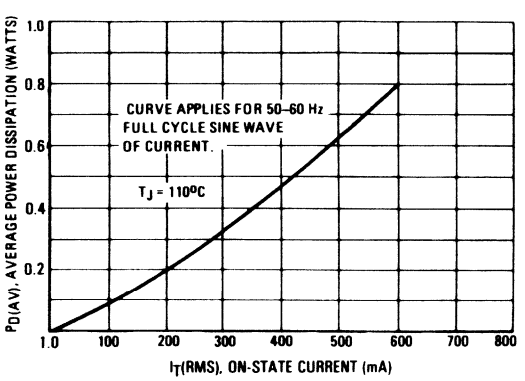


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FIGURE 5 – NORMALIZED GATE TRIGGER CURRENT

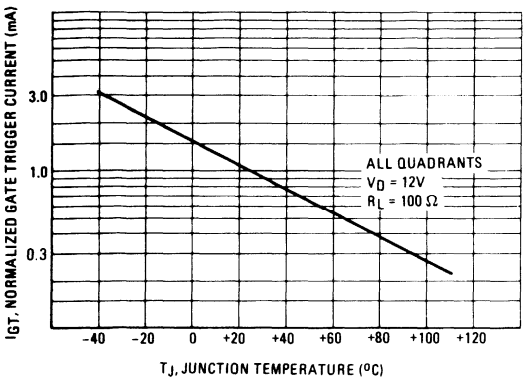


FIGURE 6 – NORMALIZED GATE TRIGGER VOLTAGE

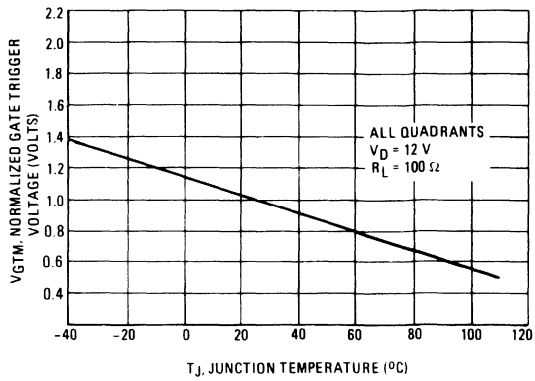


FIGURE 7 – NORMALIZED HOLD CURRENT

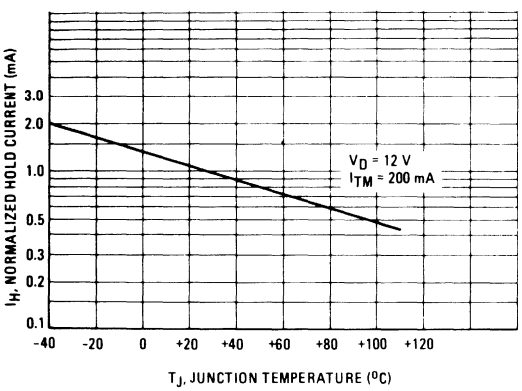


FIGURE 8 – MAXIMUM ALLOWABLE SURGE CURRENT

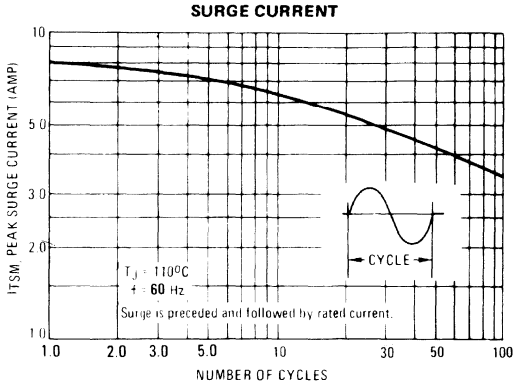
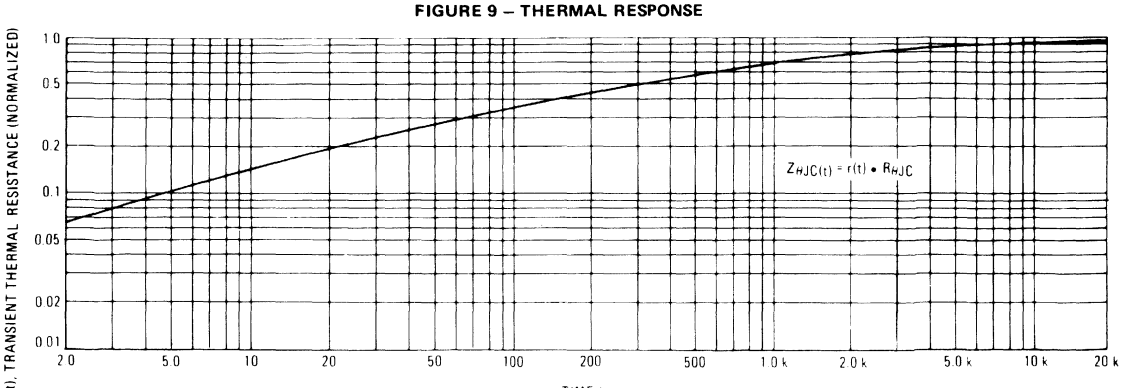


FIGURE 9 – THERMAL RESPONSE



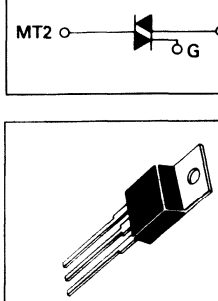
Triacs
Silicon Bidirectional Thyristors

MAC210A Series

TRIACs
10 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Four Modes



CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open — MAC210A4	V_{DRM}	200	Volts
MAC210A6		400	
MAC210A8		600	
MAC210A10		800	
On-State Current RMS (T_C = +70°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	10	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +70°C) Preceded and followed by Rated Current	I_{TSM}	100	Amps
Circuit Fusing Considerations (T_C = +70°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +70°C, Pulse Width = 10 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +70°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Current (T_C = +70°C, Pulse Width = 10 μs)	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = +125°C		—	—	2	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 14 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.2	1.65	Volts
Gate Trigger Current (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms)	I_{GT}				mA
MT2(+), G(+)		—	12	50	
MT2(+), G(−)		—	12	50	
MT2(−), G(−)		—	20	50	
MT2(−), G(+)		—	35	80	
Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms)	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
(Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = +125°C) MT2(+), G(+); MT2(−), G(−); MT2(+), G(−); MT2(−), G(+)		0.2	—	—	
Holding Current (Either Direction) (Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 500 mA, T_C = +25°C)	I_H	—	6	50	mA
Turn-On Time (Rated V_{DRM}, I_{TM} = 14 A) (I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (Rated V_{DRM}, I_{TM} = 14 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 70°C)	dv/dt(c)	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DROM}, Exponential Voltage Rise, Gate Open, T_C = +70°C)	dv/dt	—	100	—	V/μs

3

FIGURE 1 — CURRENT DERATING

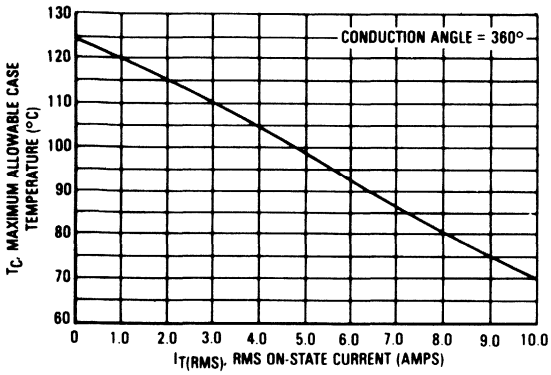


FIGURE 2 — POWER DISSIPATION

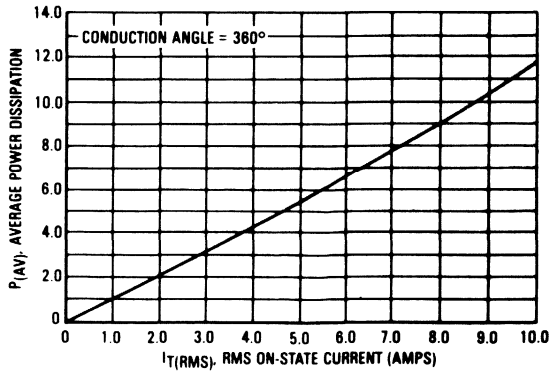


FIGURE 3 — MAXIMUM ON-STATE CHARACTERISTICS

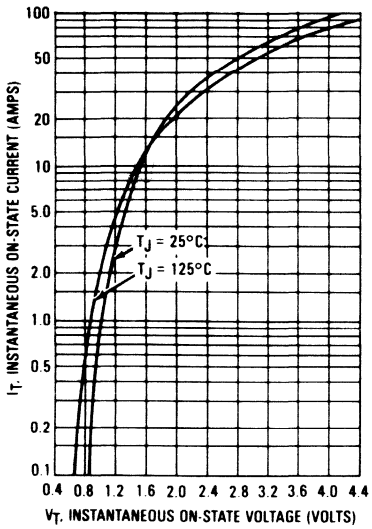


FIGURE 4 — MAXIMUM NON-REPETITIVE SURGE CURRENT

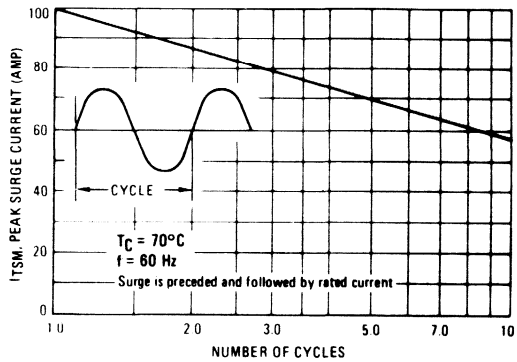


FIGURE 5 — TYPICAL GATE TRIGGER VOLTAGE

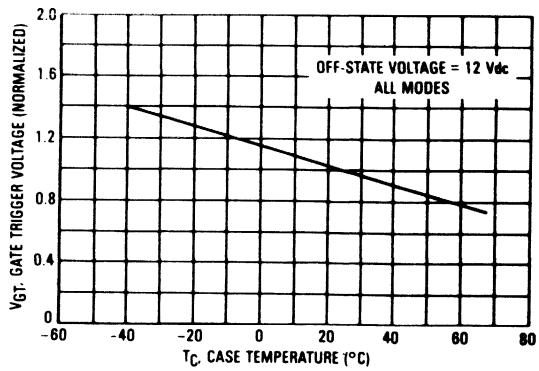


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FIGURE 6 — TYPICAL GATE TRIGGER CURRENT

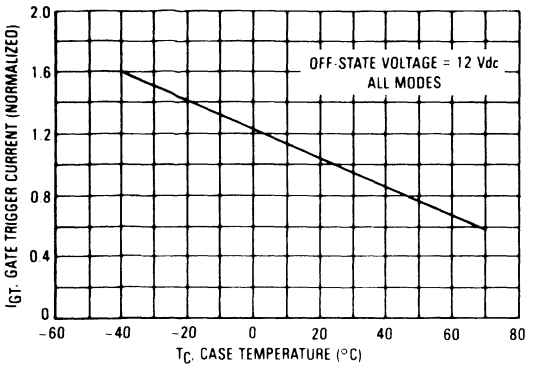


FIGURE 7 — TYPICAL HOLDING CURRENT

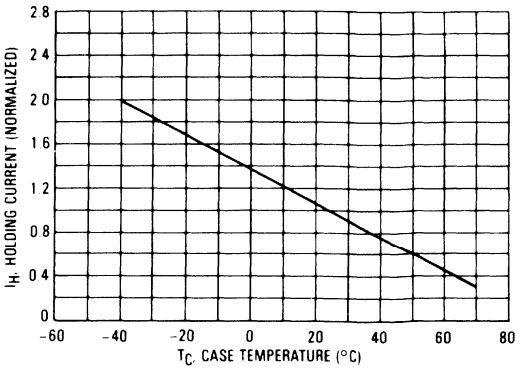
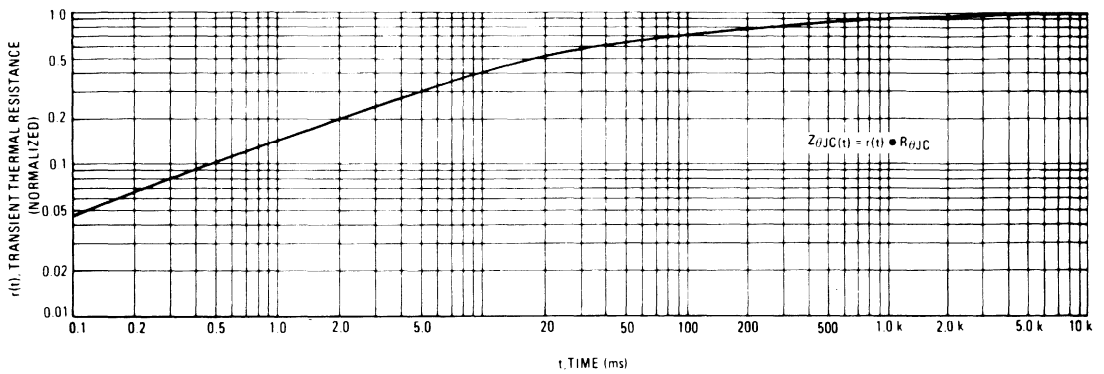


FIGURE 8 — THERMAL RESPONSE



3

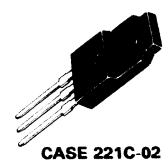
MAC210AFP Series

Triacs
Silicon Bidirectional Thyristors

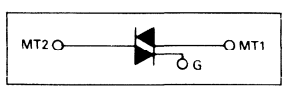
. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Four Modes

ISOLATED TRIACs THYRISTORS 10 AMPERES RMS 200–800 VOLTS



CASE 221C-02 STYLE 3



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC210A4FP MAC210A6FP MAC210A8FP MAC210A10FP	V_{DRM}	 200 400 600 800	Volts
On-State RMS Current (T_C = +70°C) Full Cycle Sine Wave 50 to 60 Hz, Note 2	$I_{T(RMS)}$	10	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_C = +70°C) preceded and followed by rated current	I_{TSM}	100	Amps
Circuit Fusing (T_C = +70°C, t = 1 to 8.3 ms)	I^2t	41	A^2s
Peak Gate Power (T_C = +70°C, Pulse Width = 10 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +70°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Current (T_C = +70°C, Pulse Width = 10 μs)	I_{GM}	2	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Case to Sink	$R_{\theta CS}$	2.2 (typ)	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

3

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM}, Gate Open	I_{DRM}				
T_J = 25°C		—	—	10	μA
T_J = +125°C		—	—	2	mA
Peak On-State Voltage (Either Direction) I_{TM} = 14 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	—	1.2	1.65	Volts
Gate Trigger Current (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	I_{GT}				mA
MT2(+), G(+)		—	12	50	
MT2(+), G(−)		—	12	50	
MT2(−), G(−)		—	20	50	
MT2(−), G(+)		—	35	80	
Gate Trigger Voltage (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J = +125°C All Trigger Modes		0.2	—	—	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 500 mA, T_C = +25°C	I_H	—	6	50	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 14 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 14 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = +70°C	$dv/dt_{(c)}$	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DROM}, Exponential Voltage Rise, Gate Open, T_C = +70°C)	dv/dt	—	100	—	V/μs

3

TYPICAL CHARACTERISTICS

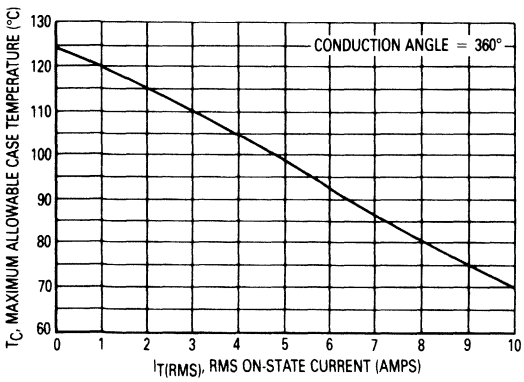


Figure 1. Current Derating

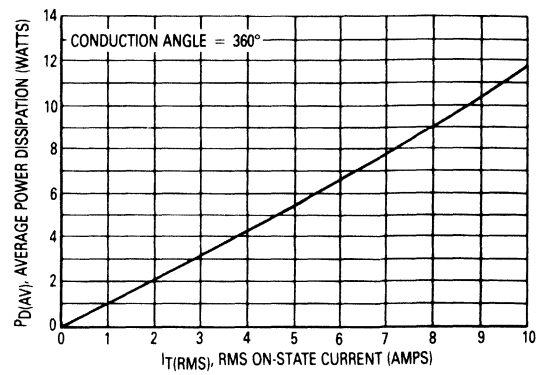


Figure 2. Power Dissipation

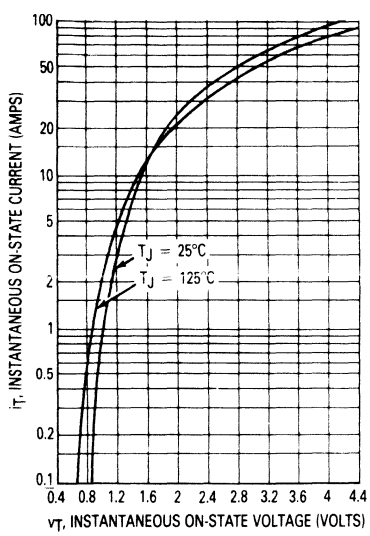


Figure 3. Maximum On-State Characteristics

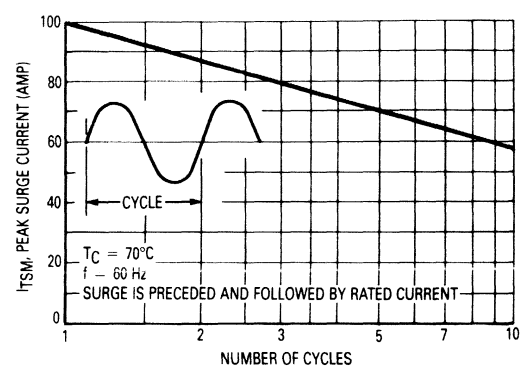


Figure 4. Maximum Nonrepetitive Surge Current

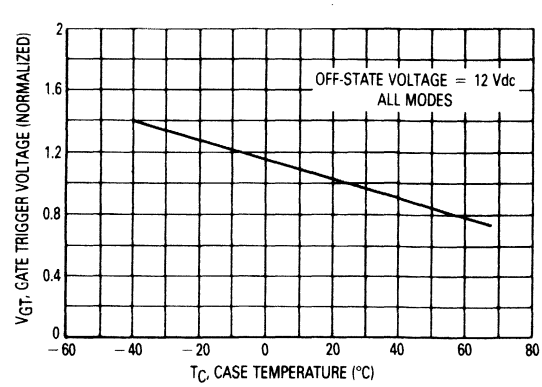


Figure 5. Typical Gate Trigger Voltage

3

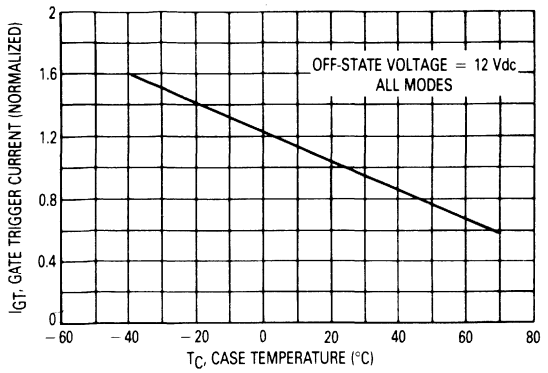


Figure 6. Typical Gate Trigger Current

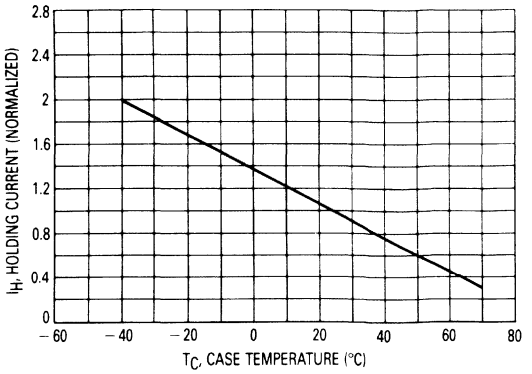


Figure 7. Typical Holding Current

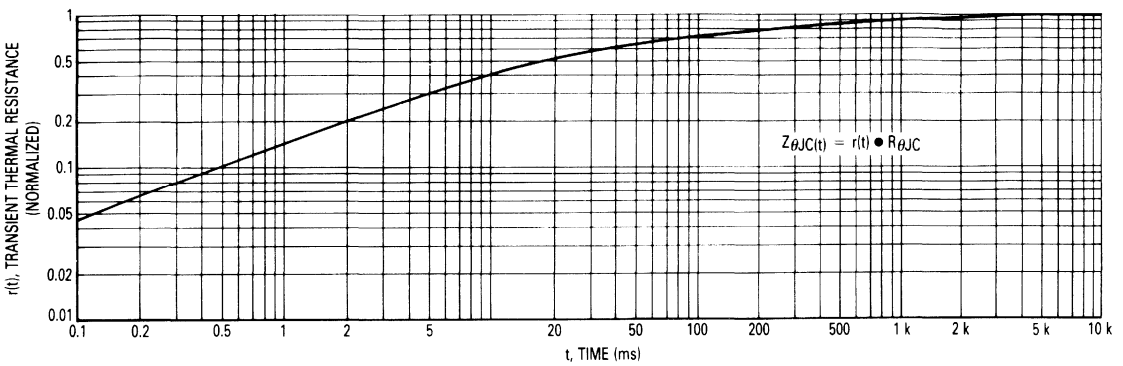


Figure 8. Thermal Response

3

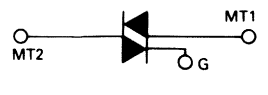
Triacs
Silicon Bidirectional Thyristors

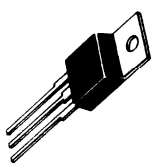
MAC212A Series

TRIACs
12 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Four Modes





CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC212A4 MAC212A6 MAC212A8 MAC212A10	V_{DRM}	 200 400 600 800	Volts
On-State Current RMS (T_C = +85°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	12	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +85°C) preceded and followed by Rated Current	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_C = +85°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +85°C, Pulse Width = 10 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +85°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Current (T_C = +85°C, Pulse Width = 10 μs)	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM}, Gate Open	I_{DRM}				
T_J = 25°C		—	—	10	μA
T_J = +125°C		—	—	2	mA
Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	—	1.3	1.75	Volts
Gate Trigger Current (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms	I_{GT}				mA
MT2(+), G(+)		—	12	50	
MT2(+), G(−)		—	12	50	
MT2(−), G(−)		—	20	50	
MT2(−), G(+)		—	35	80	
Gate Trigger Voltage (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J = +125°C MT2(+), G(+); MT2(−), G(−); MT2(+), G(−); MT2(−), G(+)		0.2	—	—	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 500 mA, T_C = +25°C	I_H	—	6	50	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 17 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 17 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = +85°C	$dv/dt_{(c)}$	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DROM}, Exponential Voltage Rise, Gate Open, T_C = +85°C)	dv/dt	—	100	—	V/μs

3

FIGURE 1 — CURRENT DERATING

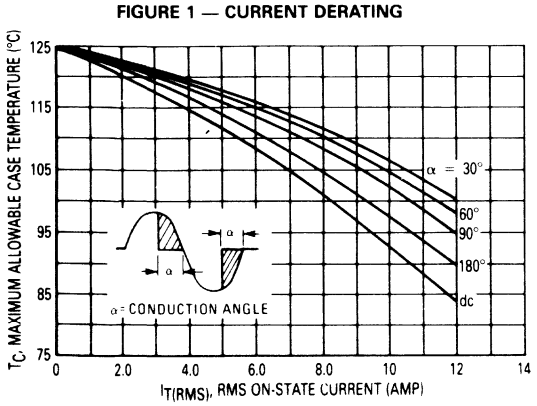


FIGURE 2 — POWER DISSIPATION

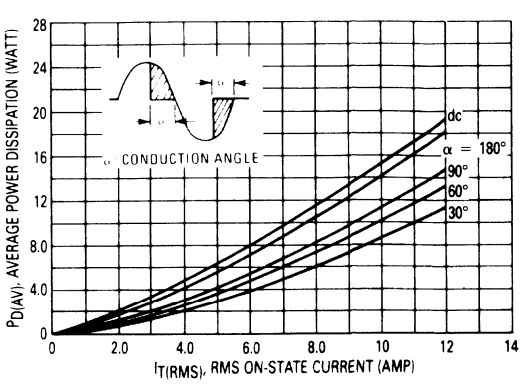


FIGURE 3 — MAXIMUM ON-STATE CHARACTERISTICS

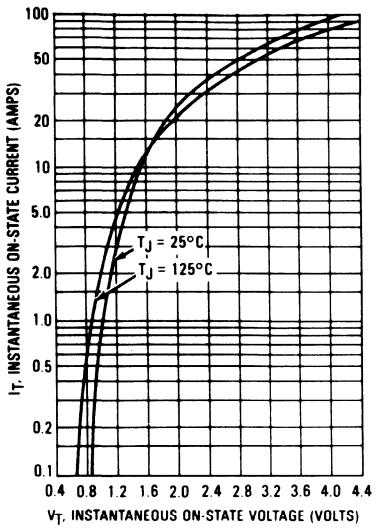


FIGURE 4 — MAXIMUM NON-REPETITIVE SURGE CURRENT

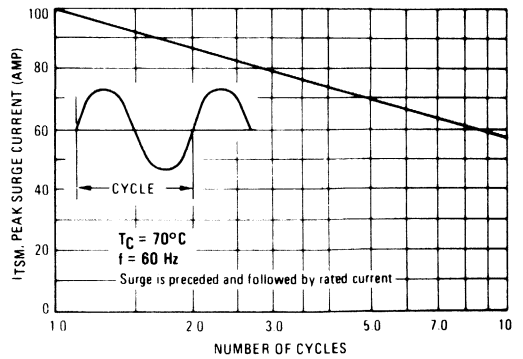


FIGURE 5 — TYPICAL GATE TRIGGER VOLTAGE

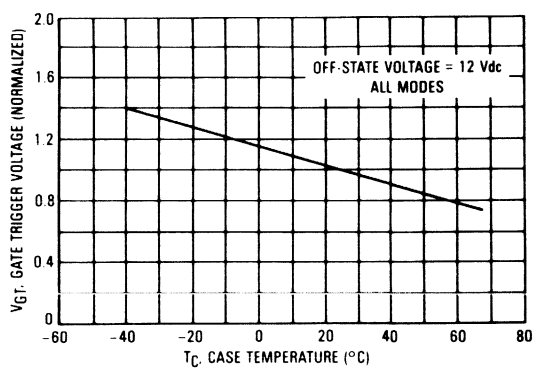


FIGURE 6 — TYPICAL GATE TRIGGER CURRENT

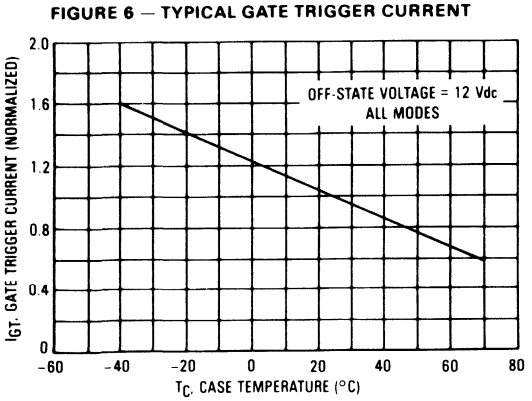


FIGURE 7 — TYPICAL HOLDING CURRENT

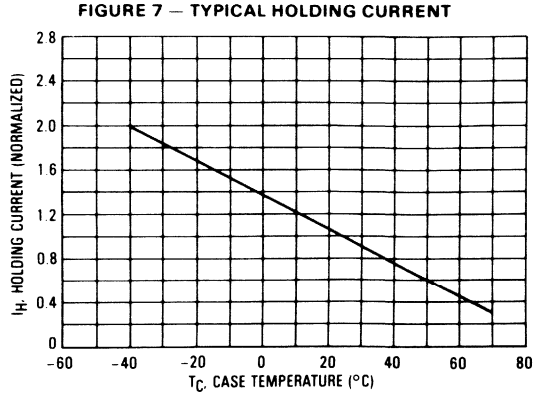


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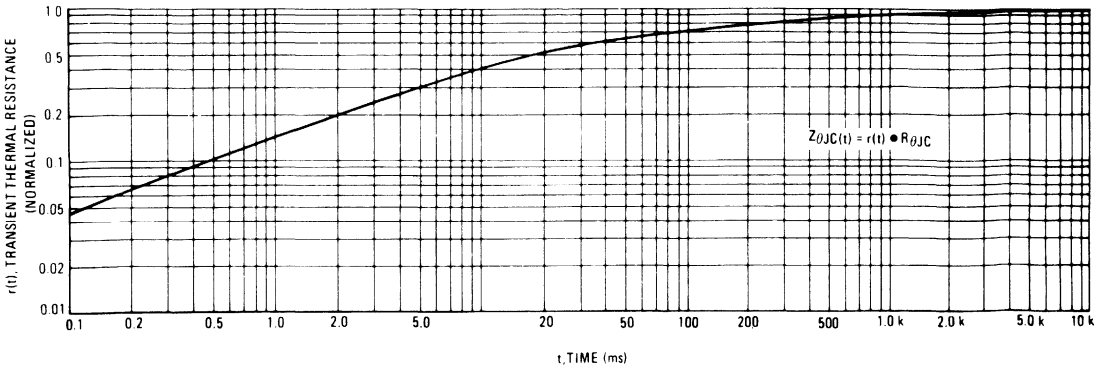
FIGURE 8 — THERMAL RESPONSE



3

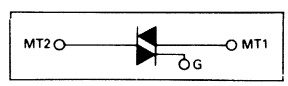
MAC212AFP Series

Triacs
Silicon Bidirectional Thyristors

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Four Modes

ISOLATED TRIACs
THYRISTORS
12 AMPERES RMS
200–800 VOLTS



CASE 221C-02
STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC212A4FP MAC212A6FP MAC212A8FP MAC212A10FP	V_{DRM}	 200 400 600 800	Volts
On-State RMS Current (T_C = +85°C) Full Cycle Sine Wave 50 to 60 Hz, Note 2	$I_{T(RMS)}$	12	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_C = +85°C) preceded and followed by rated current	I_{TSM}	100	Amps
Circuit Fusing (T_C = +85°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +85°C, Pulse Width = 10 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +85°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Current (T_C = +85°C, Pulse Width = 10 μs)	I_{GM}	2	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W
Thermal Resistance, Case to Sink	$R_{\theta CS}$	2.2 (typ)	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

3

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM}, Gate Open	I_{DRM}				
T_J = 25°C		—	—	10	μA
T_J = +125°C		—	—	2	mA
Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	—	1.3	1.75	Volts
Gate Trigger Current (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	I_{GT}				mA
MT2(+), G(+)		—	12	50	
MT2(+), G(−)		—	12	50	
MT2(−), G(−)		—	20	50	
MT2(−), G(+)		—	35	80	
Gate Trigger Voltage (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J = +125°C All Trigger Modes		0.2	—	—	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 500 mA, T_C = +25°C	I_H	—	6	50	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 17 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 17 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = +85°C	$dv/dt_{(c)}$	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DROM}, Exponential Voltage Rise, Gate Open, T_C = +85°C)	dv/dt	—	100	—	V/μs

3

TYPICAL CHARACTERISTICS

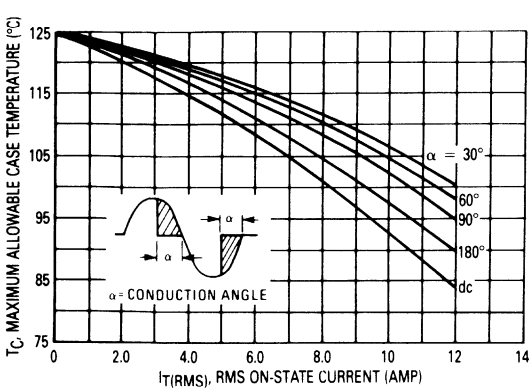


Figure 1. Current Derating

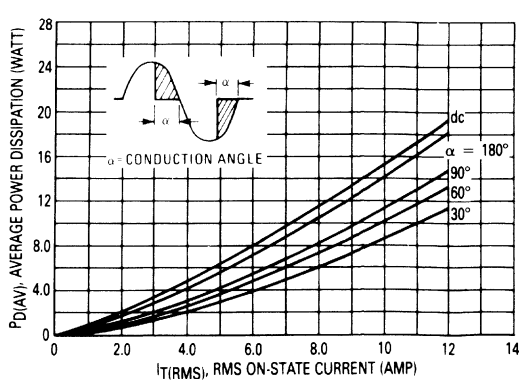


Figure 2. Power Dissipation

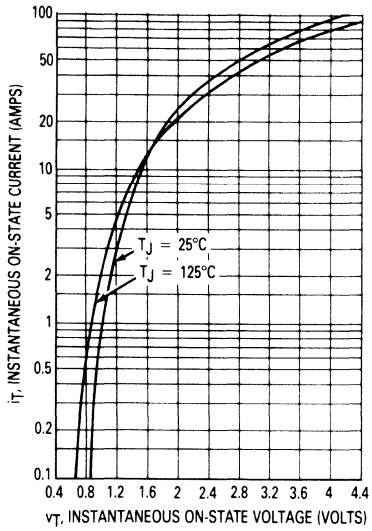


Figure 3. Maximum On-State Characteristics

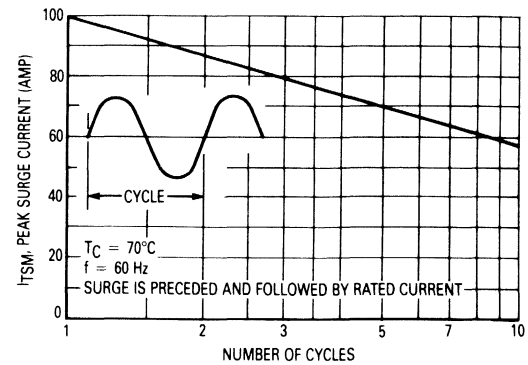


Figure 4. Maximum Nonrepetitive Surge Current

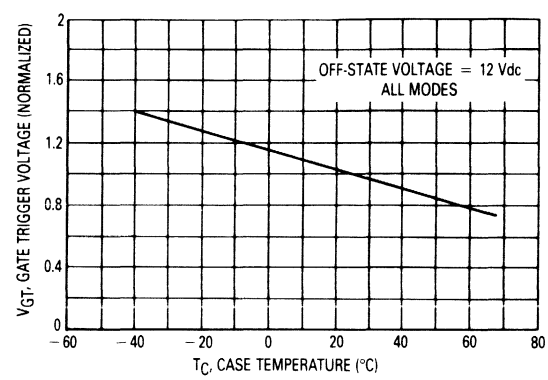


Figure 5. Typical Gate Trigger Voltage

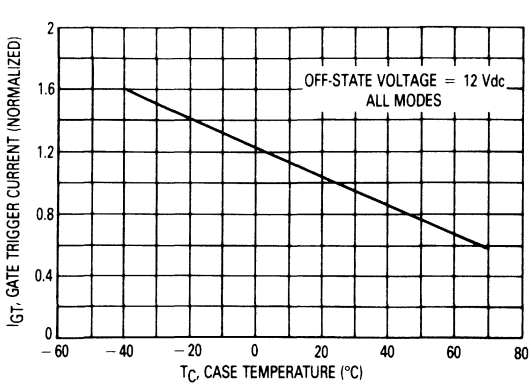


Figure 6. Typical Gate Trigger Current

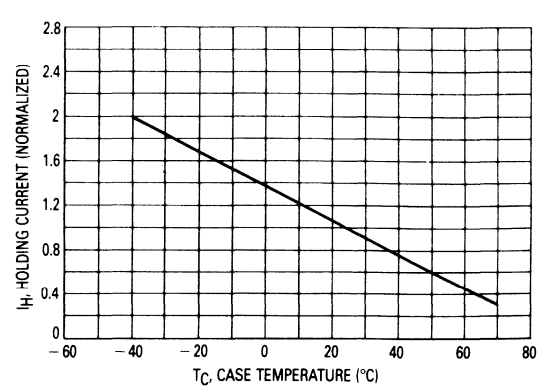


Figure 7. Typical Holding Current

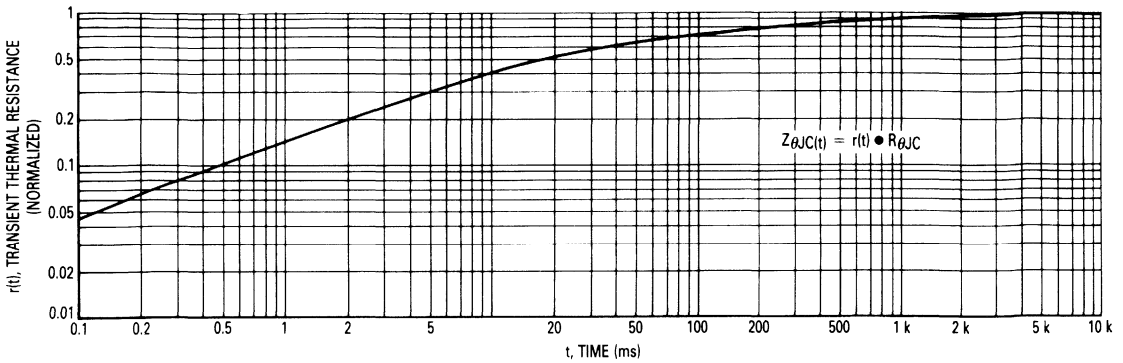


Figure 8. Thermal Response

3

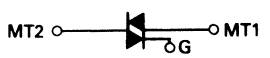
Triacs
Silicon Bidirectional Thyristors

MAC218A Series

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 800 Volts
- Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- TO-220 Construction Low Thermal Resistance, High Heat Dissipation and Durability

TRIACs
8 AMPERES RMS
200 thru 800 VOLTS



CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 Gate Open MAC218A4 A6 A8 A10	V_{DRM}	 200 400 600 800	Volts
On-State Current RMS (Conduction Angle = 360°, T_C = +80°C)	$I_{T(RMS)}$	8	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amps
Fusing Current (T_J = −40 to +100°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 11.3 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle < 2%)	V_{TM}	—	1.7	2	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 12Ω) Trigger Mode	I_{GT}				mA
MT2(+), Gate(+); MT2(+), Gate(−); MT2(−), Gate(−)		—	—	50	
MT2(−), Gate(+)		—	—	80	
Gate Trigger Voltage (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J = +125°C MT2(+), G(+); MT2(−), G(−); MT2(+), G(−); MT2(−), G(+)		0.2	—	—	
Holding Current (Either Direction) (V_D = 24 Vdc, Gate Open, Initiating Current = 200 mA)	I_H	—	—	50	mA
Critical Rate of Rise of Commutating Off-State Voltage (Rated V_{DROM}, $I_{T(RMS)}$ = 6 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DROM}, Exponential Voltage Rise, Gate Open, T_J = 125°C)	dv/dt	—	100	—	V/μs

3

FIGURE 1 — CURRENT DERATING

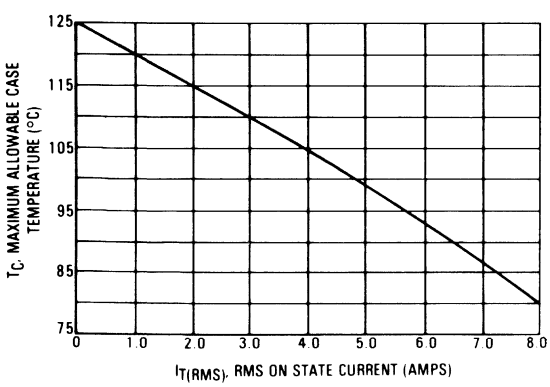


FIGURE 2 — POWER DISSIPATION

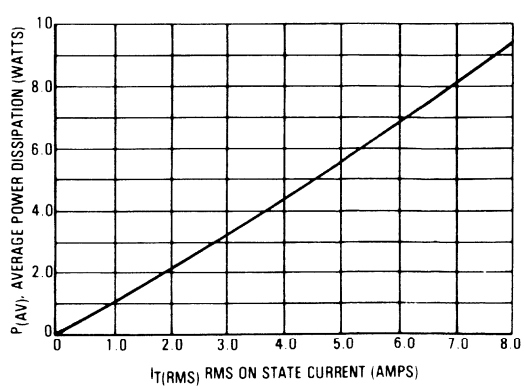


FIGURE 3 — NORMALIZED GATE TRIGGER CURRENT

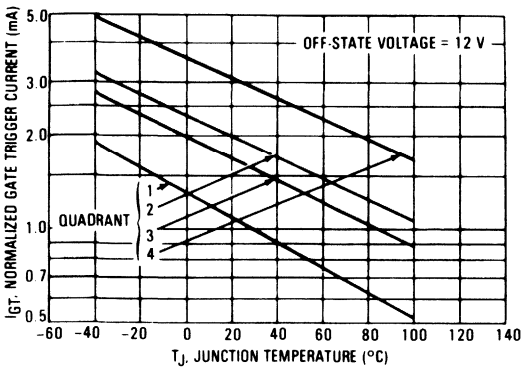


FIGURE 4 — NORMALIZED GATE TRIGGER VOLTAGE

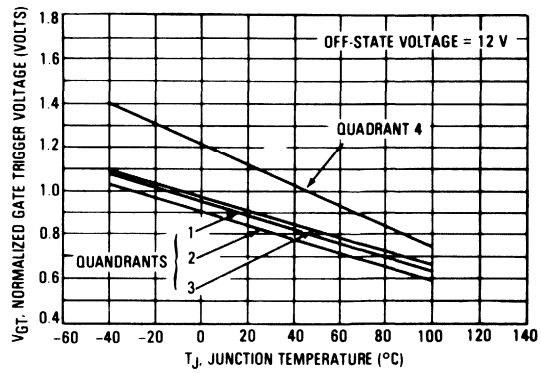
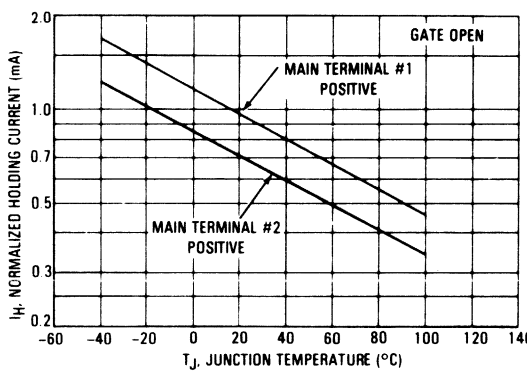


FIGURE 5 — NORMALIZED HOLDING CURRENT



3

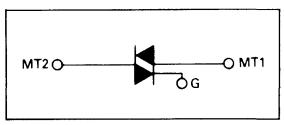
MAC218AFP Series

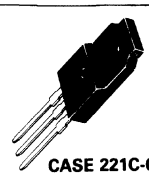
Triacs
Silicon Bidirectional Thyristors

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 800 Volts
- Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Isolated TO-220 Type Package for Ease of Mounting
- Gate Triggering Guaranteed in Four Modes

ISOLATED TRIACs
THYRISTORS
8 AMPERES RMS
200–800 VOLTS





CASE 221C-02
STYLE 3

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC218A4FP MAC218A6FP MAC218A8FP MAC218A10FP	V_{DRM}	 200 400 600 800	Volts
On-State RMS Current (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz, Note 2	$I_{T(RMS)}$	8	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz) preceded and followed by rated current	I_{TSM}	100	Amps
Circuit Fusing (T_J = −40 to +100°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Current (Pulse Width = 1 μs)	I_{GM}	4	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Case to Sink	$R_{\theta CS}$	2.2 (typ)	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) (Rated V_{DROM} @ T_J = 125°C, Gate Open)	I_{DROM}	—	—	2	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 11.3 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle < 2%)	V_{TM}	—	1.7	2	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 12 Ω) Trigger Mode	I_{GT}				mA
MT2(+), G(+)		—	—	50	
MT2(+), G(−)		—	—	50	
MT2(−), G(−)		—	—	50	
MT2(−), G(+)		—	—	80	
Gate Trigger Voltage (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J = +125°C MT2(+), G(+); MT2(−), G(−); MT2(+), G(−); MT2(−), G(+)		0.2	—	—	
Holding Current (Either Direction) (V_D = 24 Vdc, Gate Open, Initiating Current = 200 mA)	I_H	—	—	50	mA
Critical Rate of Rise of Commutating Off-State Voltage (Rated V_{DROM}, $I_{T(RMS)}$ = 6 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C)	$dv/dt_{(c)}$	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DROM}, Exponential Voltage Rise, Gate Open, T_J = 125°C)	dv/dt	—	100	—	V/μs

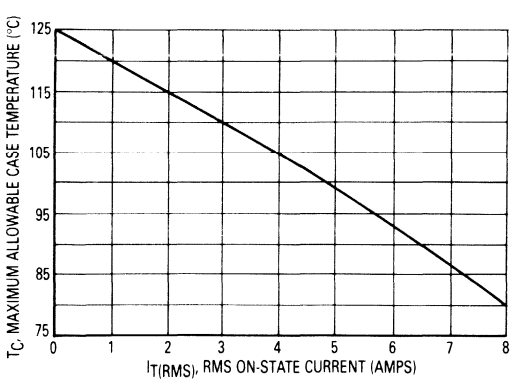


Figure 1. Current Derating

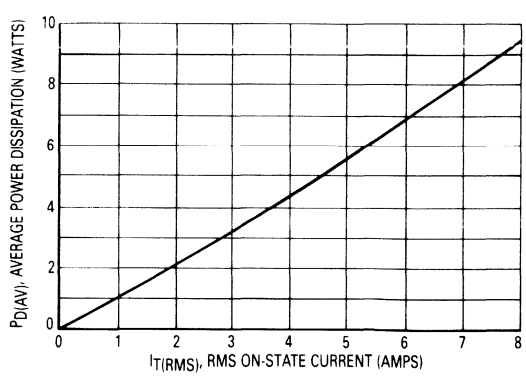


Figure 2. Power Dissipation

3

TYPICAL CHARACTERISTICS

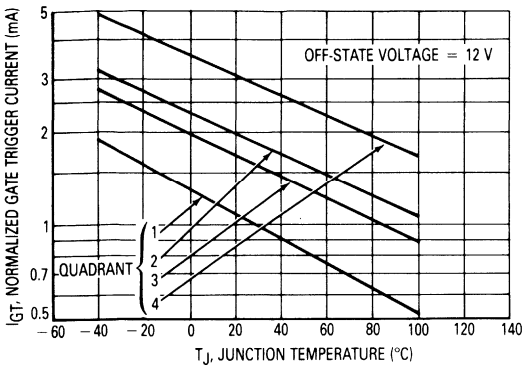


Figure 3. Normalized Gate Trigger Current

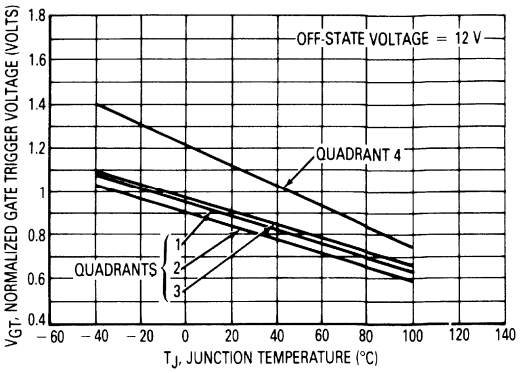


Figure 4. Normalized Gate Trigger Voltage

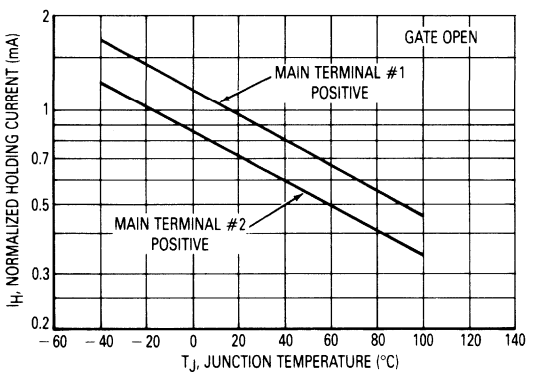


Figure 5. Normalized Holding Current

3

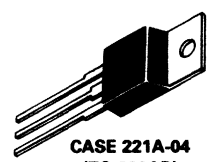
Triacs
Silicon Bidirectional Triode Thyristors

MAC223A Series

. . . designed primarily for full-wave ac control applications such as lighting sysjtems, heater controls, motor controls and power supplies; or wherever full-wave silicon-gate-controlled devices are needed.

- Off-State Voltages to 800 Volts
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged Thermowatt Construction for Thermal Resistance and High Heat Dissipation
- Gate Triggering Guaranteed in Four Modes

TRIACs
25 AMPERES RMS
100 thru 800 VOLTS



CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = −40 to 125°C), Note 1 (1/2 Sine Wave 50 to 60 Hz, Gate Open)	V_{DRM}		Volts
MAC223A4		200	
6		400	
8		600	
10		800	
On-State RMS Current (T_C = 80°C) (Full Cycle Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	25	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = 125°C)	I_{TSM}	250	Amps
Circuit Fusing (T_J = −40 to 125°C; t = 8.3 ms)	I^2t	260	A^2s
Peak Gate Current (t ≤ 2 μs)	I_{GM}	2	Amps
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±10	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20	Watts

Note 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

(cont.)

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	−40 to 125	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C
Mounting Torque	—	8	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Note 1) (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
Peak On-State Voltage (I_{TM} = 35 A Peak, Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.4	1.85	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	I_{GT}				mA
MT2(+), G(+); MT2(−), G(−); MT2(+), G(−)		—	20	50	
MT2(−), G(+)		—	30	80	
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	V_{GT}				Volts
MT2(+), G(+); MT2(−), G(−); MT(+), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.3	2.5	
(V_D = Rated V_{DRM}, T_J = 125°C, R_L = 10 k) All Trigger Modes		0.2	0.4	—	
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	10	50	mA
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 35 A Peak, I_G = 200 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C)	dv/dt	—	40	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 35 A Peak, Commutating di/dt = 13.4 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs

Note 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

3

FIGURE 1 — RMS CURRENT DERATING

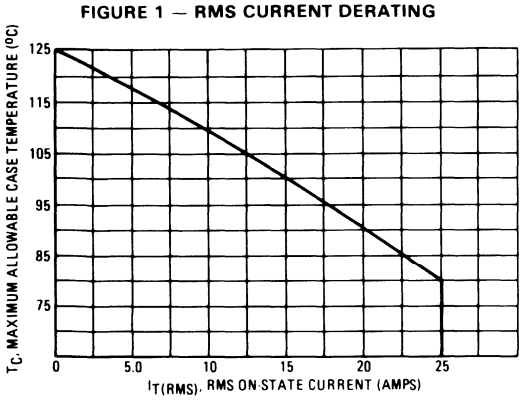


FIGURE 2 — ON-STATE POWER DISSIPATION

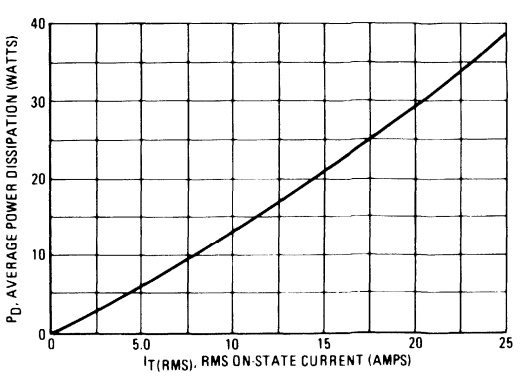


FIGURE 3 — GATE TRIGGER CURRENT

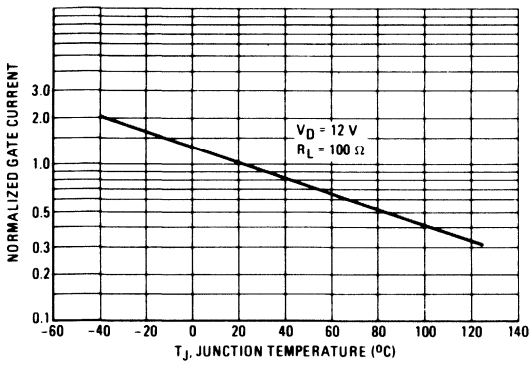


FIGURE 4 — GATE TRIGGER VOLTAGE

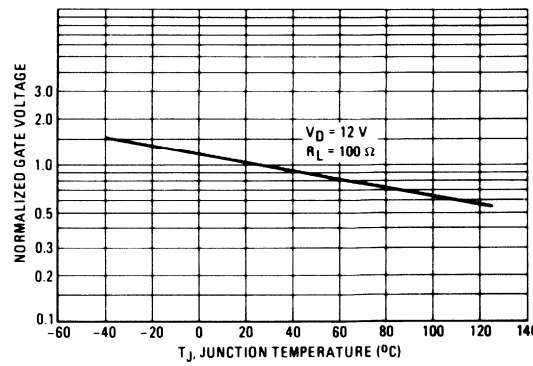


FIGURE 5 — HOLD CURRENT

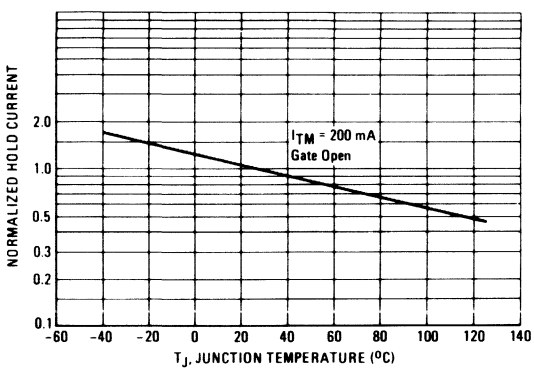
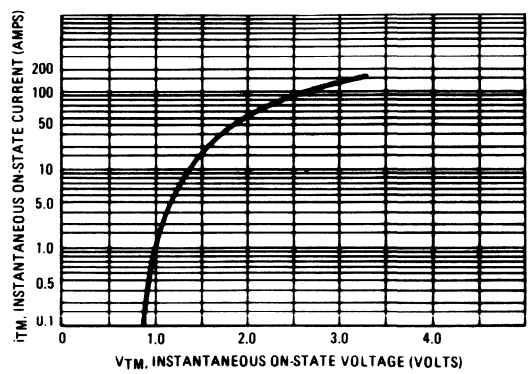


FIGURE 6 — ON-STATE CHARACTERISTICS



3

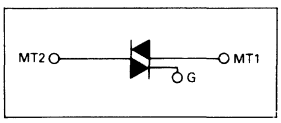
MAC223AFP Series

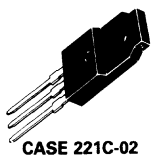
Triacs
Silicon Bidirectional Triode Thyristors

. . . designed primarily for full-wave ac control applications, such as lighting systems, heater controls, motor controls and power supplies; or wherever full-wave silicon-gate-controlled devices are needed.

- Off-State Voltages to 800 Volts
- All Diffused and Glass Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged Thermowatt Construction for Thermal Resistance and High Heat Dissipation
- Gate Triggering Guaranteed in Four Modes

ISOLATED TRIACs THYRISTORS 25 AMPERES RMS 100–800 VOLTS





CASE 221C-02 STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC223A4FP MAC223A6FP MAC223A8FP MAC223A10FP	V_{DRM}	 200 400 600 800	Volts
On-State RMS Current (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz, Note 2	$I_{T(RMS)}$	25	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_J = +125°C) preceded and followed by rated current	I_{TSM}	250	Amps
Circuit Fusing (T_J = −40 to 125°C; t = 8.3 ms)	I^2t	260	A^2s
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current (t ≤ 2 μs)	I_{GM}	2	Amps
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±10	Volts
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque	—	8	in/lb

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current, Note 1 T_J = 25°C (V_D = Rated V_{DRM}, T_J = 125°C	I_{DRM}	— —	— —	10 2	μA mA
Peak On-State Voltage (I_{TM} = 35 A Peak; Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%	V_{TM}	—	1.4	1.85	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(−), G(−), MT2(+), G(−) MT2(−), G(+)	I_{GT}	 — —	 20 30	 50 80	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(−), G(−), MT2(+), G(−) MT2(−), G(+) (V_D = Rated V_{DRM}, T_J = 125°C, R_L = 10 k) All Trigger Modes	V_{GT}	 — — 0.2	 1.1 1.3 0.4	 2 2.5 —	Volts
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	10	50	mA
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 35 A Peak, I_G = 200 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C)	dv/dt	—	40	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 35 A Peak, Commutating di/dt = 13.4 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs

NOTE 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

3

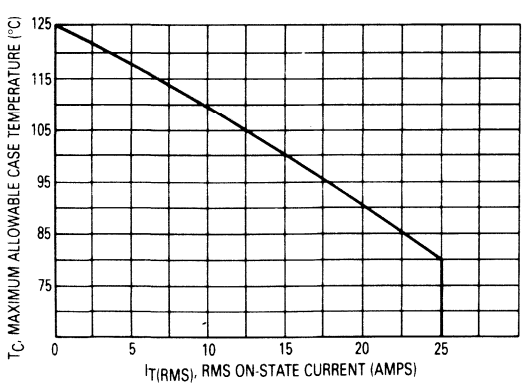


Figure 1. RMS Current Derating

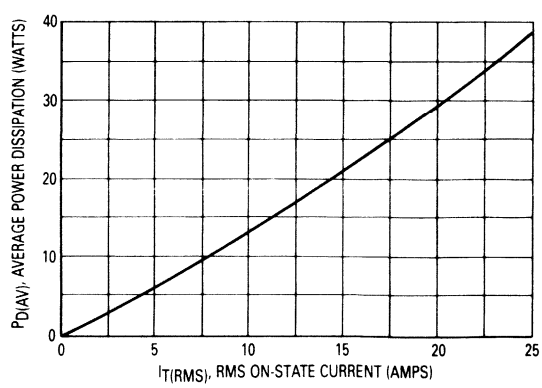


Figure 2. On-State Power Dissipation

TYPICAL CHARACTERISTICS

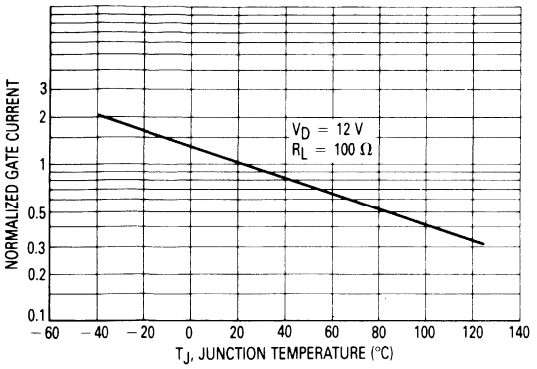


Figure 3. Gate Trigger Current

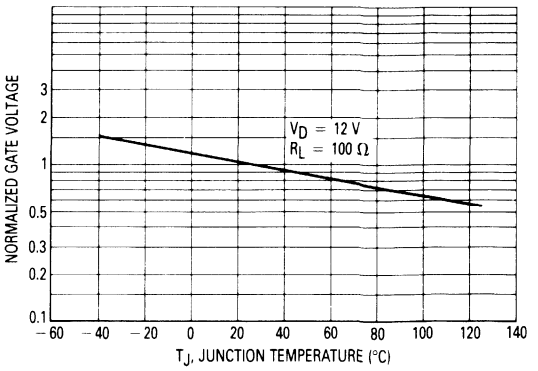


Figure 4. Gate Trigger Voltage

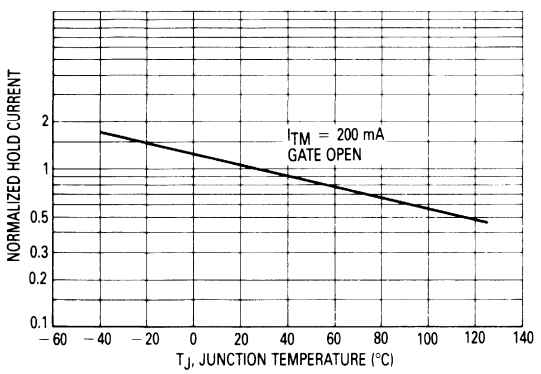


Figure 5. Hold Current

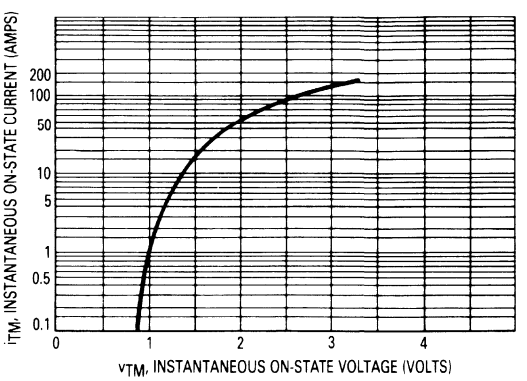


Figure 6. On-State Characteristics

3

Triacs

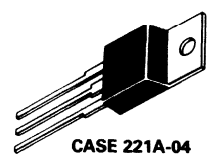
Silicon Bidirectional 40 Amperes RMS Triode Thyristors

MAC224A Series

. . . designed primarily for full-wave ac control applications such as lighting systems, heater controls, motor controls and power supplies.

- Blocking Voltage to 800 Volts
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Gate Triggering Guaranteed in Four Modes

TRIACs
40 AMPERES RMS
200 thru 800 VOLTS



CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = −40 to 125°C), Note 1 (1/2 Sine Wave 50 to 60 Hz, Gate Open)	V_{DRM}		Volts
MAC224A4		200	
6		400	
8		600	
10		800	
On-State RMS Current (T_C = 75°C), Note 2 (Full Cycle Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	40	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = 125°C)	I_{TSM}	350	Amps
Circuit Fusing (T_J = −40 to 125°C; t = 8.3 ms)	I^2t	500	A^2s
Peak Gate Current (t ≤ 2 μs)	I_{GM}	±2	Amps
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±10	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = 75°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	Watts

Notes: 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage. (cont.)
2. This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents. (See Figure 1 for maximum case temperatures.)

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−40 to 125	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C
Mounting Torque	—	8	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	— —	— —	10 2	μA mA
Peak On-State Voltage (I_{TM} = 56 A Peak, Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.4	1.85	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(+), G(−); MT2(+), G(−) MT2(−), G(+)	I_{GT}	— —	25 40	50 80	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(−), G(−); MT(+), G(−) MT2(−), G(+)	V_{GT}	— —	1.1 1.3	2 2.5	Volts
Gate Non-Trigger Voltage (V_D = Rated V_{DRM}, T_J = 125°C, R_L = 10 k) All Trigger Modes	V_{GD}	0.2	—	—	Volts
Holding Current (V_D = 12 Vdc, Gate Open)	I_H	—	30	75	mA
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 56 A Peak, I_G = 200 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C)	dv/dt	—	50	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 56 A Peak, Commutating di/dt = 13.4 A/ms, Gate Unenergized, T_C = 75°C)	dv/dt(c)	—	5	—	V/μs

3

FIGURE 1 — RMS CURRENT DERATING

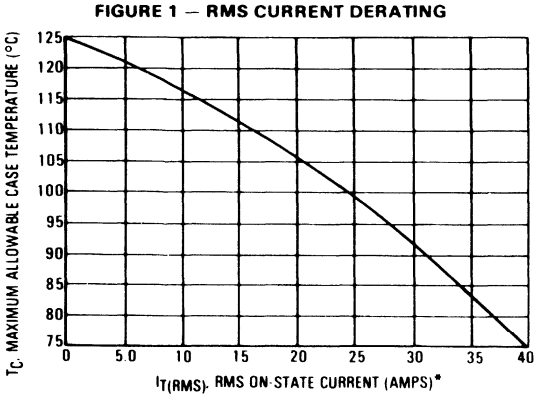
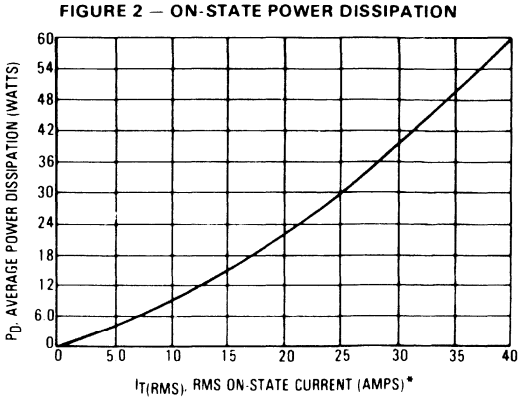


FIGURE 2 — ON-STATE POWER DISSIPATION



*This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents.

FIGURE 3 — GATE TRIGGER CURRENT

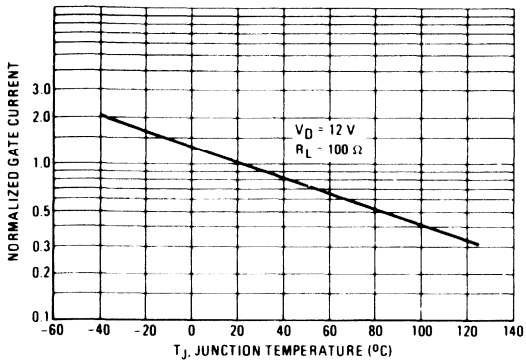


FIGURE 4 — GATE TRIGGER VOLTAGE

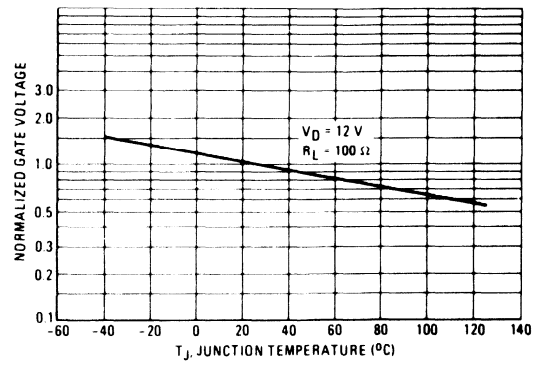


FIGURE 5 — HOLDING CURRENT

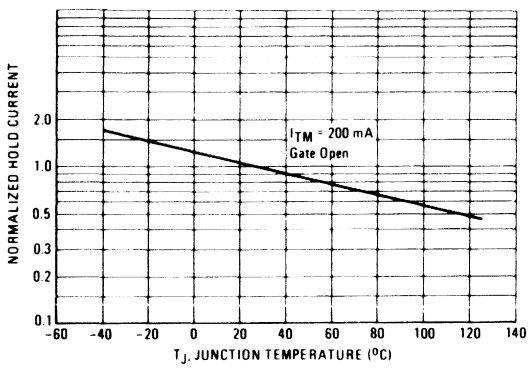


FIGURE 6 — ON-STATE CHARACTERISTICS

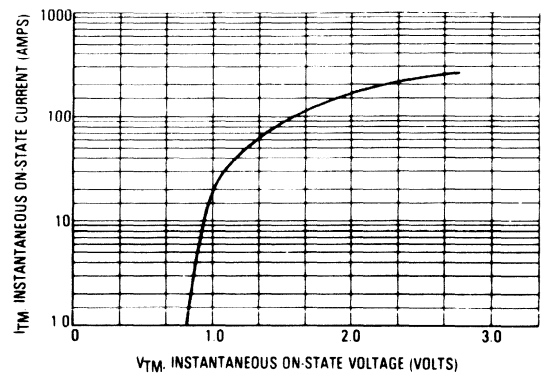
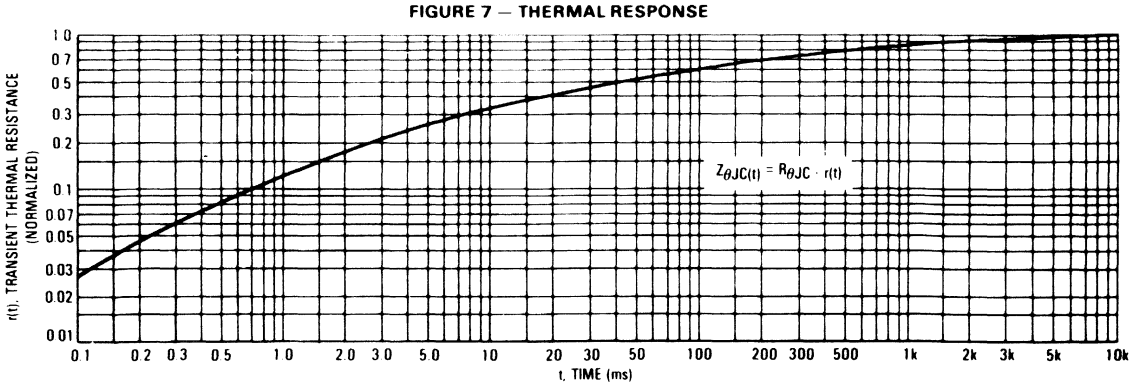


FIGURE 7 — THERMAL RESPONSE



3

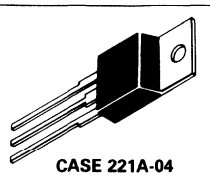
Triacs
Silicon Bidirectional Triode Thyristors

MAC228A Series

TRIACs
8 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for industrial and consumer applications for full wave control of ac loads such as appliance controls, heater controls, motor controls, and other power switching applications.

- Four Mode Triggering for Drive Circuits that Source Current
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal resistance and High Heat Dissipation
- Center Gate Geometry for Uniform Current Spreading



CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 (T_J = −40 to 110°C) 1/2 Sine ave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC228A4		200	
A6		400	
A8		600	
A10		800	
On-State RMS Current (T_C = 80°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	8	Amps
Peak Non-Repetitive Surge Current (One Full Cycle 60 Hz, T_J = 110°C)	I_{TSM}	80	Amps
Circuit Fusing (T_J = −40 to 110°C, t = 8.3 ms)	I^2t	40	A^2s
Peak Gate Current (t ≤ 2 μs)	I_{GM}	±2	Amps
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±10	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20	Watts

Note 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage. (cont.)

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	−40 to 110	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C
Mounting Torque		8	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 110°C		—	—	2	mA
Peak On-State Voltage (I_{TM} = 11 A Peak, Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.5	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	I_{GT}				mA
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−)		—	—	5	
MT2(−), G(+)		—	—	10	
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	V_{GT}				Volts
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−)		—	—	2	
MT2(−), G(+)		—	—	2.5	
(V_D = Rated V_{DRM}, T_C = 110°C, R_L = 10 k) MT2(+), G(+); MT2(+), G(−); MT2(−), G(−); MT2(−), G(+)		0.2	—	—	
Holding Current (V_D = 12 Vdc, I_{TM} = 200 mA, Gate Open)	I_H	—	—	15	mA
Gate-Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 16 A Peak, I_G = 30 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 110°C)	dv/dt	—	25	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 11 A Peak, Commutating di/dt = 5.8 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs

FIGURE 1 — RMS CURRENT DERATING

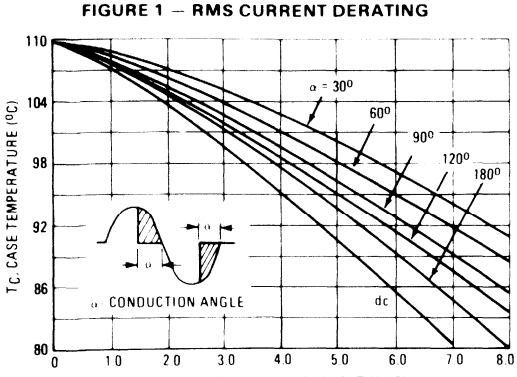
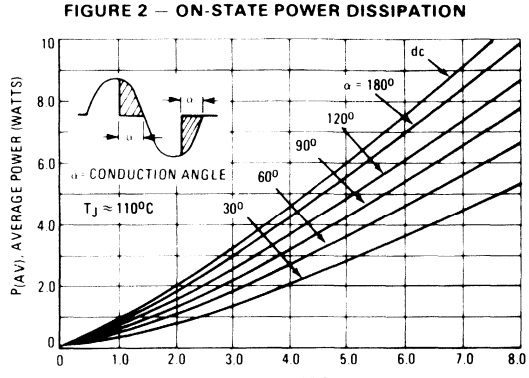


FIGURE 2 — ON-STATE POWER DISSIPATION



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- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal resistance and High Heat Dissipation
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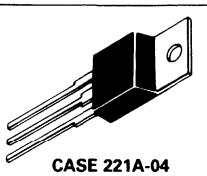


CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 (T_J = −40 to 110°C) 1/2 Sine ave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC229A4		200	
A6		400	
A8		600	
A10		800	
On-State RMS Current (T_C = 80°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	8	Amps
Peak Non-Repetitive Surge Current (One Full Cycle 60 Hz, T_J = 110°C)	I_{TSM}	80	Amps
Circuit Fusing (T_J = −40 to 110°C, t = 8.3 ms)	I^2t	40	A^2s
Peak Gate Current (t ≤ 2 μs)	I_{GM}	±2	Amps
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±10	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20	Watts

Note 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

(cont.)

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	−40 to 110	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C
Mounting Torque		8	in. lb.

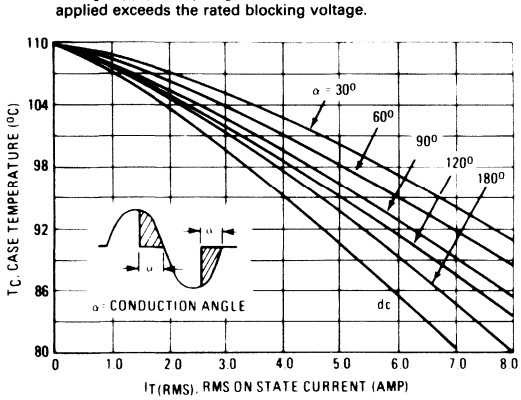
THERMAL CHARACTERISTICS

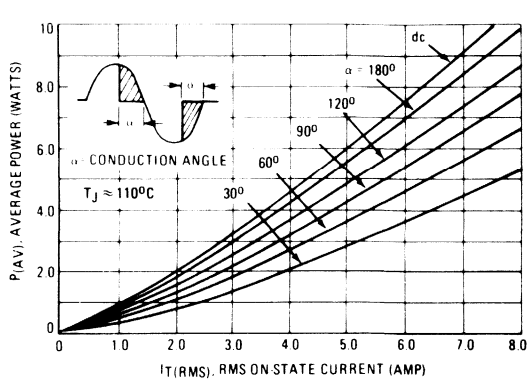
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current, Note 1 (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 110°C		—	—	2	mA
Peak On-State Voltage (I_{TM} = 11 A Peak, Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.5	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	I_{GT}				mA
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−)		—	—	10	
MT2(−), G(+)		—	—	20	
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	V_{GT}				Volts
MT2(+), G(+); MT2(+), G(−); MT2(−), G(−)		—	—	2	
MT2(−), G(+)		—	—	2.5	
(V_D = Rated V_{DRM}, T_C = 110°C, R_L = 10 k) MT2(+), G(+); MT2(+), G(−); MT2(−), G(−); All types		0.2	—	—	
MT2(−), G(+) MAC229 series		0.2	—	—	
Holding Current (V_D = 12 Vdc, I_{TM} = 200 mA, Gate Open)	I_H	—	—	15	mA
Gate-Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 16 A Peak, I_G = 30 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 110°C)	dv/dt	—	25	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 11 A Peak, Commutating di/dt = 5.8 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs

Note 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.





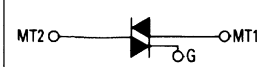
Triacs
Silicon Bidirectional Triode Thyristors

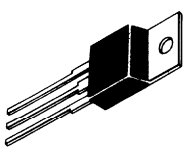
MAC310A Series

TRIACs
10 AMPERES RMS
200 thru 600 VOLTS

. . . designed primarily for industrial and consumer applications for full wave control of ac loads such as appliance controls, heater controls, motor controls, and other power switching applications.

- Sensitive Gate Triggering in Three Trigger Modes for AC Triggering or Sinking Current Sources (MAC310 series)
- Four Mode Triggering (10 mA) for Drive Circuits that Source Current (MAC310A series)
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation
- Center Gate Geometry for Uniform Current Spreading





CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = −40 to 110°C) Note 1. 1/2 Sine Wave to 50 to 60 Hz, Gate Open — MAC310A4 / MAC310A6 / MAC310A8	V_{DRM}	200 / 400 / 600	Volts
On-State RMS Current (T_C = 80°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	10	Amps
Peak Non-Repetitive Surge Current (One Full Cycle 60 Hz, T_J = 110°C)	I_{TSM}	100	Amps
Circuit Fusing (T_J = −40 to 110°C, t = 8.3 ms)	I^2t	40	A^2s
Peak Gate Current (t ≤ 2 μs)	I_{GM}	±2	Amps
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±10	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	Watts
Operating Junction Temperature Range	T_J	−40 to 110	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C
Mounting Torque	—	8	in-lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 110°C)	I_{DRM}	—	—	2	mA
Peak On-State Voltage (I_{TM} = 14 A Peak, Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.7	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(+), G(−); MT2(−), G(−); MT2(−), G(+)	I_{GT}	—	—	10	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(+), G(−); MT2(−), G(−); MT2(−), G(+) (V_D = Rated V_{DRM}, T_C = 110°C, R_L = 10 k) All Trigger Modes	V_{GT}	— 0.2	— —	2.5 —	Volts
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	—	15	mA
Gate-Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 14 A Peak, I_G = 30 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 110°C)	dv/dt	—	25	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 14 A Peak, Commutating di/dt = 14 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs

Note 1. Ratings apply for open gate conditions. Devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

3

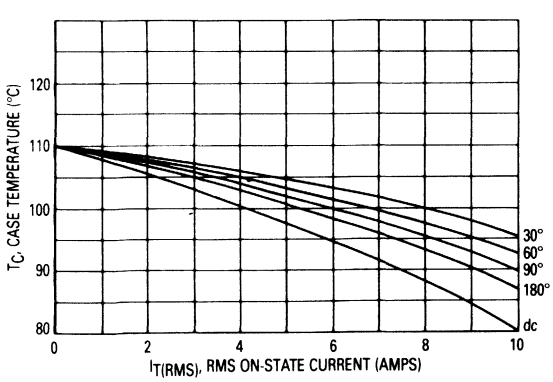


Figure 1. RMS Current Derating

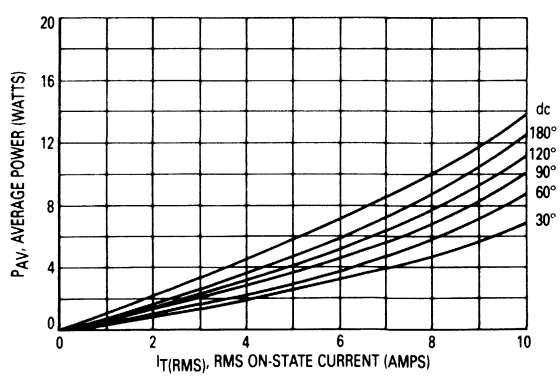


Figure 2. On-State Power Dissipation

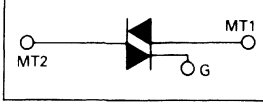
Triacs
Silicon Bidirectional Thyristors

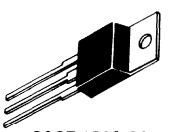
MAC320A Series

TRIACs
20 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Four Modes





CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC320A4 MAC320A6 MAC320A8 MAC320A10	V_{DRM}	 200 400 600 800	Volts
Peak Gate Voltage	V_{GM}	10	Volts
On-State Current RMS (T_C = +75°C) (Full Cycle, Sine Wave, 50 to 60 Hz)	$I_{T(RMS)}$	20	Amp
Peak Surge Current (One Full Cycle, 60 Hz, T_C = +75°C) preceded and followed by rated current	I_{TSM}	150	Amp
Peak Gate Power (T_C = +75°C, Pulse Width = 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +75°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM}, Gate Open	I_{DRM}				
T_J = 25°C		—	—	10	μA
T_J = +125°C		—	—	2	mA
Peak On-State Voltage (Either Direction) I_{TM} = 28 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	—	1.4	1.7	Volts
Gate Trigger Current (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms	I_{GT}				mA
MT2 (+), G(+); MT2 (+), G(−); MT2 (−), G(−)		—	—	50	
MT2 (−), G(+)		—	—	80	
Gate Trigger Voltage (Continuous dc) Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms	V_{GT}				Volts
MT2 (+), G(+); MT2 (+), G(−); MT2 (−), G(−)		—	0.9	2	
MT2 (−), G(+)		—	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J = +110°C MT2 (+), G(+); MT2 (−), G(−); MT2 (+), G(−); MT2 (−), G(+)		0.2	—	—	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H	—	6	40	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 28 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 28 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = +75°C	dv/dt(C)	—	5	—	V/μs

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FIGURE 1 — RMS CURRENT DERATING

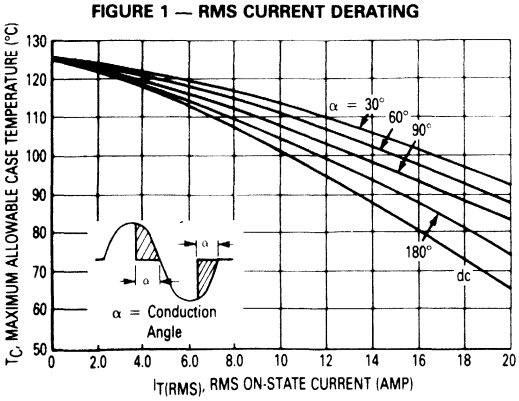

FIGURE 2 — ON-STATE POWER DISSIPATION

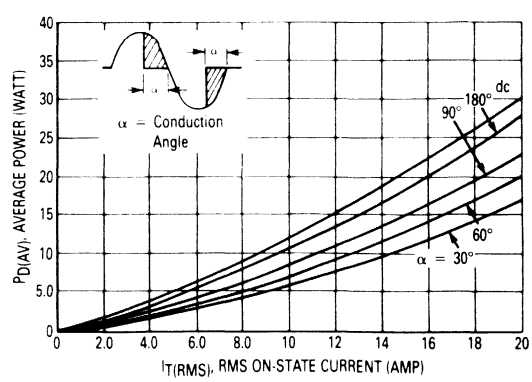

FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

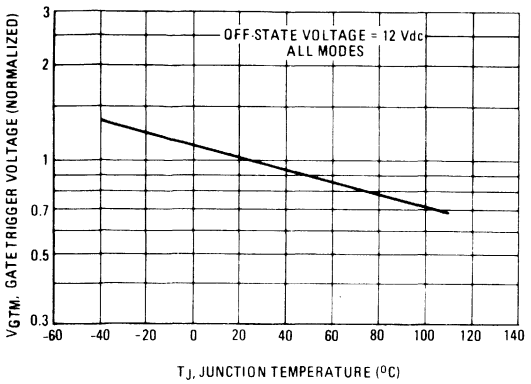

FIGURE 4 — TYPICAL GATE TRIGGER CURRENT

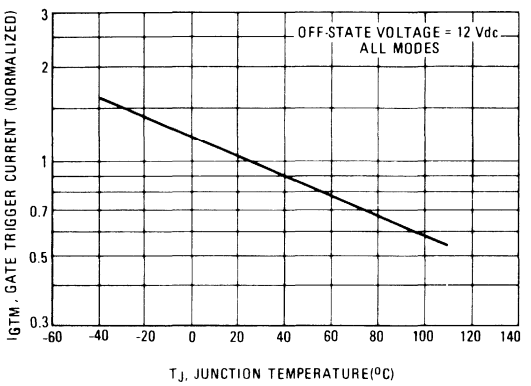

FIGURE 5 — MAXIMUM ON-STATE CHARACTERISTICS

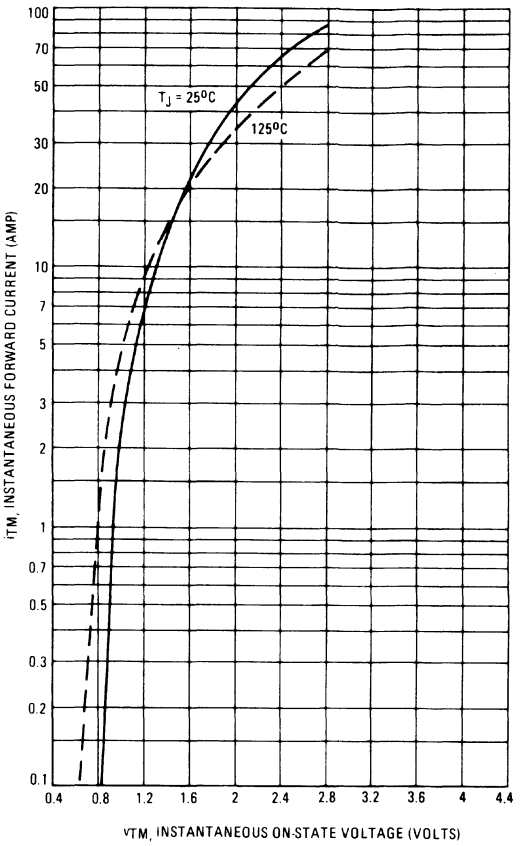

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FIGURE 6 — TYPICAL HOLDING CURRENT

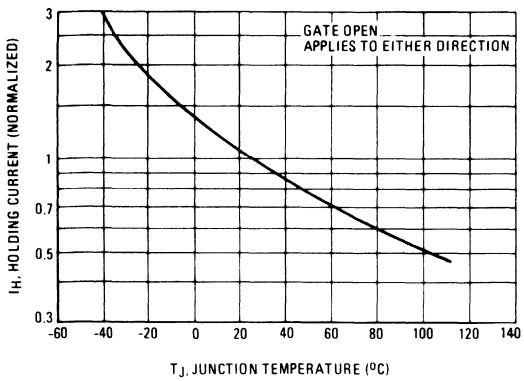


FIGURE 7 — MAXIMUM ON-REPETITIVE SURGE CURRENT

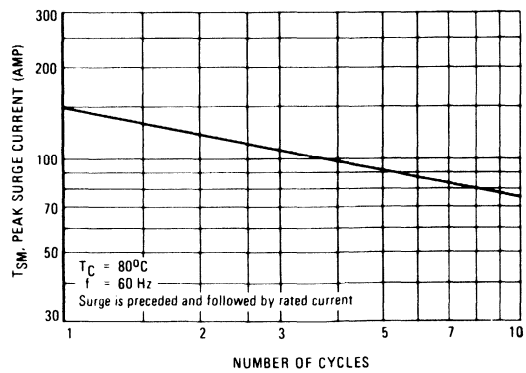
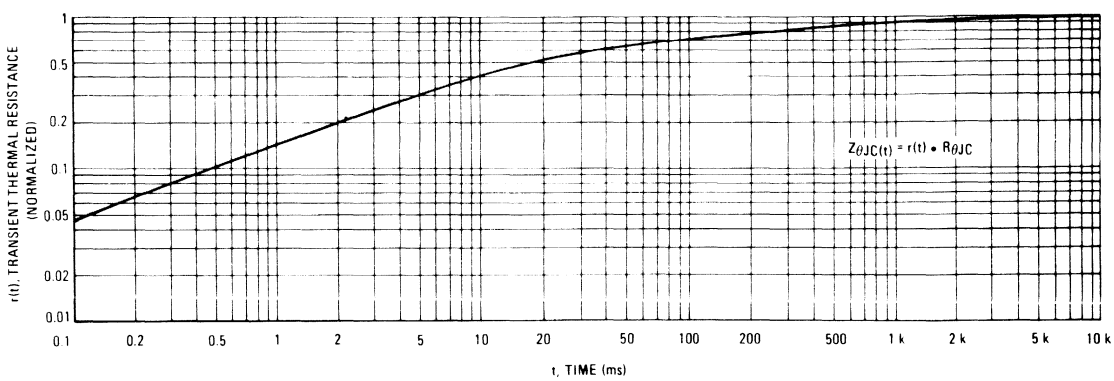


FIGURE 8 — THERMAL RESPONSE



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MAC320AFP Series

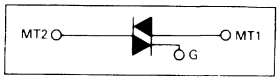
Triacs
Silicon Bidirectional Thyristors

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Four Modes

ISOLATED TRIACs THYRISTORS 20 AMPERES RMS 200–800 VOLTS

CASE 221C-02 STYLE 3



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open MAC320A4FP MAC320A6FP MAC320A8FP MAC320A10FP	V_{DRM}	 200 400 600 800	Volts
Peak Gate Voltage	V_{GM}	10	Volts
On-State RMS Current (T_C = +75°C) Full Cycle Sine Wave 50 to 60 Hz, Note 2	$I_{T(RMS)}$	20	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_C = +75°C) preceded and followed by rated current	I_{TSM}	150	Amps
Peak Gate Power (T_C = +75°C, Pulse Width = 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +75°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W
Thermal Resistance, Case to Sink	$R_{\theta CS}$	2.2 (typ)	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM}, Gate Open	I_{DRM}				
T_J = 25°C		—	—	10	μA
T_J = +125°C		—	—	2	mA
Peak On-State Voltage (Either Direction) I_{TM} = 28 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	—	1.4	1.7	Volts
Peak Gate Trigger Current	I_{GT}				mA
Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms					
Minimum Gate Pulse Width = 2 μs					
MT2(+), G(+)		—	—	50	
MT2(+), G(−)		—	—	50	
MT2(−), G(−)		—	—	50	
MT2(−), G(+)		—	—	80	
Peak Gate Trigger Voltage	V_{GT}				Volts
Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms					
Minimum Gate Pulse Width = 2 μs					
MT2(+), G(+)		—	0.9	2	
MT2(+), G(−)		—	0.9	2	
MT2(−), G(−)		—	1.1	2	
MT2(−), G(+)		—	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J = +110°C All Trigger Modes		0.2	—	—	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H	—	6	40	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 28 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 28 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = +75°C	dv/dt(c)	—	5	—	V/μs

3

TYPICAL CHARACTERISTICS

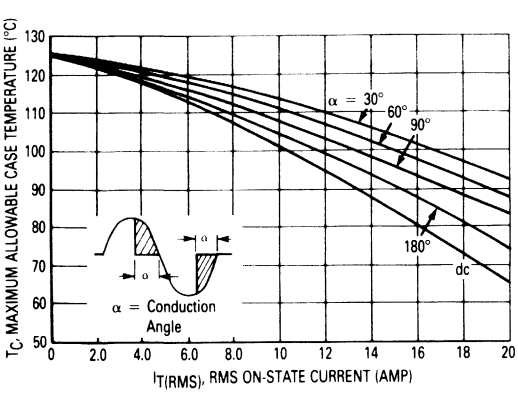

Figure 1. RMS Current Derating

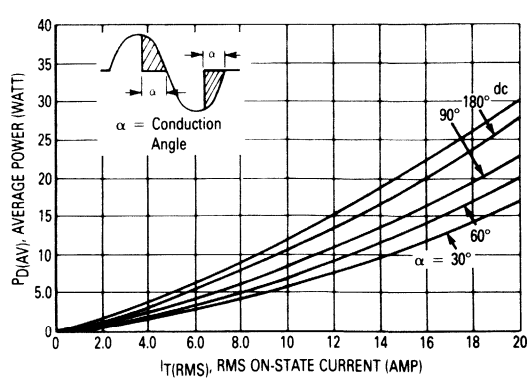

Figure 2. On-State Power Dissipation

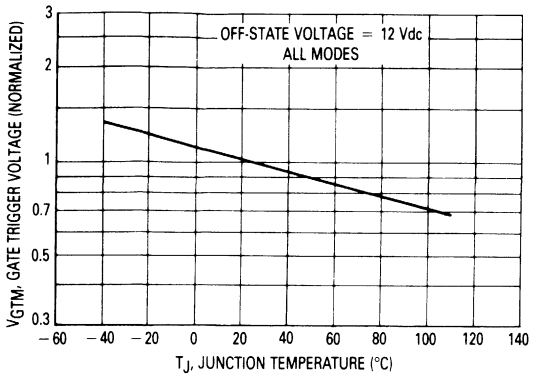

Figure 3. Typical Gate Trigger Voltage

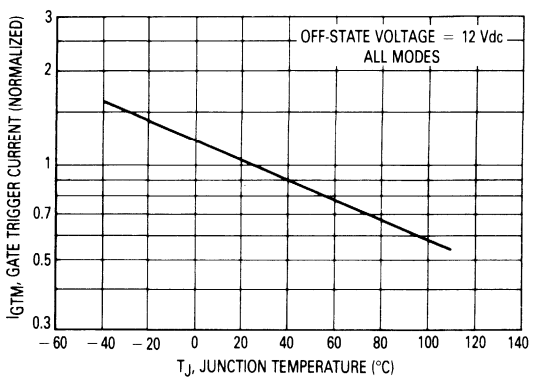

Figure 4. Typical Gate Trigger Current

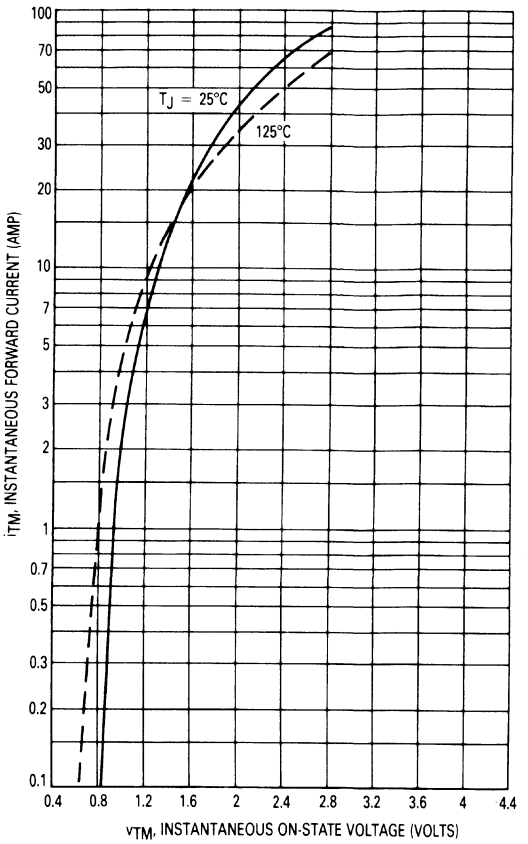

Figure 5. Maximum On-State Characteristics

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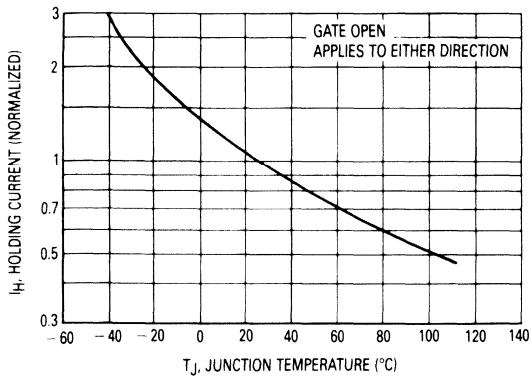


Figure 6. Typical Holding Current

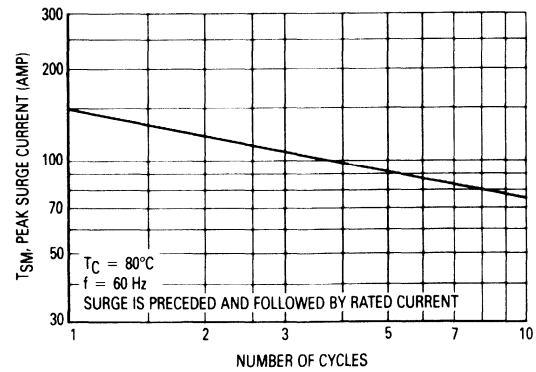


Figure 7. Maximum Nonrepetitive Surge Current

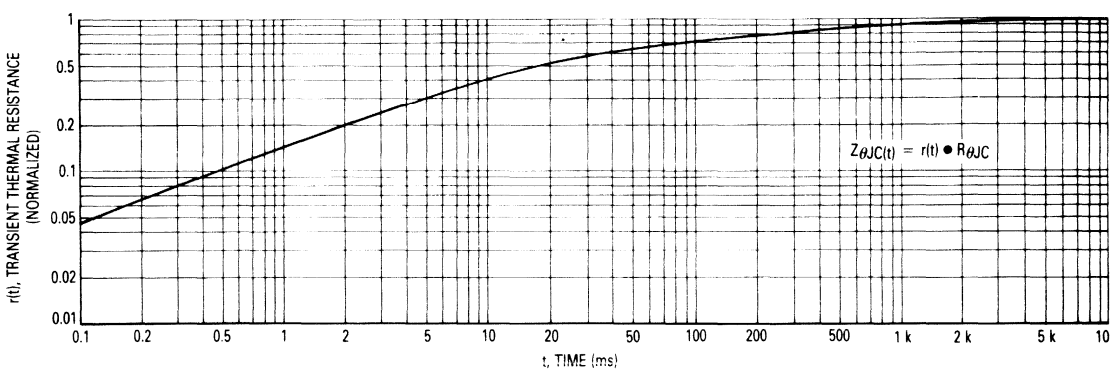


Figure 8. Thermal Response

3

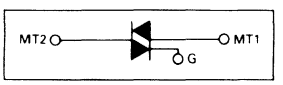
Triacs
Silicon Bidirectional Thyristors

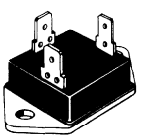
MAC625 Series
MAC635 Series

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 600 Volts
- TO-3 Isolated Mounting
- High Isolation Voltage — 2.5 kV rms
- High Commutating dv/dt — 6 V/μs Min
- UL Recognized — File # E69369

ISOLATED TRIACs
THYRISTORS
25/35 AMPERES RMS
200–600 VOLTS





CASE 383-01

MAXIMUM RATINGS

3

Rating		Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) (T_J = −40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open		V_{DRM}		Volts
	MAC625-4/635-4		200	
	MAC625-6/635-6		400	
	MAC625-8/635-8		600	
Peak Gate Voltage		V_{GM}	10	Volts
On-State RMS Current		$I_{T(RMS)}$		Amps
(T_C = +75°C) Full Cycle Sine Wave 50 to 60 Hz (2)	MAC625 Series		25	
(T_C = 58°C)	MAC635 Series		35	
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_C = +75°C) preceded and followed by rated current	MAC625 Series	I_{TSM}	250	Amps
	MAC635 Series		330	
Peak Gate Power (T_C = +75°C, Pulse Width = 2 μs)		P_{GM}	10	Watts
Average Gate Power (T_C = +75°C, t = 8.3 ms)		$P_{G(AV)}$	1	Watt
Peak Gate Current		I_{GM}	3	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)		$V_{(ISO)}$	2500	Volts
Operating Junction Temperature		T_J	−40 to +125	°C
Storage Temperature Range		T_{stg}	−40 to +125	°C
Circuit Fusing (T_C = +70°C, t = 1 to 8.3 ms)	MAC625 Series	I^2t	260	A^2s
	MAC635 Series		360	

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
(2) The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM}, Gate Open	I_{DRM} I_{RRM}	—	—	10	μA
Peak On-State Voltage (Either Direction) I_{TM} = 1.4 $I_{T(RMS)}$	V_{TM}	—	—	1.4	Volts
Peak Gate Trigger Current	I_{GT}				mA
Main Terminal Voltage = 6 Vdc, I_T = 1 A					
MT2(+), G(+)		—	—	50	
MT2(+), G(−)		—	—	50	
MT2(−), G(−)		—	—	50	
MT2(−), G(+)		—	—	—	
Peak Gate Trigger Voltage	V_{GT}				Volts
Main Terminal Voltage = 6 Vdc, I_T = 1 A					
Minimum Gate Pulse Width = 2 μs					
MT2(+), G(+)		—	—	3	
MT2(+), G(−)		—	—	3	
MT2(−), G(−)		—	—	3	
MT2(−), G(+)		—	—	—	
Gate Non-Trigger Voltage Main Terminal Voltage = 1/2 Rated V_{DRM}, R_L = 10 kΩ, T_J = 125°C	V_{GD}	0.2	—	—	Volts
Holding Current (Either Direction)	I_H	—	30	—	mA
Turn-On Time V_D = 1/2 Rated V_{DRM}, I_{TM} = Rated I_T, I_{GT} = 100 mA	t_{gt}	—	—	10	μs
Critical Rate of Rise of Commutation Voltage V_D = 2/3 Rated V_{DRM}, Commutating di/dt = 15 A/ms T_J = 125°C	dv/dt(c)	6	—	—	V/μs
dv/dt @ V_D = 2/3 V_{DRM}, T_J = 125°C	dv/dt	100	—	—	V/μs

3

TYPICAL CHARACTERISTICS

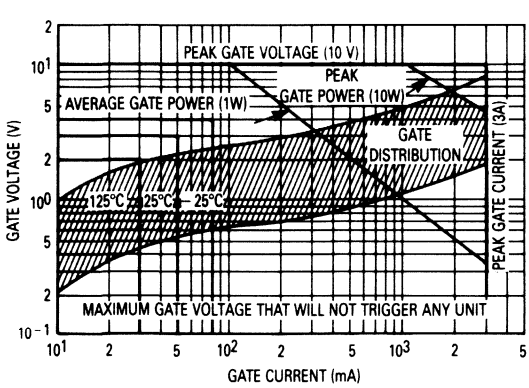


Figure 1. Gate Characteristics

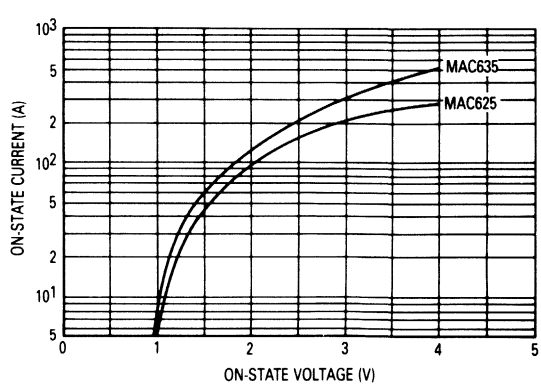


Figure 2. On-State Voltage

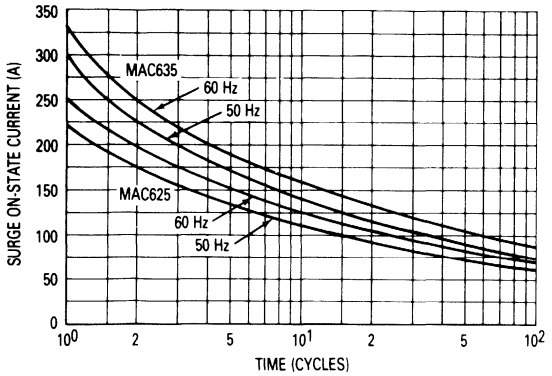


Figure 3. Surge On-State Current Rating (Non-Repetitive)

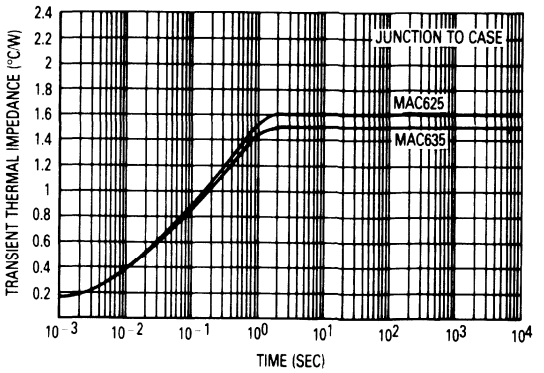


Figure 4. Transient Thermal Impedance

RMS On-State Current versus Maximum Power Dissipation

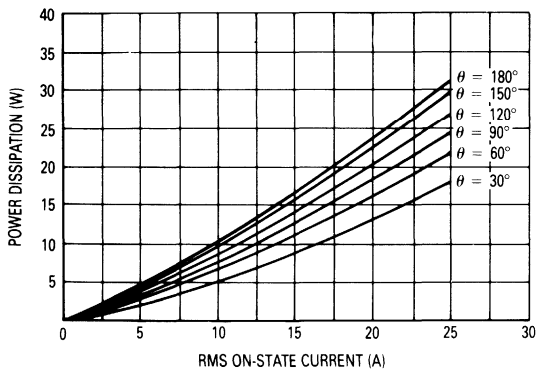


Figure 5. MAC625

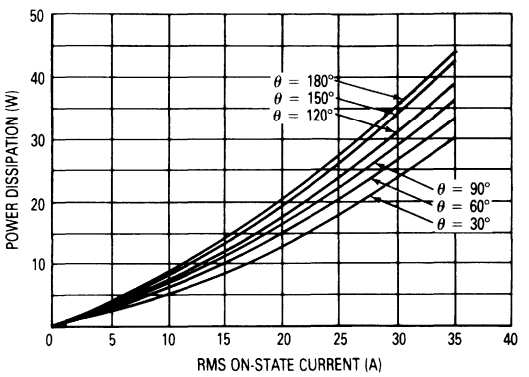


Figure 6. MAC635

RMS On-State Current versus Allowable Case Temperature

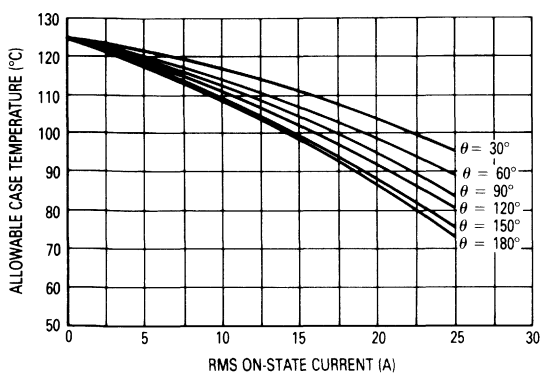


Figure 7. MAC625

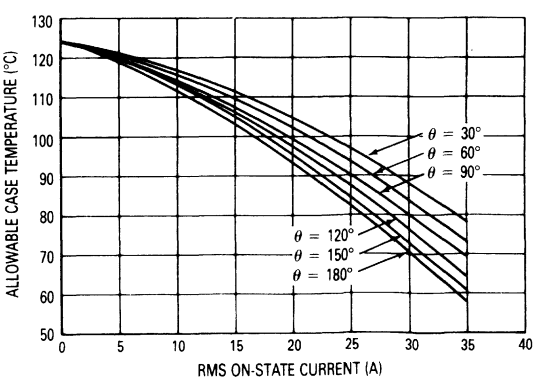


Figure 8. MAC635

Ambient Temperature versus RMS On-State Current

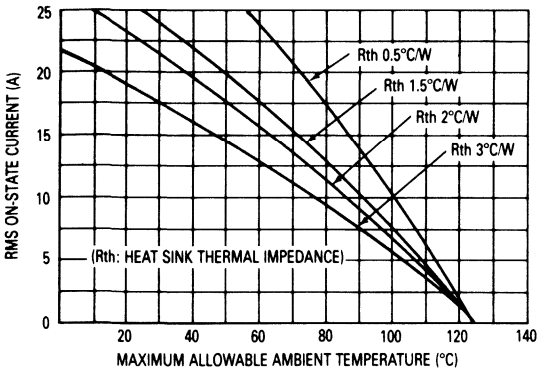


Figure 9. MAC625

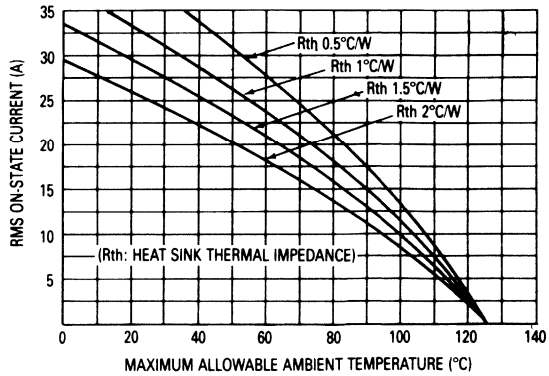


Figure 10. MAC635

3

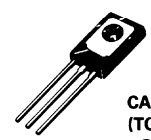
Triacs
Silicon Bidirectional Thyristors

. . . designed for full-wave ac power control applications, and specifically designed to be used in conjunction with MOC30XX opto couplers in circuits similar to that shown on page 206.

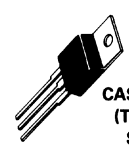
- Blocking Voltages to 400 Volts
- Load Current Controlled Up to 40 A
- Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Gate Triggering Guaranteed in Four Modes
- Designed for Use with MOC Series Optoisolators Having Triac Driver Outputs

MAC3010
MAC3020
MAC3030
MAC3040
Series

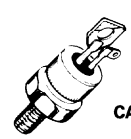
TRIACs
4, 8, 15, 25 and 40
AMPERES RMS
250 thru 400 VOLTS



CASE 77-05
(TO-225AA)
STYLE 5
-4



CASE 221A-04
(TO-220AB)
STYLE 4
-8, -15, -25



CASE 263-04
STYLE 2
-40

CASE 311-02
STYLE 2
-401

3

MAXIMUM RATINGS

Rating	Symbol	Current Ratings					Unit
		-4	-8	-15	-25	-40 -401	
On-State RMS Current (see Figure 1) (Full Cycle Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	4	8	15	25	40	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_J = 110°C)	I_{TSM}	30	80	150	250	300	Amps
Circuit Fusing Considerations (T_J = −40 to +110°C, t = 8.3 ms)	I^2t	3.6	26	90	260	370	A^2s
Peak Gate Voltage (t ≤ 2 μs)	V_{GM}	±5	±10	±10	±10	±10	Volts
Peak Gate Power (t ≤ 2 μs)	P_{GM}	10	20	20	20	20	Watts
Average Gate Power (T_C = 80°C, t ≤ 8.3 ms)	$P_{G(AV)}$	0.5	0.5	0.5	0.5	0.5	Watts
Peak Gate Current (t ≤ 2 μs)	I_{GM}	11	12	12	12	12	Amps
Operating Junction Temperature Range	T_J	*	−40 to +125			*	°C
Storage Temperature Range	T_{stg}	−40 to +150					°C
Mounting Torque	—	6	8	8	8	30	in. lb.
MAC3010/MAC3030, Note 1 MAC3020/MAC3040	V_{DRM}	250 400	250 400	250 400	250 400	250 400	Volts

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking voltage such that the voltage applied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	-4	-8	-15	-25	-40 -401	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	2.2	2	1.2	0.9	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	60	60	60	1	°C/W

*T_J −40° to +100°C.

-8, -15, -25 CURRENT RATINGS

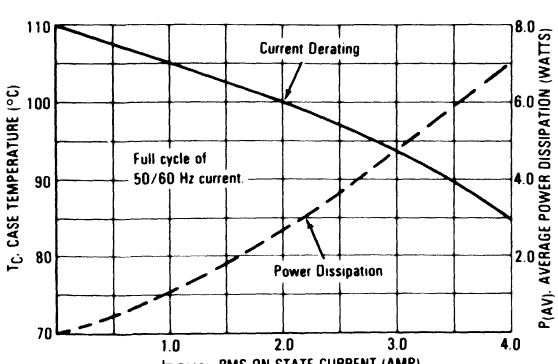
ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
Peak On-State Voltage (I_{TM} = $\sqrt{2}$ $I_{T(RMS)}$ A Peak; Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}				Volts
MAC3030-8		—	—	1.6	
MAC3030-15		—	—	1.6	
MAC3030-25		—	—	1.85	
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ohms) MT2(+), G(+); MT2(−), G(−) All Types	I_{GT}	—	—	40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ohms)	V_{GT}				Volts
MT2(+), G(+); MT2(−), G(−) All Types		—	—	2	
(T_J = 125°C, R_L = 10 k Ohms) MT2(+), G(+); MT1(−), G(−) All Types		0.2	—	—	
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	—	40	mA
Gate Controlled Turn-On Time (I_{TM} = 2 $I_{T(RMS)}$ A Peak, I_G = 100 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (I_{TM} = 2 $I_{T(RMS)}$ A Peak, Commutating di/dt = 0.52 $I_{T(RMS)}$ A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (Exponential Waveform, T_C = 125°C)	dv/dt	—	40	—	V/μs

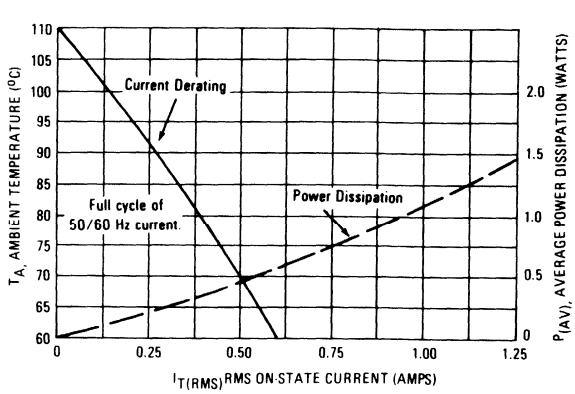
3

FIGURE 1 — CURRENT DERATING AND POWER DISSIPATION

A. REFERENCE: CASE TEMPERATURE



B. REFERENCE: AMBIENT TEMPERATURE



-8, -15, -25 CURRENT RATINGS

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
Peak On-State Voltage (I_{TM} = $\sqrt{2}$ $I_{T(RMS)}$ A Peak; Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}				Volts
MAC3030-8		—	—	1.6	
MAC3030-15		—	—	1.6	
MAC3030-25		—	—	1.85	
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ohms) MT2(+), G(+); MT2(−), G(−) All Types	I_{GT}	—	—	40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ohms)	V_{GT}				Volts
MT2(+), G(+); MT2(−), G(−) All Types		—	—	2	
(T_J = 125°C, R_L = 10 k Ohms) MT2(+), G(+); MT1(−), G(−) All Types		0.2	—	—	
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	—	40	mA
Gate Controlled Turn-On Time (I_{TM} = 2 $I_{T(RMS)}$ A Peak, I_G = 100 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (I_{TM} = 2 $I_{T(RMS)}$ A Peak, Commutating di/dt = 0.52 $I_{T(RMS)}$ A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (Exponential Waveform, T_C = 125°C)	dv/dt	—	40	—	V/μs

3

FIGURE 2 — RMS CURRENT DERATING

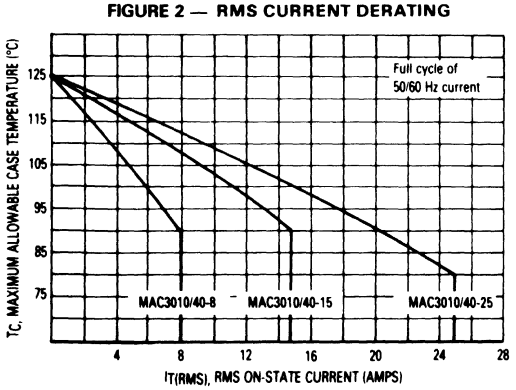
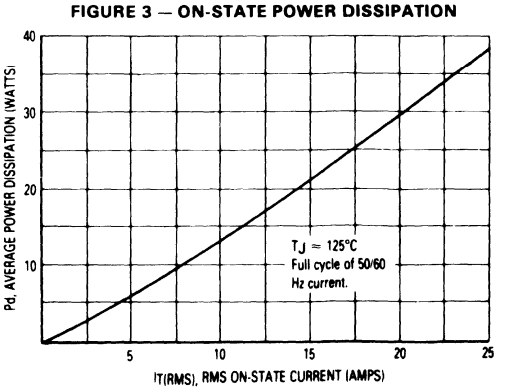


FIGURE 3 — ON-STATE POWER DISSIPATION



-40, -401 CURRENT RATINGS

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C T_J = 110°C	I_{DRM}, I_{RRM}	— —	— —	10 2	μA mA
Peak On-State Voltage (Either Direction) (I_{TM} = 56 A Peak; Pulse Width ≤ 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.85	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(−), G(−)	I_{GT}	—	—	40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+); MT2(−), G(−) (R_L = 10 kΩ, T_J = 110°C) MT2(+), G(+); MT1(−), G(−)	V_{GT}	— 0.2	— —	2 —	Volts
Holding Current (V_D = 12 V, I_{TM} = 200 mA, Gate Open)	I_H	—	—	50	mA
Gate Controlled Turn-On Time (I_{TM} = 56 A pk, I_G = 200 mA)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (I_{TM} = 56 A pk, Commutating di/dt = 22 A/ms, Gate Unenergized, T_C = 60°C)	dv/dt(c)	—	5	—	V/μs
Critical Rate of Rise of Off-State Voltage (Exponential Waveform, T_C = 110°C)	dv/dt	—	30	—	V/μs

3

FIGURE 4 — RMS CURRENT DERATING

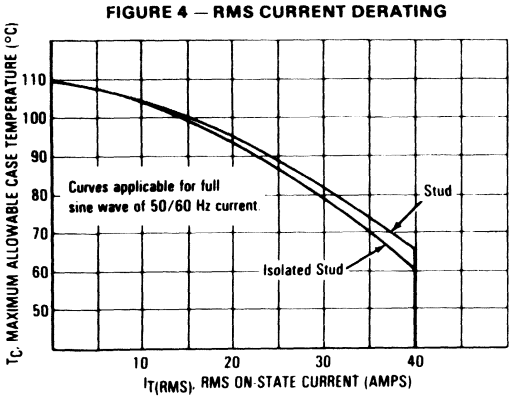
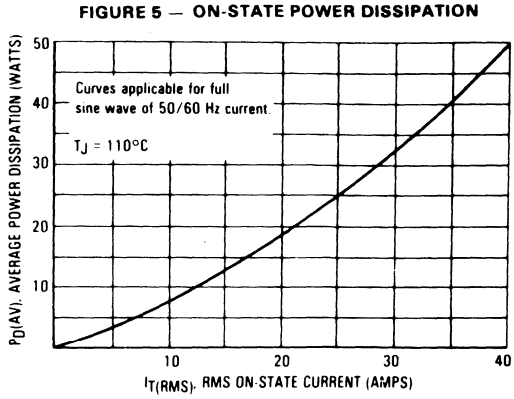


FIGURE 5 — ON-STATE POWER DISSIPATION



USING THE MOC OPTO COUPLERS AND MAC TRIAC SERIES DEVICES

The MOCXXXX Opto Coupler can be used as a triac driver with MACXXXX-X by selecting R_C to limit the surge current thru the coupler and yet supply enough gate drive to the triac to guarantee complete turn on. The maximum surge current rating of the coupler (I_{TSM}) determines the minimum value of R_C:

$$R_C\,(\text{min}) = \frac{V_{in}(pk)}{I_{TSM}\,(\text{coupler})}$$

For high line 110 Vac nominal voltage: $V_{in}(pk) = 187$ V.

$$R_C\,(\text{min}) = \frac{187\text{ V}}{1.2\text{ A}} = 155.8\text{ ohms}$$

In practice, this would be a 180 ohm resistor.

The maximum gate drive required determines the maximum value of R_C:

$$R_C\,(\text{max}) = \frac{V_{IH}-V_{TM}}{I_{GT}(\text{triac})}$$

Where V_{IH} is the inhibit voltage of the coupler and V_{TM} is the on-state voltage of the triac in the coupler.

For the MOC3040 and MAC3040 −25 V_{IH} = 40 V. V_{TM} = 3.0 V, and I_{GT} = 40 mA.

$$R_C\,(\text{max}) = \frac{40\text{ V}-3.0\text{ V}}{40\text{ mA}} = 930\text{ ohms}$$

In practice, the gate is driven two or three times I_{GT} to guarantee complete turn on. R_C (max) would be 460 ohms or 310 ohms.

The line voltage at turn on is:

$$V_{\text{Line at turn on}} = R_C \cdot I_{GT} + V_{TM}(\text{coupler}) + V_{GT}(\text{triac})$$

For the above example V_{GT}(triac) = 2.0 V, I_{GT} = 80 mA, R_C = 210 ohms.

$$V_{\text{Line at turn on}} = (210)(0.08\text{ A}) + 3.0\text{ V} + 2.0\text{ V} = 22\text{ V}$$

Resistive Loads

Resistive heating elements and incandescent lamps are typical loads for the triac. Cold incandescent lamps can draw 5–6 times their hot RMS value on start up. The triac must be specified to sustain the repetitive surge (I_{TSM}). In practice, the RMS value is chosen at two times actual so the surge rating of the triac will be very high.

Inductive Loads

Motors, solenoids, and magnets are typical problem loads for the triac and coupler. Since the triac turns off as the current approaches zero, but the inductive voltage is still high, it appears to the triac as a rise in applied voltage. If this rate of rise in voltage exceeds the dv/dt commutating of the triac or the dv/dt static of the coupler, the triac will turn back on.

Snubber Network

When the dv/dt of the circuit exceeds the capability of the coupler or triac, a R_SC_S network is placed across the main terminals of the triac. In most applications the snubber used for the triac will also protect the coupler. The R_S also limits the energy from the C_S destroying the gate region on the first use of the triac.

Since the power factor of the board (cosine of the I-V phase shift) is not always known, a typical design can be a starting point for scope verification.

For power factor = 0.1, 110 V nominal line.

$$V_{\text{turn off voltage}} = V_{pk} \sin\phi \approx V_{pk} \approx 187\text{ V}$$

Setting the dv/dt $_C$ (triac) equal to the circuit $V_{Turn\ off}$ over the snubber time constant and solving for R_S:

$$dv/dt\ C\ (\text{triac}) = \frac{V_{Turn\ off}}{R_SC_S}$$

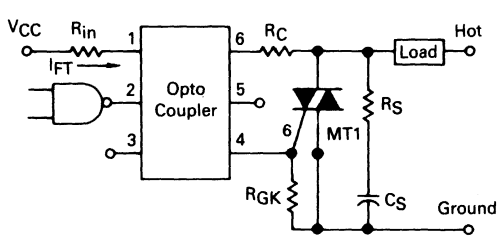
$$R_S = \frac{V_{Turn\ off}}{dv/dt\ (c)\ C_S}$$

For MAC3030-25 dv/dt (c) = 5.0 V/μs, and choosing C_S = 0.1 μF

$$R_S = \frac{187\text{ V}}{(5.0\text{ V}/\mu\text{s})\,(0.1\ \mu\text{F})}$$

$$R_S = 374\text{ ohms}$$

In practice, R_S is selected empirically. For more details see AN780A.



Silicon Bidirectional Switch (Plastic)

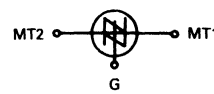
Bidirectional Diode Thyristors

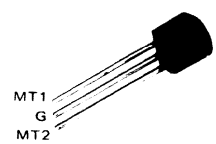
MBS4991
MBS4992
MBS4993

SBS (PLASTIC)

. . . designed for full-wave triggering in Triac phase control circuits, half-wave SCR triggering application and as voltage level detectors. Supplied in an inexpensive plastic TO-226AA package for high-volume requirements, this low-cost plastic package is readily adaptable for use in automatic insertion equipment.

- Low Switching Voltage — 8 Volts Typical
- Uniform Characteristics in Each Direction
- Low On-State Voltage — 1.7 Volts Maximum
- Low Off-State Current — 0.1 μA Maximum
- Low Temperature Coefficient — 0.02 %/°C Typical





CASE 29-04
(TO-226AA)
STYLE 12

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation	P_D	500	mW
DC Forward Current	I_F	200	mA
DC Gate Current (off-state only)	$I_G(off)$	5	mA
Repetitive Peak Forward Current (1% Duty Cycle, 10 μs Pulse Width, T_A = 100°C)	$I_{FM}(rep)$	2	Amps
Non-Repetitive Forward Current (10 μs Pulse Width, T_A = 25°C)	$I_{FM}(nonrep)$	6	Amps
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Switching Voltage	MBS4991 MBS4992, MBS4993	V_S	6 7.5	8 8	10 9	Vdc
Switching Current	MBS4991 MBS4992 MBS4993	I_S	— —	175 90 175	500 120 250	μAdc
Switching Voltage Differential (See Figure 10)	MBS4991 MBS4992, MBS4993	$\|V_{S1}-V_{S2}\|$	— —	0.3 0.1	0.5 0.2	Vdc
Gate Trigger Current (V_F = 5 Vdc, R_L = 1 k ohm)	MBS4992 MBS4993	I_{GF}	— —	— —	100 500	μAdc
Holding Current	MBS4991 MBS4992 MBS4993	I_H	— — —	0.7 0.2 0.3	1.5 0.5 0.75	mAdc
Off-State Blocking Current (V_F = 5 Vdc, T_A = 25°C) (V_F = 5 Vdc, T_A = 85°C) (V_F = 5 Vdc, T_A = 25°C) (V_F = 5 Vdc, T_A = 100°C)	 MBS4991 MBS4991 MBS4992, MBS4993 MBS4992, MBS4993	I_B	 — — — —	 0.08 2 0.08 6	 1 10 0.1 10	μAdc
Forward On-State Voltage (I_F = 175 mAdc) (I_F = 200 mAdc)	 MBS4991 MBS4992, MBS4993	V_F	 — —	 1.4 1.5	 1.7 1.7	Vdc
Peak Output Voltage (C_C = 0.1 μF, R_L = 20 ohms, (Figure 7)		V_O	3.5	4.8	—	Vdc
Turn-On Time (Figure 8)		t_{on}	—	1	—	μs
Turn-Off Time (Figure 9)		t_{off}	—	30	—	μs
Temperature Coefficient of Switching Voltage (−50 to +125°C)		T_C	—	+0.02	—	%/°C
Switching Current Differential (See Figure 10)		$I_{S1}-I_{S2}$	—	—	100	μA

3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SWITCHING VOLTAGE versus TEMPERATURE

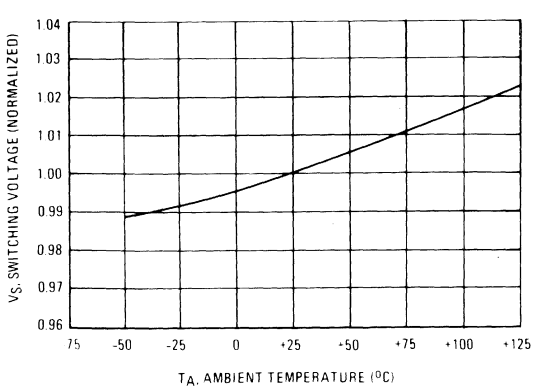


FIGURE 2 – SWITCHING CURRENT versus TEMPERATURE

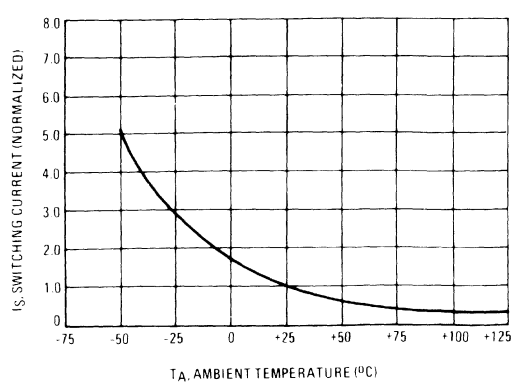


FIGURE 3 – HOLDING CURRENT versus TEMPERATURE

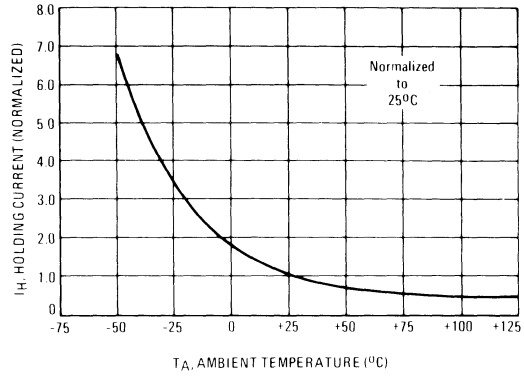


FIGURE 4 – OFF-STATE BLOCKING CURRENT versus TEMPERATURE

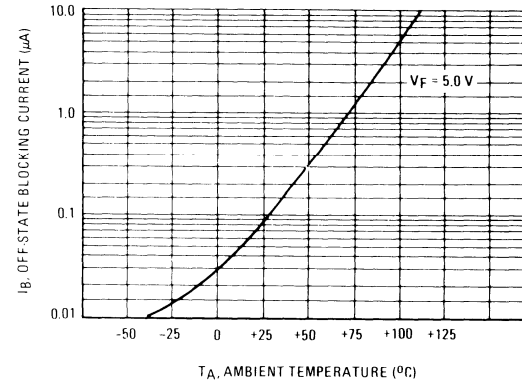


FIGURE 5 – ON-STATE VOLTAGE versus FORWARD CURRENT

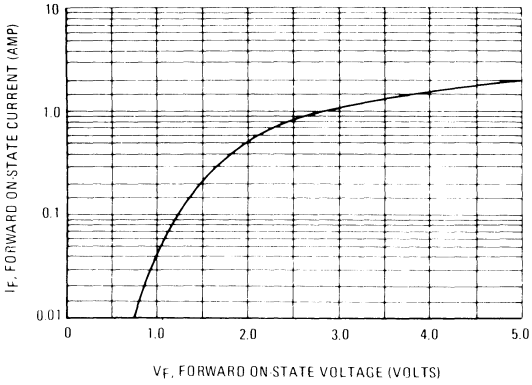


FIGURE 6 – PEAK OUTPUT VOLTAGE (FUNCTION OF R_L AND C_c)

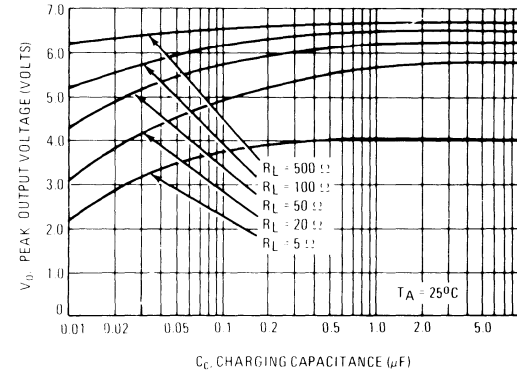


FIGURE 7 – PEAK OUTPUT VOLTAGE TEST CIRCUIT

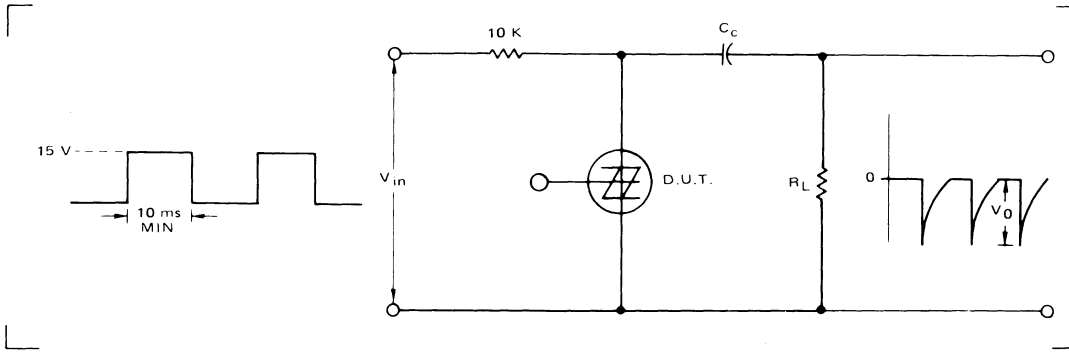
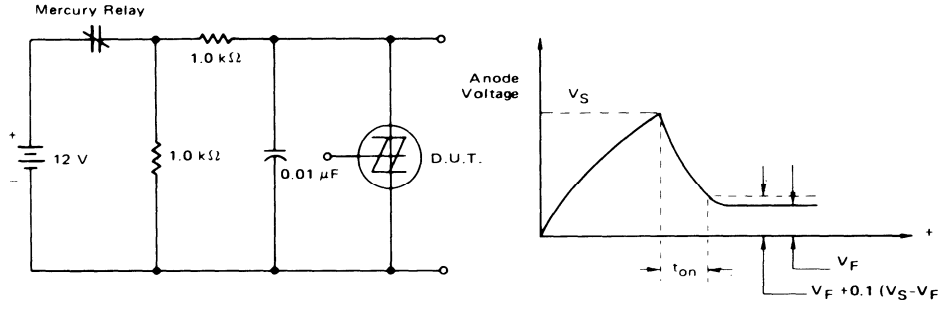
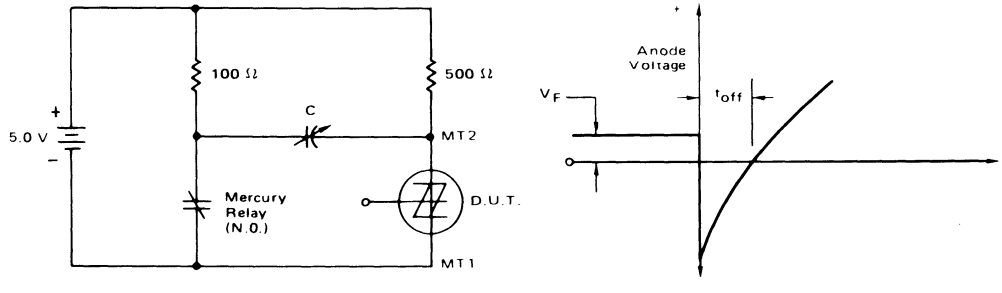


FIGURE 8 – TURN-ON TIME TEST CIRCUIT



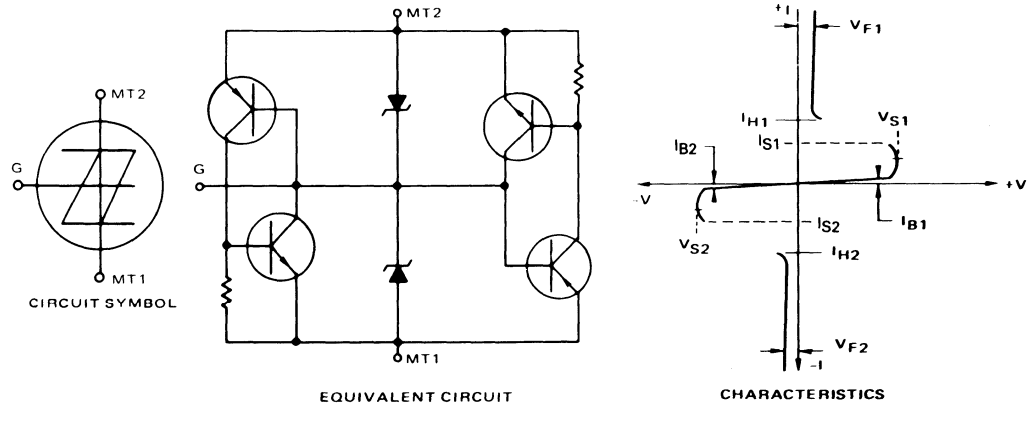
Turn-on time is measured from the time V_S is achieved to the time when the anode voltage drops to within 90% of the difference between V_S and V_F.

FIGURE 9 – TURN-OFF TIME TEST CIRCUIT



With the SBS in conduction and the relay contacts open, close the contacts to cause anode A2 to be driven negative. Decrease C until the SBS just remains off when anode A2 becomes positive. The turn off time, t_{off}, is the time from initial contact closure and until anode A2 voltage reaches zero volts.

FIGURE 10 – DEVICE EQUIVALENT CIRCUIT, CHARACTERISTICS AND SYMBOLS



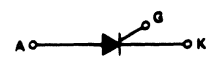
Plastic Silicon Controlled Rectifiers

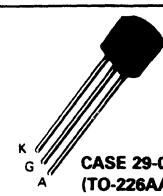
MCR22-2 thru 8

SCRs
1.5 AMPERES RMS
50 thru 600 VOLTS

. . . designed and tested for repetitive peak operation required for CD ignition, fuel ignitors, flash circuits, motor controls and low-power switching applications.

- 150 Amperes for 2 μs Safe Area
- High dv/dt
- Very Low VF at High Current
- Low-Cost TO-226AA





CASE 29-04
(TO-226AA)
STYLE 10

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Blocking Voltage	V_{RRM}		Volts
MCR22-2		50	
MCR22-3		100	
MCR22-4		200	
MCR22-6		400	
MCR22-8		600	
On-State Current RMS (All Conduction Angles)	$I_{T(RMS)}$	1.5	Amps
Peak Nonrepetitive Surge Current, T_A = 25°C (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	15	Amps
Circuit Fusing Considerations, T_A = 25°C (t = 2 to 8.3 ms)	I^2t	0.9	A^2s
Peak Gate Power, T_A = 25°C	P_{GM}	0.5	Watt
Average Gate Power, T_A = 25°C	$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current, T_A = 25°C (300 μs, 120 PPS)	I_{FGM}	0.2	Amp
Peak Reverse Gate Voltage	V_{RGM}	5	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Lead Solder Temperature (Lead Length ≥ 1/16″ from case, 10 s Max)	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	50	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	160	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 Ohms.)

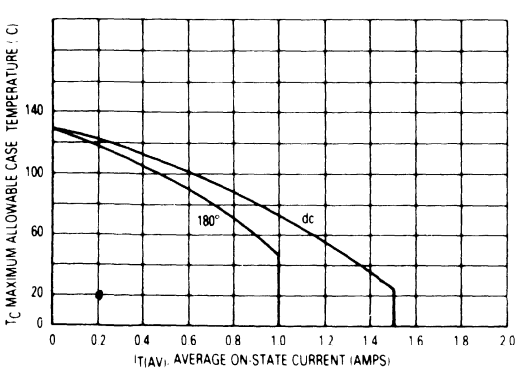
Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)		V_{DRM}				Volts
	MCR22-2		50	—	—	
	MCR22-3		100	—	—	
	MCR22-4		200	—	—	
	MCR22-6		400	—	—	
	MCR22-8		600	—	—	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM})	T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
	T_C = 125°C		—	—	200	μA
Forward "On" Voltage (I_{TM} = 1 A peak)		V_{TM}	—	1.2	1.7	Volts
Gate Trigger Current (Continuous dc), Note 1 (Anode Voltage = 6 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	—	30	200	μA
	T_C = −40°C		—	—	500	
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C	V_{GT}	—	—	0.8	Volts
	T_C = −40°C		—	—	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C	V_{GD}	0.1	—	—	
Holding Current (Anode Voltage = 12 Vdc)	T_C = 25°C	I_H	—	2	5	mA
	T_C = −40°C		—	—	10	
Forward Voltage Application Rate (T_C = 125°C)		dv/dt	—	25	—	V/μs
Turn-On Time		t_{on}	—	1.2	—	μs
Turn-Off Time		t_{off}	—	40	—	μs

Note 1. R_{GK} Current Not Included in Measurement.

3

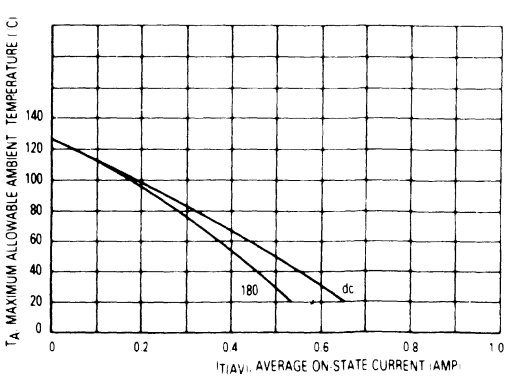
CURRENT DERATING

FIGURE 1 — MAXIMUM CASE TEMPERATURE



$R_{\theta JC}$ = 50°C/W
COOLING TIME = 3.0 ms
T_J = 125°C

FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE



$R_{\theta JA}$ = 160°C/W
COOLING TIME = 3.0 ms
T_J = 125°C

FIGURE 3 — TYPICAL FORWARD VOLTAGE

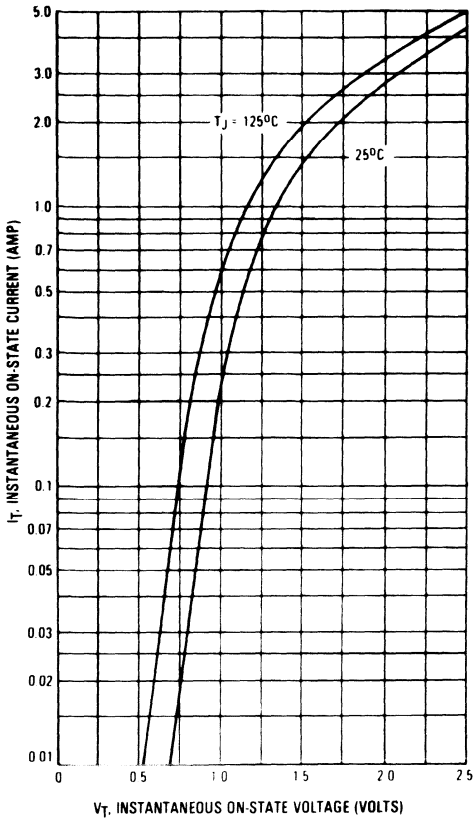


FIGURE 4 — PEAK REPETITIVE CAPACITOR DISCHARGE CURRENT

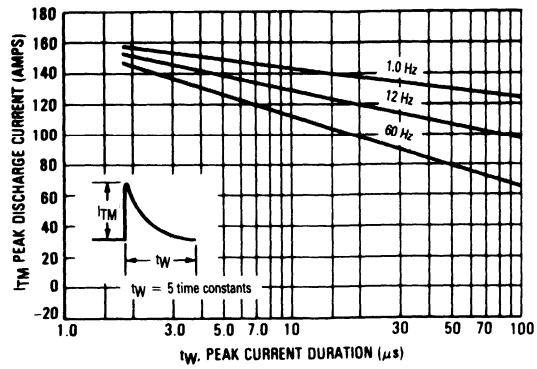


FIGURE 5 — PEAK REPETITIVE SINUSOIDAL CURVE

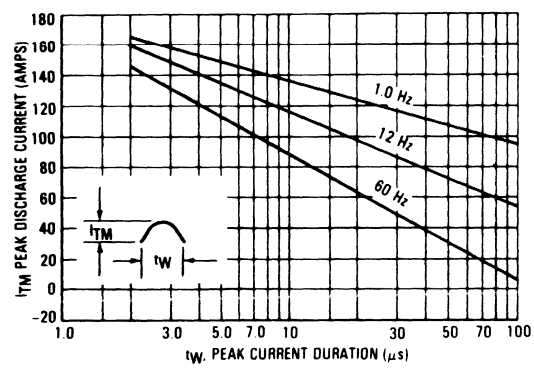
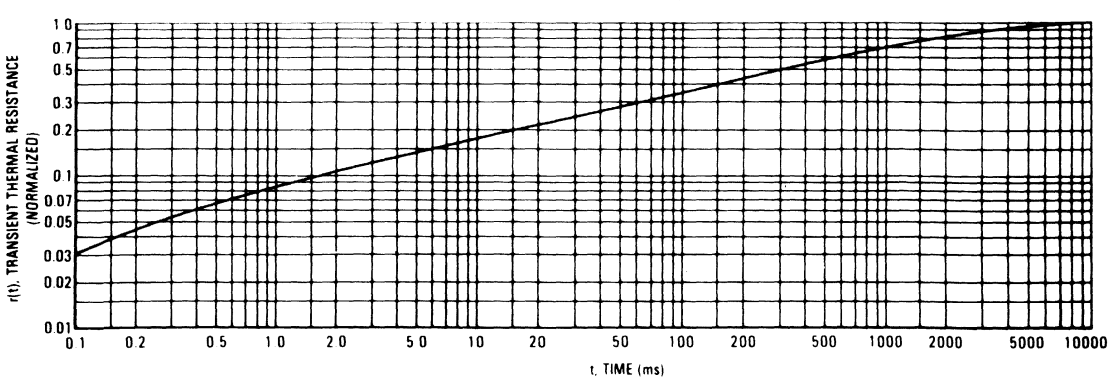


FIGURE 6 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE TRIGGER VOLTAGE

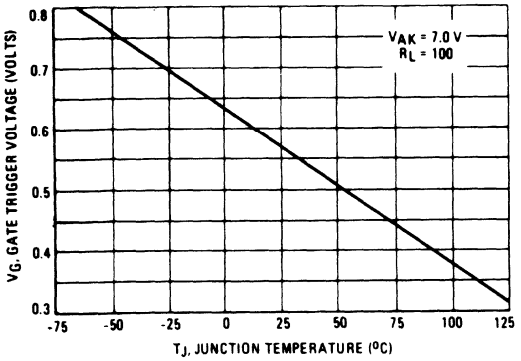


FIGURE 8 — TYPICAL GATE TRIGGER CURRENT

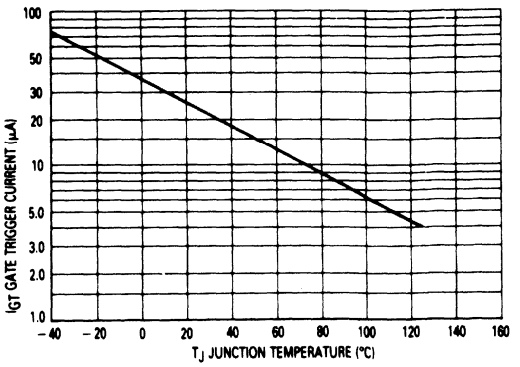


FIGURE 9 — HOLDING CURRENT

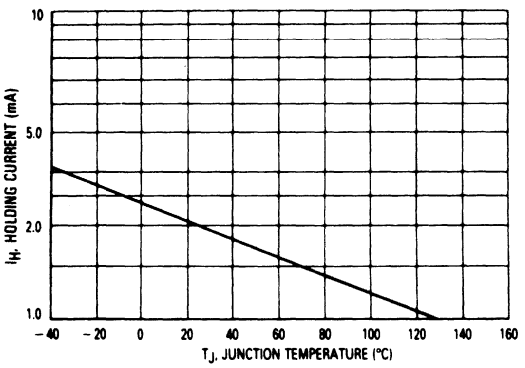
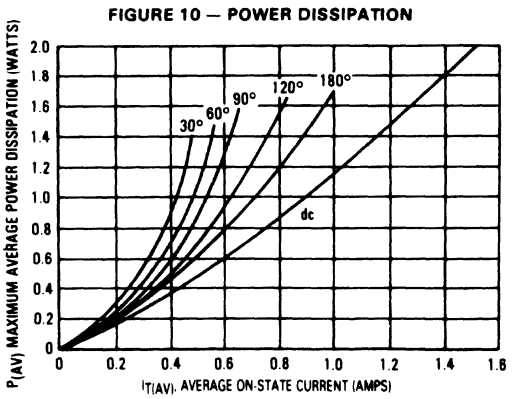


FIGURE 10 — POWER DISSIPATION



3

Silicon Controlled Rectifier

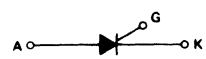
Reverse Blocking Triode Thyristor

MCR63-2 thru 10
MCR64-2 thru 10
MCR65-2 thru 10

SCRs
55 AMPERES RMS
50 thru 800 VOLTS

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light, and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 550 Amps
- Rugged Construction in Either Pressfit, Stud, or Isolated Stud
- Glass Passivated Junctions for Maximum Reliability



MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage, Note 1		V_{DRM} or V_{RRM}		Volts
	-2		50	
MCR63	-3		100	
MCR64	-4		200	
MCR65	-6		400	
	-8		600	
	-10		800	
Non-Repetitive Peak Reverse Blocking Voltage (t ≤ 5 ms)		V_{RSM}		Volts
	-2		75	
MCR63	-3		150	
MCR64	-4		300	
MCR65	-6		500	
	-8		700	
	-10		900	
Forward Current RMS		$I_{T(RMS)}$	55	Amps
Peak Surge Current (One cycle, 60 Hz, T_J = −40 to +125°C)		I_{TSM}	550	Amps
Circuit Fusing Considerations (T_J = −40 to +125°C, t = 1 to 8.3 ms)		I^2t	1255	A^2s
Peak Gate Power		P_{GFM}	20	Watts
Average Gate Power (Pulse Width ≤ 2 μs)		$P_{GF(AV)}$	0.5	Watt
Peak Forward Gate Current		I_{GFM}	2	Amps
Peak Gate Voltage — Forward		V_{GFM}	10	Volts
Reverse		V_{GRM}	10	
Operating Junction Temperature Range		T_J	−40 to +125	°C
Storage Temperature Range		T_{stg}	−40 to +150	°C
Stud Torque		—	30	in. lb.

Note 1. V_{RRM} for all types can be applied on a continuous dc basis without incurring damage Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

CASE 263-04
STYLE 1
MCR64 Series

CASE 310-02
STYLE 1
MCR63 Series

CASE 311-02
STYLE 1
MCR65 Series

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Pressfit and Stud		1	
Isolated Stud		1.1	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	10	μA
T_J = 125°C		—	2	mA
Forward "On" Voltage (I_{TM} = 175 A Peak)	V_{TM}	—	2	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 50 Ω) T_C = 25°C	I_{GT}	—	40	mA
T_C = −40°C		—	75	
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 50 Ω) T_C = 25°C	V_{GT}	—	3	Volts
T_C = −40°C		—	3.5	
(V_D = Rated V_{DRM}, R_L = 1 kΩ, T_J = 125°C)		0.2	—	
Holding Current (V_D = 12 V, R_L = 50 Ω, Gate Open)	I_H	—	60	mA
Forward Voltage Application Rate (T_J = 125°C, V_D = Rated V_{DRM})	dv/dt	50	—	V/μs

3

FIGURE 1 – AVERAGE CURRENT DERATING

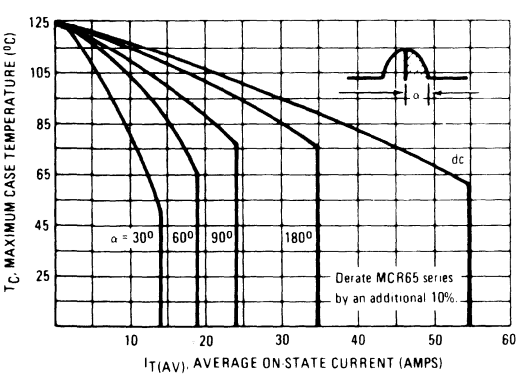
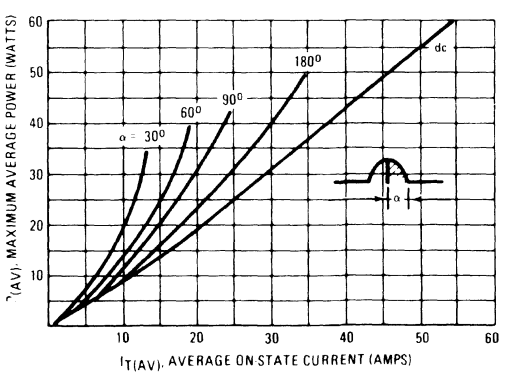


FIGURE 2 – POWER DISSIPATION



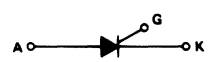
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristor

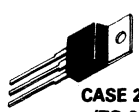
MCR67 Series
MCR68 Series
MCR69 Series

SCRs
12 and 25 AMPERES RMS
50 thru 400 VOLTS

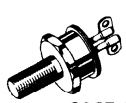
. . . designed for overvoltage protection in crowbar circuits.

- Glass-Passivated Junctions for Greater Parameter Stability and Reliability
- Center-Gate Geometry for Uniform Current Spreading Enabling High Discharge Current
- Small Rugged, Thermowatt or Metal Packages Constructed for Low Thermal Resistance for Maximum Power Dissipation and Durability
- High Capacitor Discharge Current
  300 Amps (MCR67, 68)
  750 Amps (MCR69)





CASE 221A-04
(TO-220AB)
STYLE 3
MCR68/MCR69 Series



CASE 86-01
STYLE 1
MCR67 Series

MAXIMUM RATINGS

Rating	Symbol	Value MCR67	Value MCR68	Value MCR69	Unit
Repetitive Peak Forward or Reverse Blocking Voltage, Note 1 (T_J = −40 to +125°C) MCR67, 68, 69 -2	V_{DRM} or V_{RRM}	50			Volts
-3		100			
-6		400			
Peak Discharge Current, Note 2	I_{TM}	300	300	750	Amps
On-State Current (T_C = 85°C) (1/2 Cycle, Sine Wave, 60 Hz)	$I_{T(RMS)}$	12	12	25	Amps
	$I_{T(AV)}$	8	8	16	
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	100	100	300	Amps
Circuit Fusing (t ≤ 8.3 ms)	I^2t	40	40	375	A^2s
Critical Rate-of-Rise of Current (Note 3)	di/dt	75		100	A/μs
Peak Gate Current (t ≤ 2 μs)	I_{GM}	2			Amps
Peak Gate Power (t ≤ 2 μs)	P_{GM}	20			Watts
Average Gate Power	$P_{G(AV)}$	0.5			Watt
Operating Junction Temperature Range	T_J	−40 to +125			°C
Storage Temperature Range	T_{stg}	−40 to +150			°C
Mounting Torque	—	15	8	8	in. lb.

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	2	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60			°C/W

Notes: 1. V_{DRM} for all types can be applied on a continuous basis over the operating junction temperature range without recurring damage. Ratings apply for open or shorted gate conditions or negative voltage on the gate. Devices should not be tested for blocking voltages such that the supply voltage exceeds the rating of the device.
2. Ratings apply for t_w = 1 ms. See Figure 1 for I_{TM} capability for various duration of an exponentially decaying current waveform, t_w is defined as 5 time constants of an exponentially decaying current pulse.
3. Test Conditions: I_G = 150 mA, V_D = Rated V_{DRM}, I_{TM} = Rated Value, T_J = 125°C.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C		I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C			—	—	2	mA
Forward On-State Voltage		V_{TM}				Volts
(I_{TM} = 24 Amps), Note 1	MCR67, 68		—	—	2.2	
(I_{TM} = 50 Amps), Note 1	MCR69		—	—	1.8	
(I_{TM} = 300 Amps, t_w = 1 ms), Note 2	MCR67, 68		—	6	—	
(I_{TM} = 750 Amps, t_w = 1 ms), Note 2	MCR69		—	6	—	
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω)		I_{GT}	2	7	30	mA
Gate Trigger Voltage (Continuous dc)		V_{GT}				volts
(V_D = 12 Volts, R_L = 100 Ω)			—	0.65	1.5	
(V_D = Rated V_{DRM}, R_L = 1 kΩ, T_J = 125°C)			0.2	0.40	—	
Holding Current (I_{TM} = 100 mA, Gate-Open)		I_H	3	15	50	mA
Latching Current (V_D = 12 Vdc, I_G = 150 mA, $t_r \leq$ 50 μs)		I_L	—	—	60	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Gate Open, Exponential Waveform, T_J = 125°C)		dv/dt	10	—	—	V/μs
Gate Controlled Turn-On Time, Note 3 (V_D = Rated V_{DRM}, I_G = 150 mA)		t_{gt}				μs
(I_{TM} = 24 Amps, peak)	MCR67, 68		—	1	—	
(I_{TM} = 50 Amps, peak)	MCR69		—	1	—	

Notes: 1. Pulse duration ≤ 300 μs, duty cycle ≤ 2%.
2. Ratings apply for t_w = 1 ms. See Figure 1 for I_{TM} capability for various durations of an exponentially decyaing current waveform. t_w is defined as 5 time constants of an exponentially decaying current pulse.
3. The gate controlled turn-on time in a crowbar circuit will be influenced by the circuit inductance.

3

FIGURE 1 – PEAK CAPACITOR DISCHARGE CURRENT

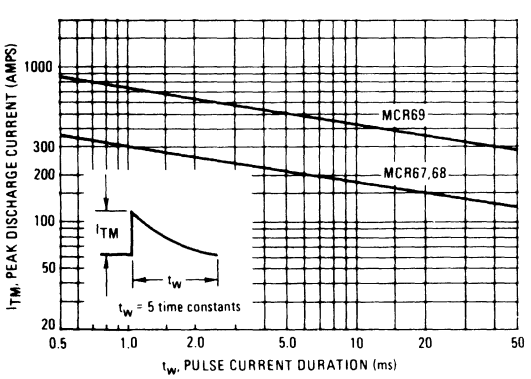


FIGURE 2 – PEAK CAPACITOR DISCHARGE CURRENT DERATING

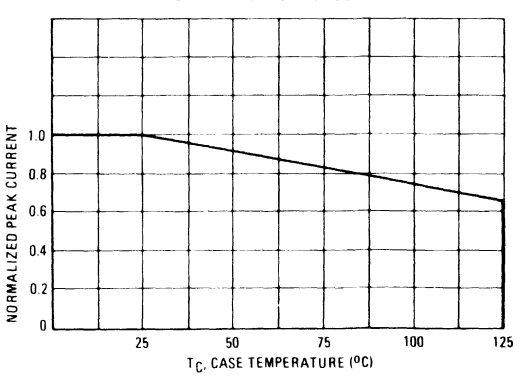


FIGURE 3 – CURRENT DERATING
MCR67,68

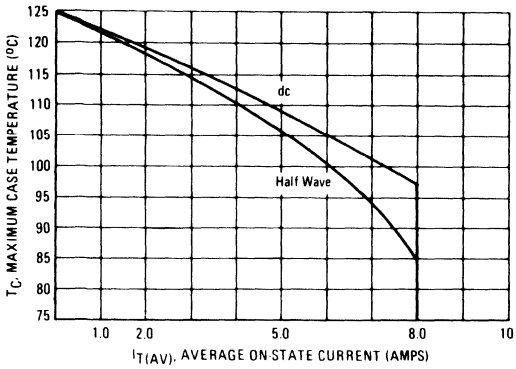


FIGURE 4 – CURRENT DERATING
MCR69

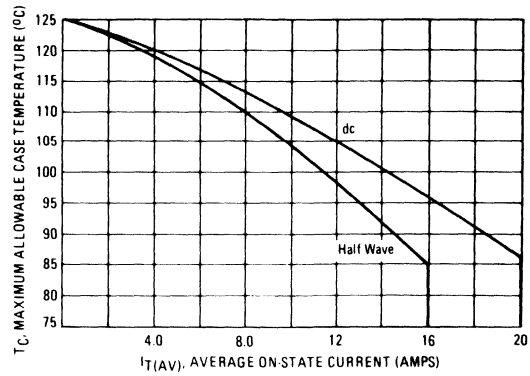


FIGURE 5 – MAXIMUM POWER DISSIPATION
MCR67,68

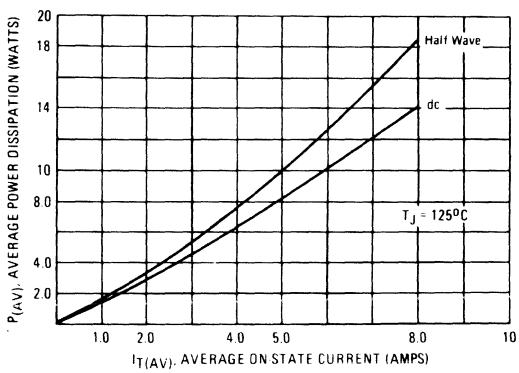


FIGURE 6 – MAXIMUM POWER DISSIPATION
MCR69

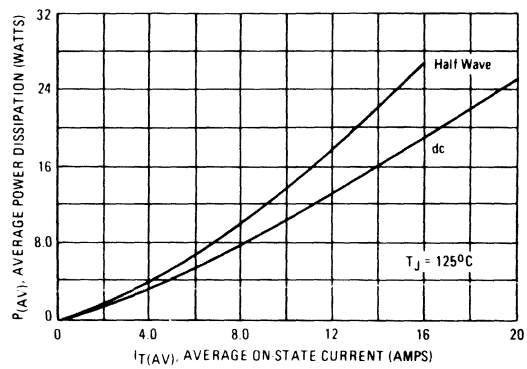


FIGURE 7 – THERMAL RESPONSE

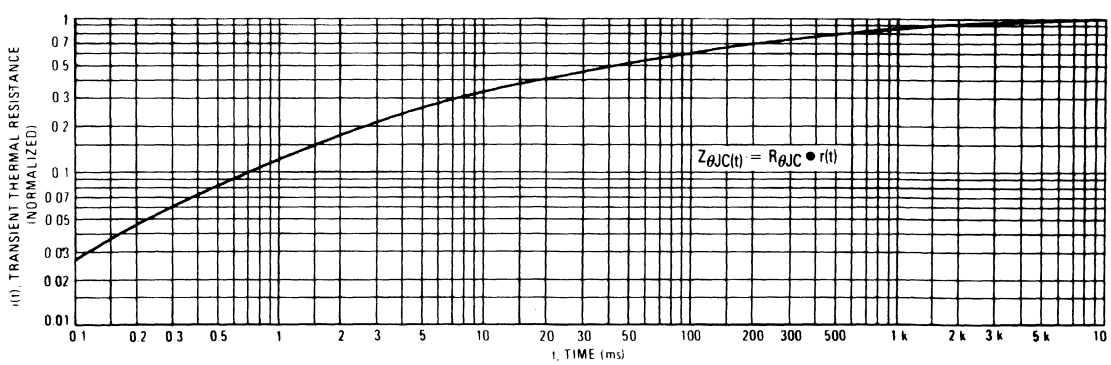


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FIGURE 8 – GATE TRIGGER CURRENT

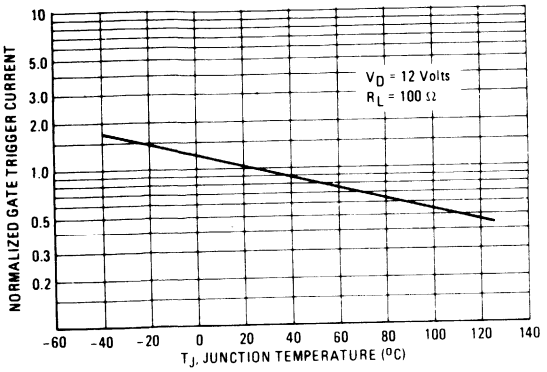


FIGURE 9 – GATE TRIGGER VOLTAGE

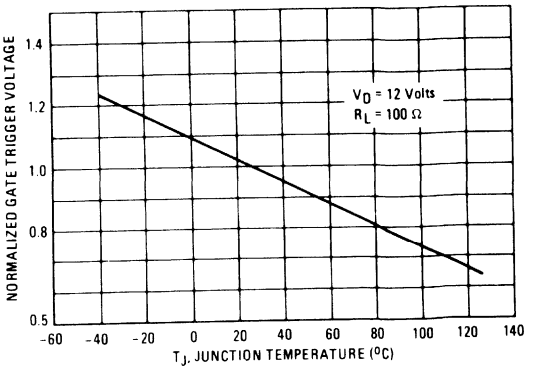
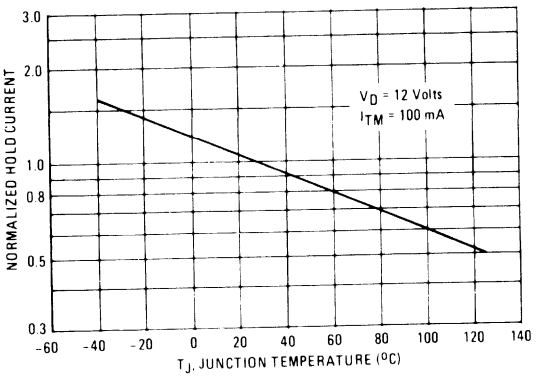


FIGURE 10 – HOLDING CURRENT



3

Silicon Controlled Rectifiers

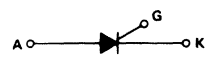
Reverse Blocking Triode Thyristor

MCR70 Series
MCR71 Series

SCRs
35 and 55 AMPERES RMS
50 thru 400 VOLTS

. . . designed for overvoltage protection in crowbar circuits.

- Glass-Passivated Junctions for Greater Parameter Uniformity and Stability
- Center-Gate Geometry for Uniform Current Spreading Enabling High Peak Current Capability
- High Capacitor Discharge Current Capability
  850 Amps (MCR70)
  1700 Amps (MCR71)
- Hermetically-Sealed Metal Packages



CASE 175-03
STYLE 1
MCR70 Series

CASE 263-04
STYLE 1
MCR71 Series

MAXIMUM RATINGS

Rating	Symbol	Value MCR70	Value MCR71	Unit
Repetitive Peak Forward or Reverse Blocking Voltage, Note 1 — MCR70, 71-2	V_{DRM} or V_{RRM}	50		Volts
MCR70, 71-3		100		
MCR70, 71-6		400		
Peak Discharge Current, Note 2	I_{TM}	850	1700	Amps
On-State Current ($T_C \leq 75°C$)	$I_{T(RMS)}$ $I_{T(AV)}$	35 22	55 35	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	350	550	Amps
Circuit Fusing ($t \leq 8.3$ ms)	I^2t	510	1255	A^2s
Critical Rate-of-Rise of Current, Note 3	di/dt	100	200	A/μS
Forward Peak Gate Power ($t \leq 20$ μs)	P_{GM}	20		Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5		Watts
Forward Peak Gate Current ($t \leq 20$ μs)	I_{GM}	2		Watt
Operating Junction Temperature Range	T_J	−40 to +125		°C
Storage Temperature Range	T_{stg}	−40 to +150		°C
Mounting Torque	—	30		in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W

Notes: 1. The rated voltage can be applied over the rated operating junction temperatures without incurring damage. Ratings apply for shorted-open or shorted-gate conditions or negative voltage on the gate. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltages.
2. Rating is for t_w = 1 ms. See Figure 1 for I_{TM} limits of an exponentially decaying current pulse of various durations.
3. Test Conditions: I_G = 150 mA, V_D = Rated V_{DRM}, I_{TM} = Rated Value, T_J = 125°C.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C		I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C			—	—	2	mA
On-State Voltage, Note 1		V_{TM}				Volts
(I_{TM} = 70 A)	MCR70 series		—	1.5	1.85	
(I_{TM} = 175 A)	MCR71 series		—	1.7	2.1	
(I_{TM} = 850 A, t_w = 1 ms) Note 2	MCR70 series		—	6	—	
(I_{TM} = 1700 A, t_w = 1 ms) Note 2	MCR71 series		—	7	—	
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω)		I_{GT}	2	10	30	mA
Gate Trigger Voltage (Continuous dc)		V_{GT}				volts
(V_D = 12 Volts, R_L = 100 Ω)			—	1	1.5	
(V_D = Rated V_{DRM}, R_L = 1 kΩ, T_J = 125°C)			0.2	—	—	
Holding Current (I_{TM} = 0.5 A, Gate-Open)		I_H	3	15	50	mA
Latching Current (V_D = 12 Vdc, I_G = 150 mA, t_r ≤ 50 μs)		I_L	—	30	60	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Gate Open, Exponential Waveform, T_C = 125°C)		dv/dt	10	—	—	V/μs
Turn-On Time, Note 3 (V_D = Rated V_{DRM}, I_G = 150 mA)		t_{on}				μs
(I_{TM} = 70 Amps, peak)	MCR70 series		—	1	—	
(I_{TM} = 110 Amps, peak)	MCR71 series		—	1.2	—	

Notes: 1. Duty Cycle ≤ 1%, Pulse Width ≤ 300 μs.
2. Characteristic applies for t_w = 1 ms. t_w is defined as 5 time constants of an exponentially decaying current pulse.
3. The gate controlled turn-on time in a crowbar circuit will be influenced by the circuit inductance.

3

FIGURE 1 – PEAK CAPACITOR DISCHARGE CURRENT

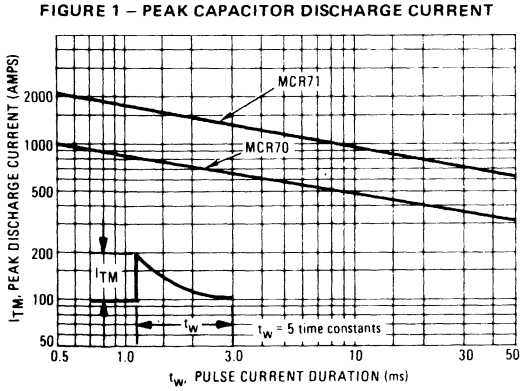


FIGURE 2 – PEAK CAPACITOR DISCHARGE CURRENT DERATING

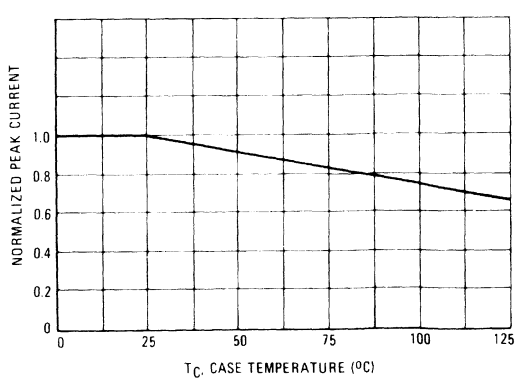


FIGURE 3 – AVERAGE CURRENT DERATING
MCR70

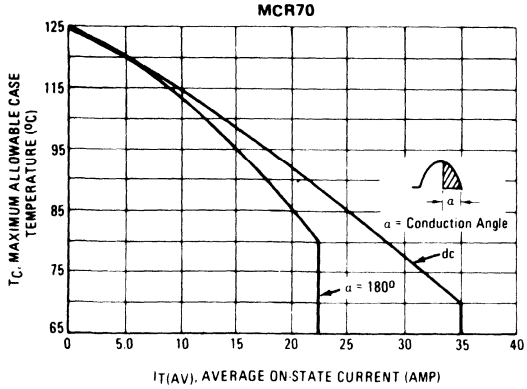


FIGURE 4 – POWER DISSIPATION
MCR70

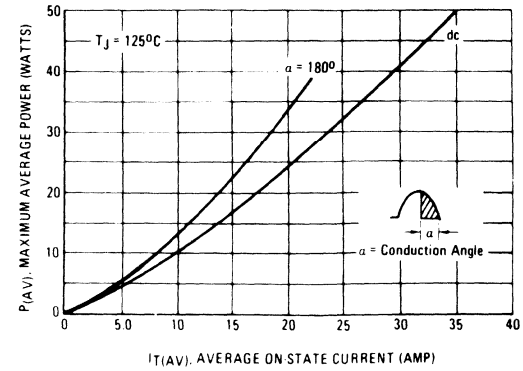


FIGURE 5 – CURRENT DERATING
MCR71

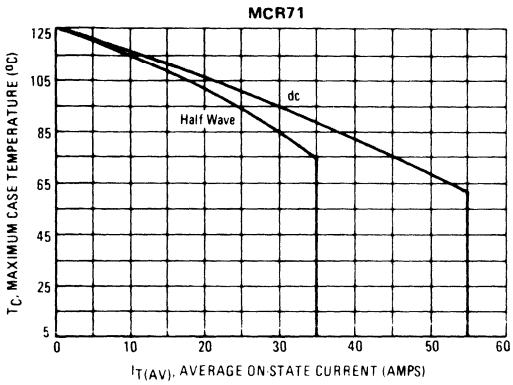


FIGURE 6 – POWER DISSIPATION
MCR71

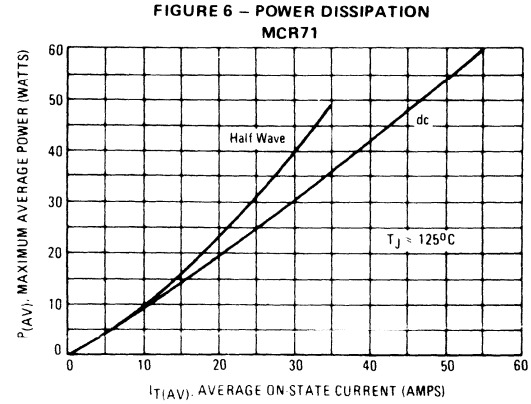


FIGURE 7 – TYPICAL THERMAL RESPONSE

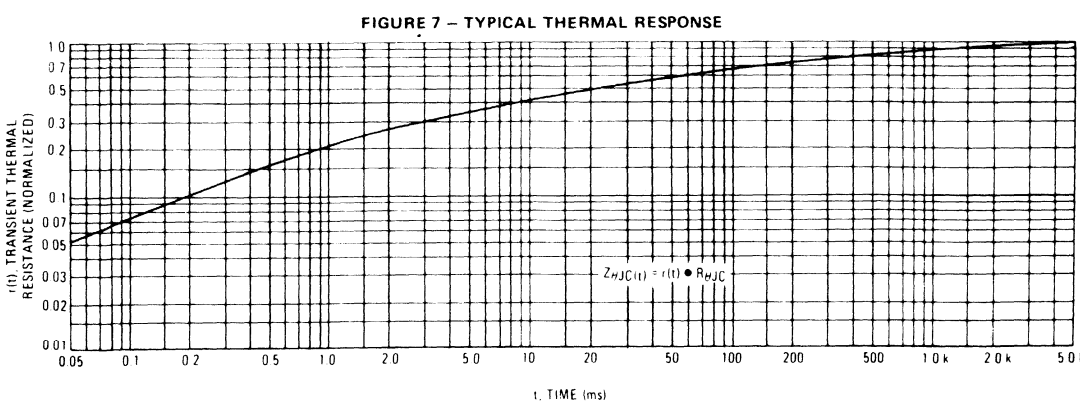


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FIGURE 8 – GATE TRIGGER CURRENT

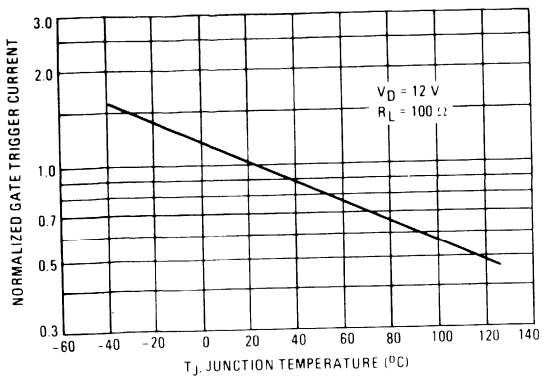


FIGURE 9 – GATE TRIGGER VOLTAGE

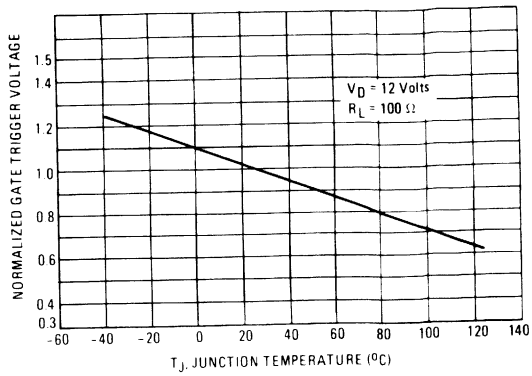
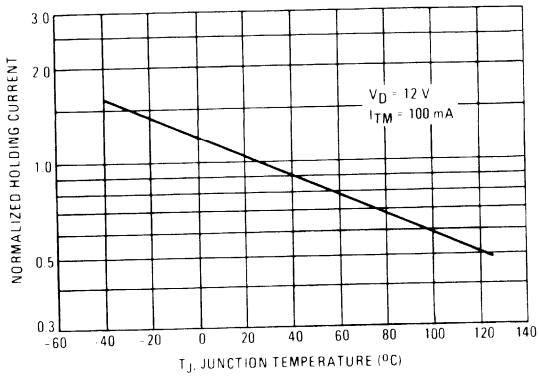


FIGURE 10 – HOLDING CURRENT



3

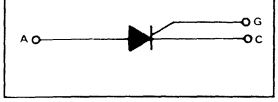
Silicon Controlled Rectifier
Reverse Blocking Triode Thyristor

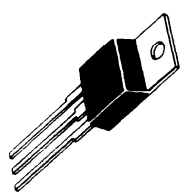
MCR72 Series

SCRs
8 AMPERES RMS
50 thru 600 VOLTS

. . . designed for industrial and consumer applications such as temperature, light and speed control; process and remote controls; warning systems; capacitive discharge circuits and MPU interface.

- Center Gate Geometry for Uniform Current Density
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Low Trigger Currents, 200 μA Maximum for Direct Driving from Integrated Circuits





CASE 221A-04
(TO-220AB)
STYLE 3

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage, Note 1 (T_J = −40 to 110°C) (1/2 Sine Wave, R_{GK} = 1 kΩ)	V_{DRM} or V_{RRM}		Volts
MCR72 -2		50	
MCR72 -3		100	
MCR72 -4		200	
MCR72 -6		400	
MCR72 -8		600	
On-State RMS Current (T_C = 83°C)	$I_{T(RMS)}$	8	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, 60 Hz, T_J = −40 to 110°C)	I_{TSM}	100	Amps
Circuit Fusing (t = 1 to 8.3 ms)	I^2t	40	A^2s
Peak Gate Voltage (t ≤ 10 μs)	V_{GM}	±5	Volts
Peak Gate Current (t ≤ 10 μs)	I_{GM}	1	Amp
Peak Gate Power (t ≤ 10 μs)	P_{GM}	5	Watts
Average Gate Power	$P_{G(AV)}$	0.75	Watts
Operating Junction Temperature Range	T_J	−40 to +110	°C

Note 1. Ratings apply for negative gate voltage or R_{GK} = 1 kΩ. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage. (cont.)

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque	—	8	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C, R_{GK} = 1 kΩ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current, Note 1 (Rated V_{DRM} or V_{RRM}) T_J = 25°C T_J = 110°C	I_{DRM}, I_{RRM}	 — —	 — —	 10 500	 μA μA
On-State Voltage (I_{TM} = 16 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.7	2	Volts
Gate Trigger Current (Continuous dc), Note 2 (V_D = 12 V, R_L = 100 Ω)	I_{GT}	—	30	200	μA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω) (V_D = Rated V_{DRM}, R_L = 10 kΩ, T_J = 110°C)	V_{GT}	 — 0.1	 0.5 —	 1.5 —	Volts
Holding Current (V_D = 12 V, I_{TM} = 100 mA)	I_H	—	—	6	mA
Critical Rate of Rise of Forward Blocking Voltage (V_D = Rated V_{DRM}, T_J = 110°C, Exponential Waveform)	dv/dt	—	10	—	V/μs
Gate Controlled Turn On Time (V_D = Rated V_{DRM}, I_{TM} = 16 A, I_G = 2 mA)	t_{gt}	—	1	—	μs

3

Notes: 1. Ratings apply for negative gate voltage or R_{GK} = 1 kΩ. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Does not include R_{GK} current.

FIGURE 1 – AVERAGE CURRENT DERATING

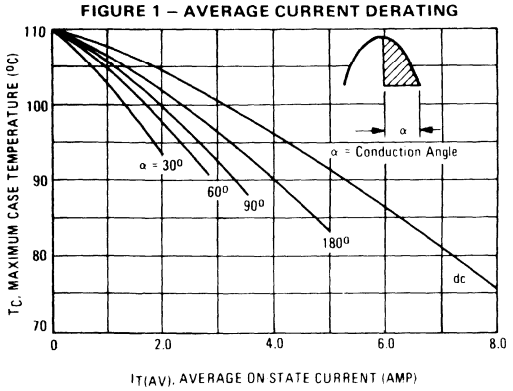


FIGURE 2 – ON-STATE POWER DISSIPATION

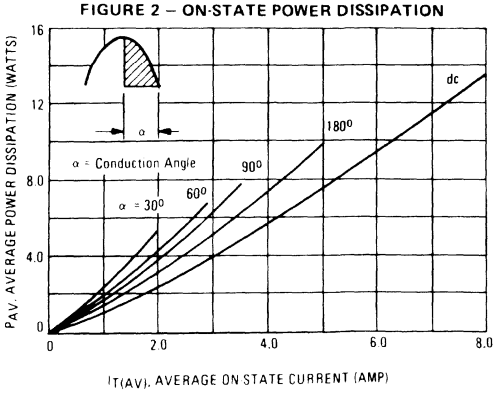


FIGURE 3 – NORMALIZED GATE CURRENT

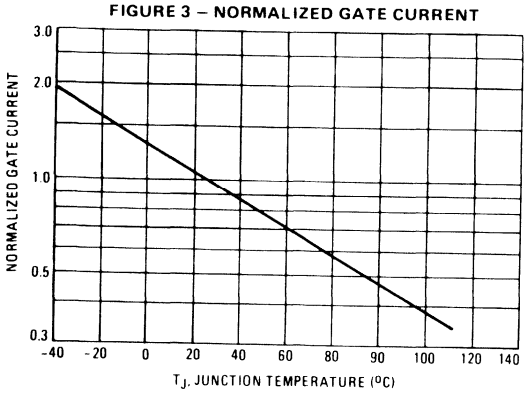
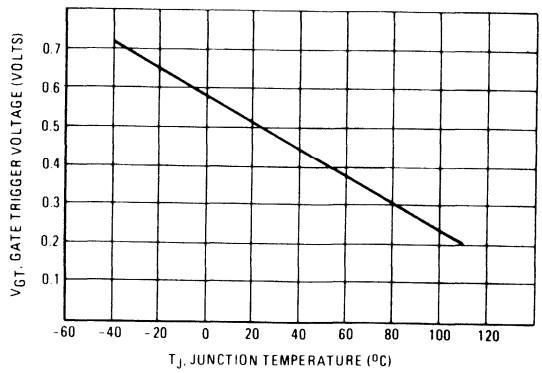


FIGURE 4 – GATE VOLTAGE



3

Plastic Silicon Controlled Rectifiers

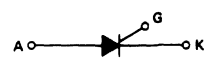
Reverse Blocking Triode Thyristors

MCR100 Series

SCRs
0.8 AMPERE RMS
100 thru 600 VOLTS

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-226AA package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current — 200 μA Maximum
- Low Reverse and Forward Blocking Current — 100 μA Maximum, T_C = 125°C
- Low Holding Current — 5 mA Maximum
- Glass-Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form



CASE 29-04
(TO-226AA)
STYLE 10

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage MCR100-3 MCR100-4 MCR100-6 MCR100-8	V_{RRM}	 100 200 400 600	Volts
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amps
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amps
Circuit Fusing Considerations, T_A = 25°C (t = 1 to 8.3 ms)	I^2t	0.415	A^2s
Peak Gate Power — Forward, T_A = 25°C	P_{GM}	0.1	Watts
Average Gate Power — Forward, T_A = 25°C	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current — Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1	Amp
Peak Gate Voltage — Reverse	V_{GRM}	5	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−65 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Lead Solder Temperature (< 1/16" from case, 10 s max)	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)	MCR100-3	V_{DRM}	100	—	Volts
	MCR100-4		200	—	
	MCR100-6		400	—	
	MCR100-8		600	—	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM})	T_C = 25°C	I_{DRM}, I_{RRM}	—	10	μA
	T_C = 125°C		—	100	μA
Forward "On" Voltage, Note 1 (I_{TM} = 1 A peak @ T_A = 25°C)		V_{TM}	—	1.7	Volts
Gate Trigger Current (Continuous dc), Note 2 (Anode Voltage = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	—	200	μA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C	V_{GT}	—	0.8	Volts
	T_C = −40°C		—	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C		0.1	—	
Holding Current (Anode Voltage = 7 Vdc, initiating current = 20 mA)	T_C = 25°C	I_H	—	5	mA
	T_C = −40°C		—	10	

Notes: 1. Forward current applied for 1 ms maximum duration, duty cycle ≤ 1%.
2. R_{GK} current is not included in measurement.

3

FIGURE 1 – MCR100-7, MCR100-8 CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

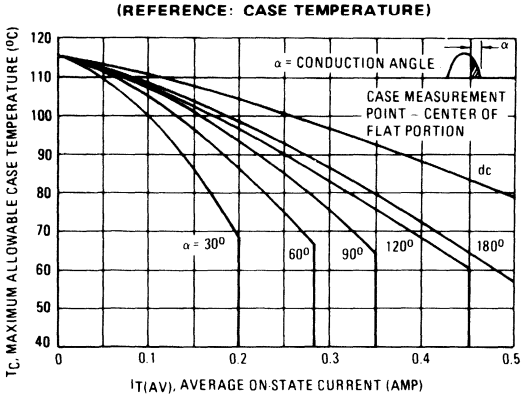
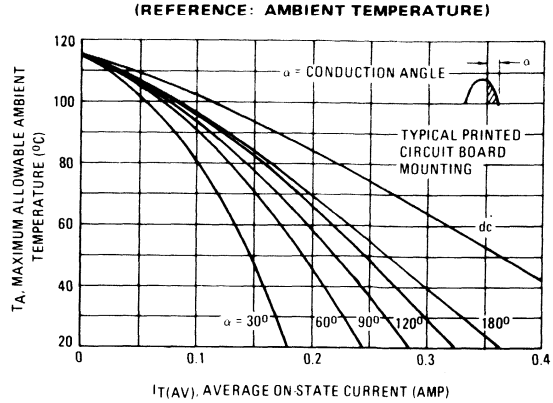


FIGURE 2 – MCR100-7, MCR100-8 CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)



Silicon Controlled Rectifiers

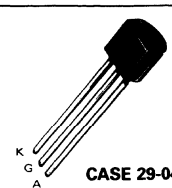
Reverse Blocking Triode Thyristor

MCR102
MCR103

SCRs
0.8 AMPERES RMS
30 and 60 VOLTS

Annular PNPN devices designed for low cost, high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-226AA package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current — 200 μA Maximum
- Low Reverse and Forward Blocking Current — 100 μA Maximum, T_C = 85°C
- Low Holding Current — 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form



CASE 29-04
(TO-226AA)
STYLE 10

3

MAXIMUM RATINGS, Note 1

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage, Note 2 (R_{GK} = 1000 ohms, T_C = +85°C) MCR102 / MCR103	V_{RRM}	30 / 60	Volts
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amps
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amps
Circuit Fusing Considerations, T_A = 25°C (t = 1 to 8.3 ms)	I^2t	0.415	A^2s
Peak Gate Power — Forward, T_A = 25°C	P_{GM}	0.1	Watt
Average Gate Power — Forward, T_A = 25°C	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current — Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1	Amp
Peak Gate Voltage — Reverse	V_{GRM}	4	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−40 to +85	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Lead Solder Temperature (< 1/16" from case, 10 s max)	—	+230	°C

Notes: 1. Temperature reference point for all case temperature is center of flat portion of package. (T_C = +85°C unless otherwise noted.)

2. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (T_C = 85°C)	MCR102 MCR103	V_{DRM}	30 60	— —	Volts
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM})	T_C = 25°C T_C = 85°C	I_{DRM}, I_{RRM}	— —	10 100	μA μA
Forward "On" Voltage, Note 1 (I_{TM} = 1 A peak @ T_A = 25°C)		V_{TM}	—	1.7	Volts
Gate Trigger Current (Continuous dc), Note 2 (Anode Voltage = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	—	200	μA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C T_C = −65°C T_C = 85°C	V_{GT} V_{GD}	— — 0.1	0.8 1.2 —	Volts
Holding Current (Anode Voltage = 7 Vdc, initiating current = 20 mA)	T_C = 25°C T_C = −65°C	I_H	— —	5 10	mA

Notes: 1. Forward current applied for 1 ms maximum duration, duty cycle ≤ 1%.
2. R_{GK} current is not included in measurement.

3

FIGURE 1 – CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

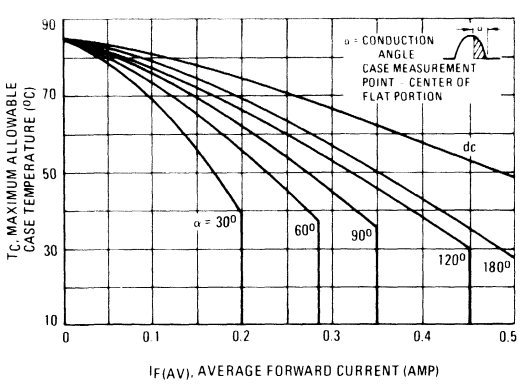
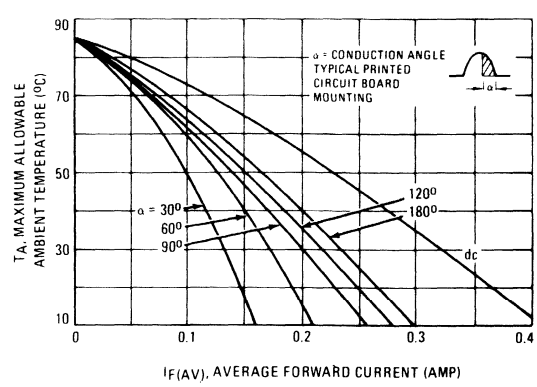


FIGURE 2 – CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)



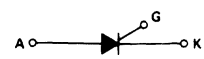
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristors

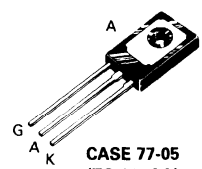
MCR106 Series

SCRs
4 AMPERES RMS
60 thru 600 VOLTS

PNPN devides designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Glass-Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability





CASE 77-05
(TO-225AA)
STYLE 2

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage, Note 1 MCR106-2 -3 -4 -6 -8	V_{RRM}	 60 100 200 400 600	Volts
RMS Foward Current (All Conduction Angles)	$I_{T(RMS)}$	4	Amps
Average Forward Current T_C = 93°C or T_A = 30°C	$I_{T(AV)}$	2.55	Amps
Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz, T_J = −40 to +110°C)	I_{TSM}	25	Amps
Circuit Fusing Considerations (T_J = −40 to +110°C, t = 1 to 8.3 ms)	I^2t	2.6	A^2s
Peak Gate Power	P_{GM}	0.5	Watt
Average Gate Power	$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current	I_{GM}	0.2	Amp
Peak Reverse Gate Voltage	V_{RGM}	6	Volts
Operating Junction Temperature Range	T_J	−40 to +110	°C

Note 1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage. (cont.)

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Storage Temperature Range	T_{stg}	−40 to +150	°C
Mounting Torque, Note 1	—	6	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C and R_{GK} = 1000 ohms unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 110°C, Note 1) MCR106-2	V_{DRM}	60	—	—	Volts
-3		100	—	—	
-4		200	—	—	
-6		400	—	—	
-8		600	—	—	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 110°C		—	—	200	μA
Forward "On" Voltage (I_{TM} = 4 A Peak)	V_{TM}	—	—	2	Volts
Gate Trigger Current (Continuous dc), Note 2 (V_{AK} = 7 Vdc, R_L = 100 ohms)	I_{GT}	—	—	200	μA
(V_{AK} = 7 Vdc, R_L = 100 ohms, T_C = −40°C)		—	—	500	
Gate Trigger Voltage (Continuous dc) (V_{AK} = 7 Vdc, R_L = 100 ohms, T_C = 25°C)	V_{GT}	—	—	1	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 ohms, T_J = 110°C)	V_{GD}	0.2	—	—	Volts
Holding Current (V_{AK} = 7 Vdc, T_C = 25°C)	I_H	—	—	5	mA
Forward Voltage Application Rate (T_J = 110°C)	dv/dt	—	10	—	V/μs

Notes: 1. Torque rating applies with use of compression washer (B52200-F006 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN209B).

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C. For optimum results, an activated flux (oxide removing) is recommended.

2. R_{GK} current is not included in measurement.

3

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

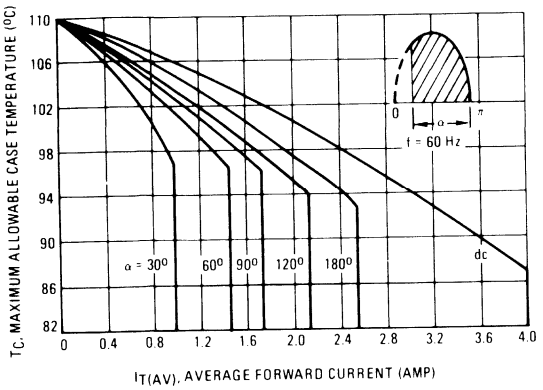
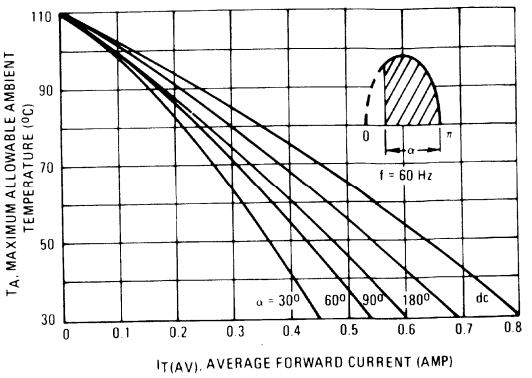


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE



3

Silicon Controlled Rectifiers

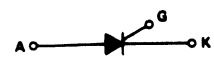
Reverse Blocking Triode Thyristors

MCR202 thru MCR206

SCRs
0.5 AMPERES RMS
30 thru 200 VOLTS

Annular PNPN devices designed for industrial/military applications such as relay and lamp drivers, small motor controllers and drivers for larger thyristors, and in sensing and detection circuits.

- Sensitive Gate Trigger Current — 200 μA Maximum
- Low Reverse and Forward Blocking Current — 100 μA Maximum, T_C = 125°C
- Low Holding Current — 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- TO-18 Hermetically Sealed Metal Package



CASE 22-03
(TO-206AA)
STYLE 6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Off-State and Reverse Voltage MCR202 MCR203 MCR204 MCR206	V_{DRM} V_{RRM}	 30 60 100 200	Volts
RMS On-State Current (All Conduction Angles) (See Figures 4 & 5)	$I_{T(RMS)}$	0.5	Amps
Peak Non-Repetitive Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6	Amps
Circuit Fusing Considerations (t = 1 to 8.3 ms)	I^2t	0.15	A^2s
Peak Forward Gate Power	P_{GM}	0.1	Watt
Average Forward Gate Power	$P_{GF(AV)}$	0.01	Watt
Peak Forward Gate Current (300 μs, 120 PPS)	I_{GFM}	1	Amp
Peak Reverse Gate Voltage	V_{GRM}	4	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	150	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	400	°C/W

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM})	T_C = 25°C T_C = 125°C	I_{DRM}, I_{RRM}	— —	10 100	μA μA
Peak On-State Voltage (I_{TM} = 1.2 A peak, ImS, Duty Cycle ≤ 1%)		V_{TM}	—	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 1) (Anode Voltage = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C T_C = −65°C	I_{GT}	— —	200 350	μA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C T_C = −65°C T_C = 125°C	V_{GT}	— — 0.1	0.8 1.2 —	Volts
Holding Current (Anode Voltage = 7 Vdc, initiating current = 20 mA)	T_C = 25°C T_C = −65°C	I_H	— —	5 10	mA

Note: 1. R_{GK} current is not included in measurement.

FIGURE 1 – CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

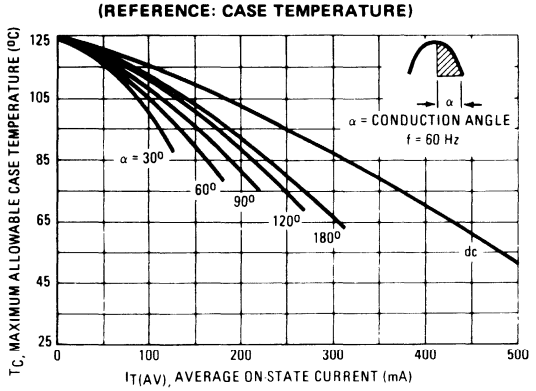


FIGURE 2 – POWER DISSIPATION

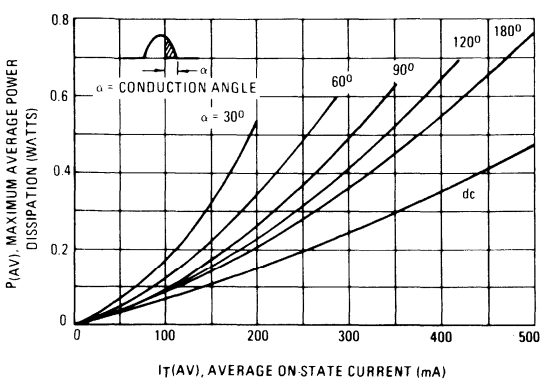


FIGURE 3 – FORWARD VOLTAGE

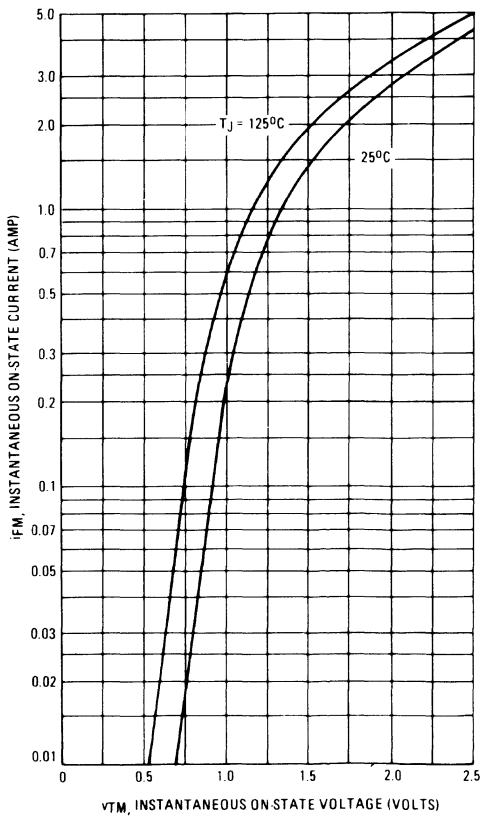


FIGURE 4 – SURGE RATINGS

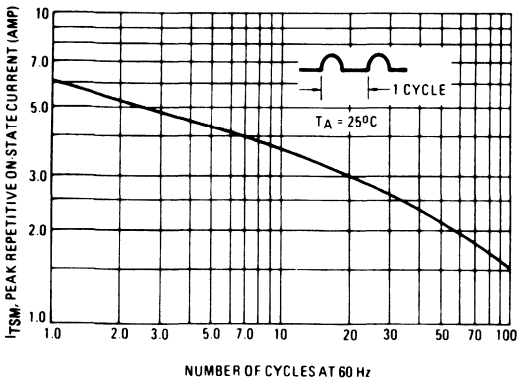


FIGURE 5 – CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)

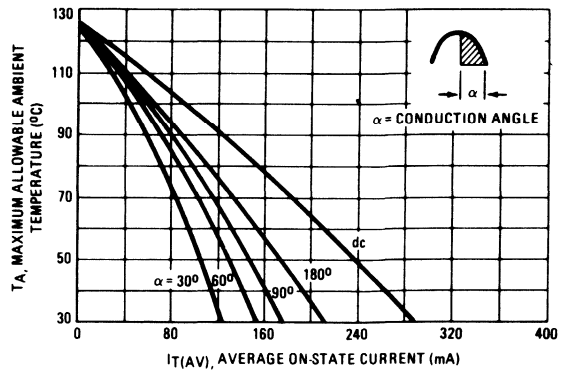
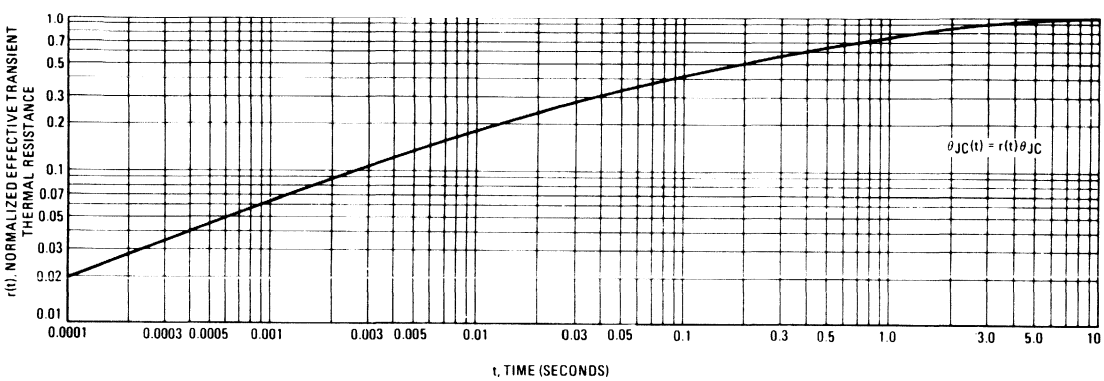


FIGURE 6 – THERMAL RESPONSE



3

TYPICAL CHARACTERISTICS

FIGURE 7 – GATE TRIGGER VOLTAGE

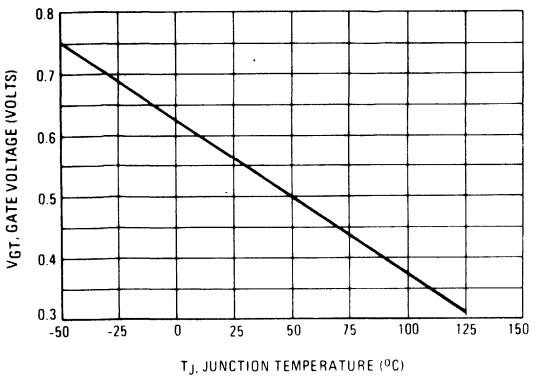


FIGURE 8 – GATE TRIGGER CURRENT

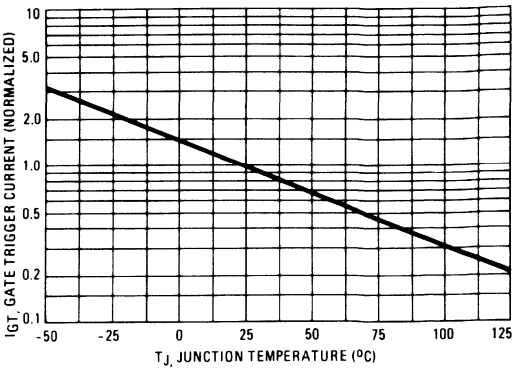
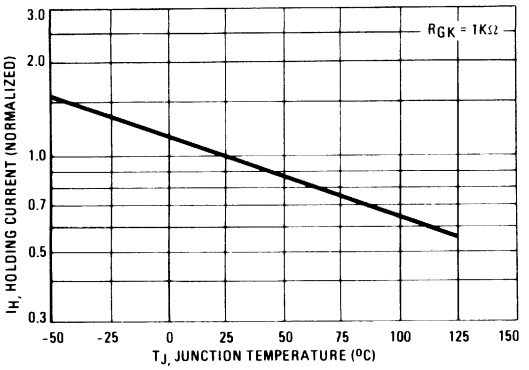


FIGURE 9 – HOLDING CURRENT



3

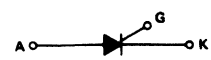
Thyristors
Silicon-Controlled Rectifiers

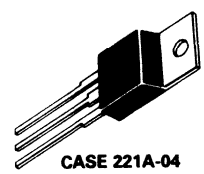
MCR218 Series

SCRs
8 AMPERES RMS
50 thru 800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass-Passivated Junctions
- Blocking Voltage to 800 Volts
- TO-220 Construction — Low Thermal Resistance, High Heat Dissipation and Durability





CASE 221A-04
(TO-220AB)
STYLE 3

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 Repetitive Peak Reverse Voltage	MCR218-2 -3 -4 -6 -8 -10	V_{RRM} V_{DRM}	 50 100 200 400 600 800	Volts
Forward Current RMS (All Conduction Angles)		$I_{T(RMS)}$	8	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)		I_{TSM}	80	Amps
Circuit Fusing Considerations (t = 8.3 ms)		I^2t	34	A^2s
Forward Peak Gate Power		P_{GM}	5	Watts
Forward Average Gate Power		$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current		I_{GM}	2	Amps
Operating Junction Temperature Range		T_J	−40 to +125	°C
Storage Temperature Range		T_{stg}	−40 to +150	°C

Note 1. V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	— —	— —	10 2	μA mA
Peak On-State Voltage, Note 1 (I_{TM} = 16 A Peak)	V_{TM}	—	1.5	1.8	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ohms)	I_{GT}	—	10	25	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ohms) (Rated V_{DRM}, R_L = 1000 Ohms, T_J = 125°C)	V_{GT}	— 0.2	— —	2.5 —	Volts
Holding Current (Anode Voltage = 24 Vdc, Peak Initiating On-State Current = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7 V, 20 Ohms)	I_H	—	16	30	mA
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)	dv/dt	—	100	—	V/μs

Note 1. Pulse Test: Pulse Width = 1 ms, Duty Cycle ≤ 2%.

3

FIGURE 2 — ON-STATE POWER DISSIPATION

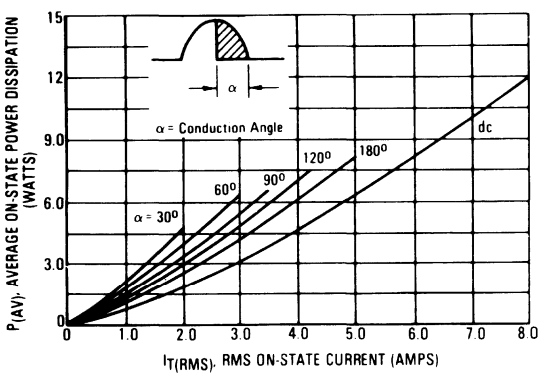


FIGURE 3 — NORMALIZED GATE TRIGGER CURRENT

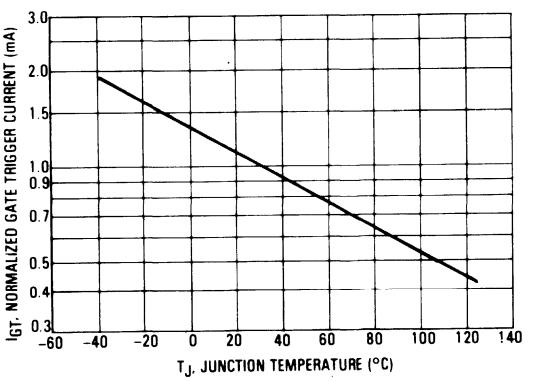


FIGURE 4 — NORMALIZED GATE TRIGGER VOLTAGE

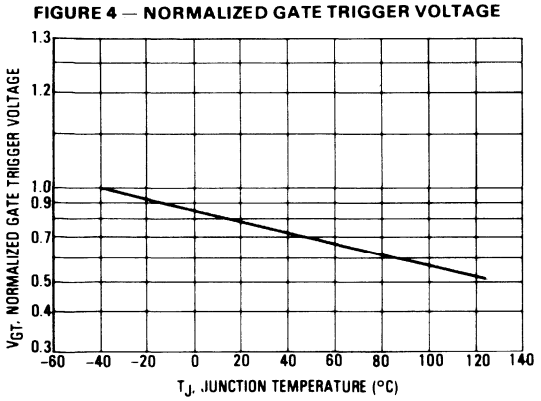
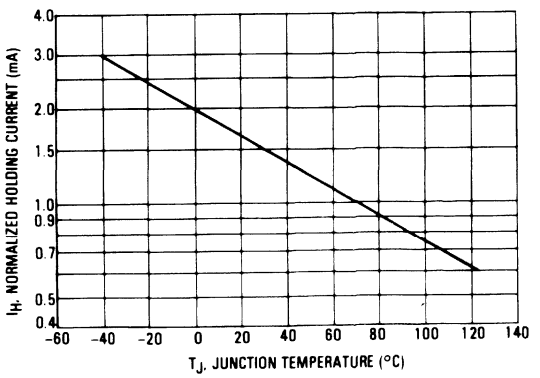


FIGURE 5 — NORMALIZED HOLDING CURRENT



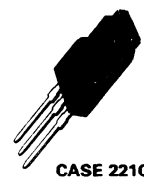
Silicon Controlled Rectifiers
Reverse Blocking Thyristors

MCR218FP Series

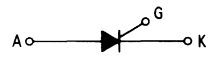
ISOLATED SCRs
8 AMPERES RMS
800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supply crowbar circuits.

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts
- 80 A Surge Current Capability
- Insulated Package Simplifies Mounting



CASE 221C-02
STYLE 2



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) Repetitive Peak Reverse Voltage MCR218-2FP MCR218-4FP MCR218-6FP MCR218-8FP MCR218-10FP	V_{DRM} V_{RRM}	 50 200 400 600 800	Volts
On-State RMS Current (T_C = +70°C) Full Cycle Sine Wave 50 to 60 Hz, Note 2	$I_{T(RMS)}$	8	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_C = +70°C) Preceded and followed by rated current	I_{TSM}	80	Amps
Circuit Fusing (T_C = +70°C, t = 1 to 8.3 ms)	I^2t	26	A^2s
Peak Gate Power (T_C = +70°C, Pulse Width = 10 μs)	P_{GM}	5	Watts
Average Gate Power (T_C = +70°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current (T_C = +70°C, Pulse Width = 10 μs)	I_{GM}	2	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W
Thermal Resistance, Case to Sink	$R_{\theta CS}$	2.2 (typ)	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current T_J = 25°C (Rated V_{DRM} @ T_J = 125°C)	I_{DRM}	— —	— —	10 2	μA mA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)	I_{RRM}	—	—	2	mA
Forward "On" Voltage, Note 1 (I_{TM} = 16 A Peak)	V_{TM}	—	1	1.8	Volts
Gate Trigger Current (Continuous dc) T_C = 25°C (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	I_{GT}	—	10	25	mA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	V_{GT}	—	—	2.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GD}	0.2	—	—	Volts
Holding Current (Anode Voltage = 12 Vdc)	I_H	—	16	30	mA
Turn-On Time (I_{TM} = 8 A, I_{GT} = 40 mAdc)	t_{gt}	—	1.5	—	μs
Turn-Off Time (V_{DRM} = Rated Voltage) (I_{TM} = 8 A, I_R = 8 A) (I_{TM} = 8 A, I_R = 8 A, T_J = 125°C)	t_q	 — —	 15 35	 — —	μs
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)	dv/dt	—	100	—	V/μs

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL CHARACTERISTICS

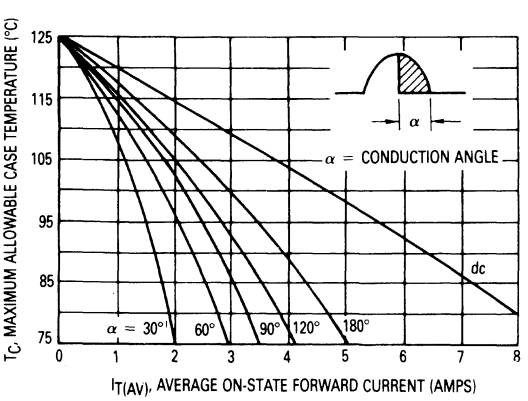


Figure 1. Current Derating

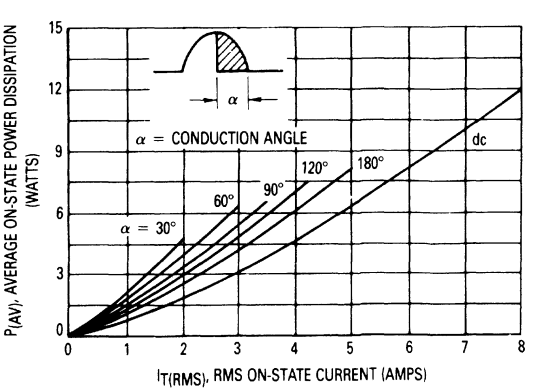


Figure 2. On-State Power Dissipation

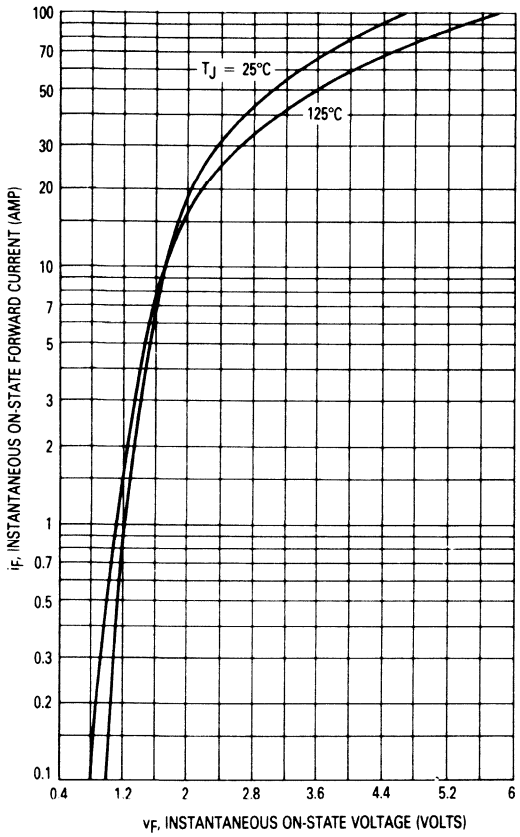


Figure 3. On-State Characteristics

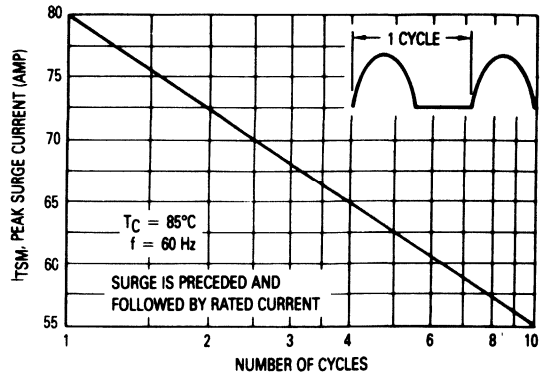


Figure 4. Maximum Non-Repetitive Surge Current

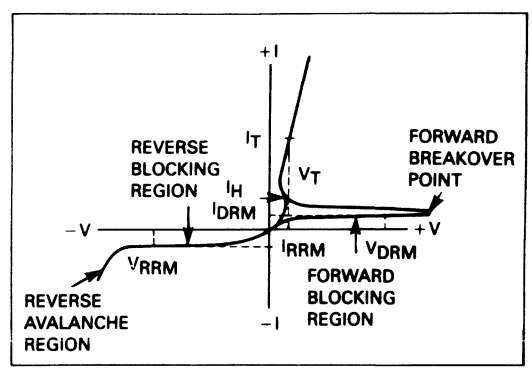


Figure 5. Characteristics and Symbols

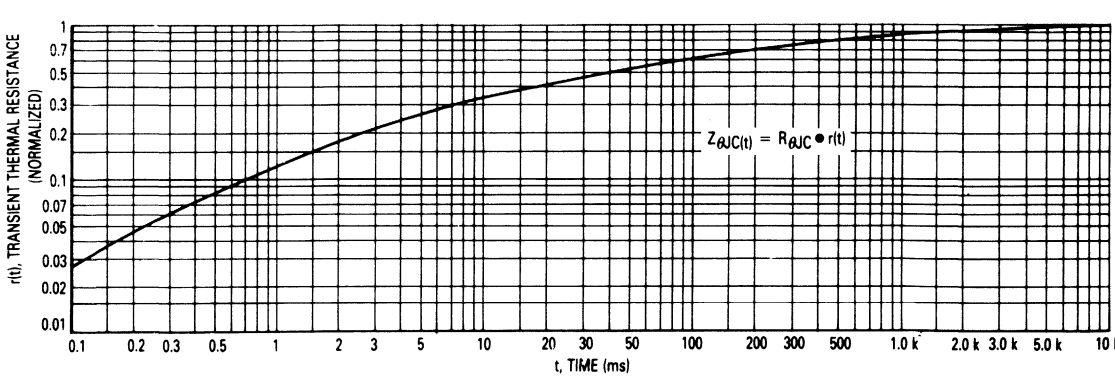


Figure 6. Thermal Response

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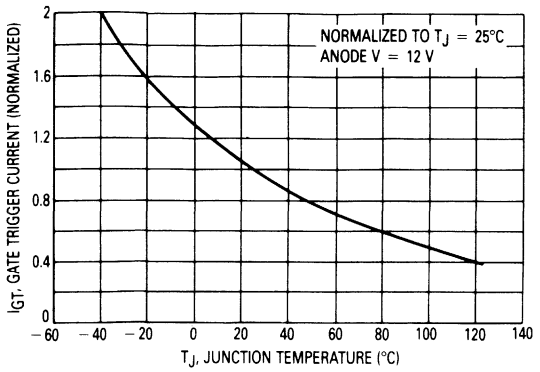


Figure 7. Gate Trigger Current versus Temperature

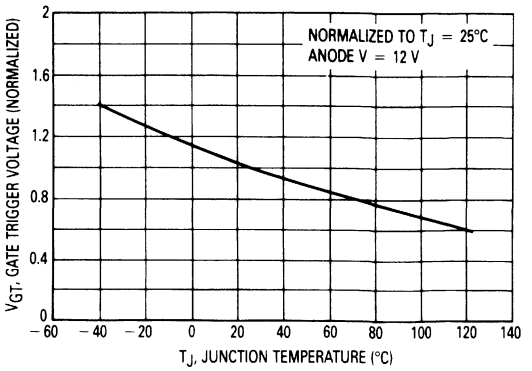


Figure 8. Gate Trigger Voltage versus Temperature

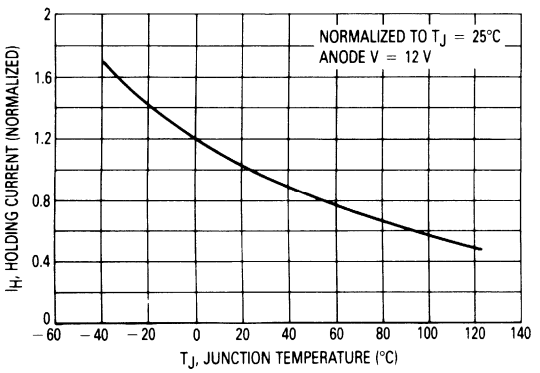


Figure 9. Holding Current versus Temperature

3

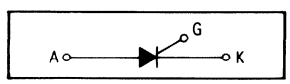
Silicon Controlled Rectifiers
Reverse Blocking Thyristors

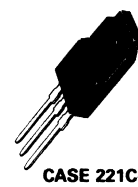
MCR225FP Series

ISOLATED SCRs
25 AMPERES RMS
800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supply crowbar circuits.

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts
- 300 A Surge Current Capability
- Insulated Package Simplifies Mounting





CASE 221C-02
STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +125°C) Repetitive Peak Reverse Voltage MCR225-2FP MCR225-4FP MCR225-6FP MCR225-8FP MCR225-10FP	V_{DRM} V_{RRM}	 50 200 400 600 800	Volts
On-State RMS Current (T_C = +70°C) Full Cycle Sine Wave 50 to 60 Hz, Note 2	$I_{T(RMS)}$	25	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_C = +70°C) Preceded and followed by rated current	I_{TSM}	300	Amps
Circuit Fusing (T_C = +70°C, t = 1 to 8.3 ms)	I^2t	373	A^2s
Peak Gate Power (T_C = +70°C, Pulse Width = 10 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +70°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current (T_C = +70°C, Pulse Width = 10 μs)	I_{GM}	2	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Case to Sink	$R_{\theta CS}$	2.2 (typ)	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current T_J = 25°C (Rated V_{DRM} @ T_J = 125°C)	I_{DRM}	— —	— —	10 2	μA mA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)	I_{RRM}	—	—	2	mA
Forward "On" Voltage, Note 1 (I_{TM} = 50 A)	V_{TM}	—	—	1.8	Volts
Gate Trigger Current (Continuous dc) T_C = 25°C (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	I_{GT}	—	—	40	mA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	V_{GT}	—	0.8	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GD}	0.2	—	—	Volts
Holding Current (Anode Voltage = 12 Vdc)	I_H	—	20	40	mA
Turn-On Time (I_{TM} = 25 A, I_{GT} = 40 mAdc)	t_{gt}	—	1.5	—	μs
Turn-Off Time (V_{DRM} = Rated Voltage) (I_{TM} = 25 A, I_R = 25 A) (I_{TM} = 25 A, I_R = 25 A, T_J = 125°C)	t_q	 — —	 15 35	 — —	μs
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)	dv/dt	—	100	—	V/μs

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL CHARACTERISTICS

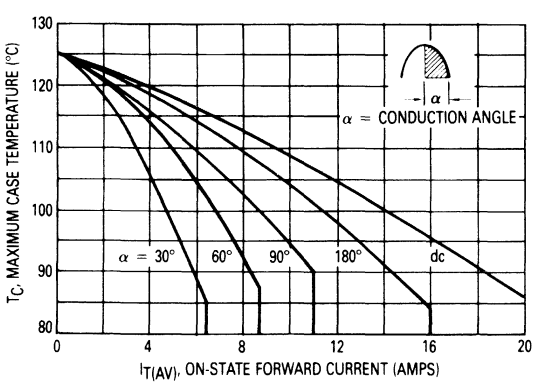


Figure 1. Average Current Derating

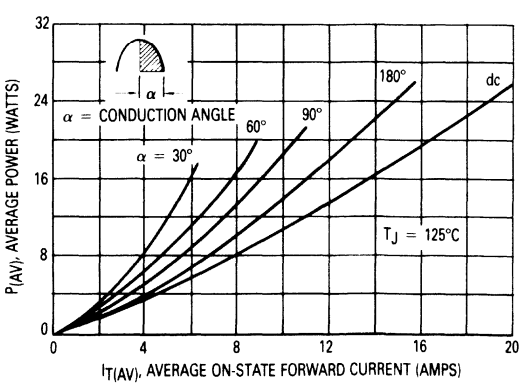


Figure 2. Maximum On-State Power Dissipation

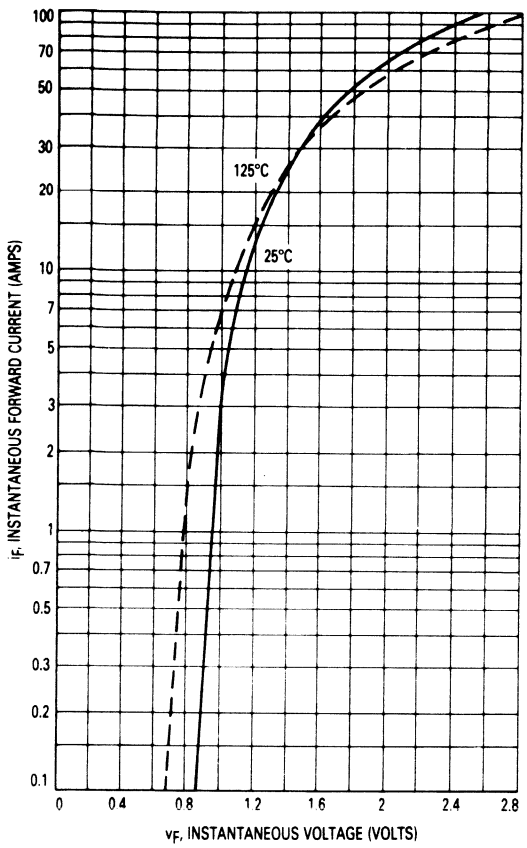


Figure 3. Maximum Forward Voltage

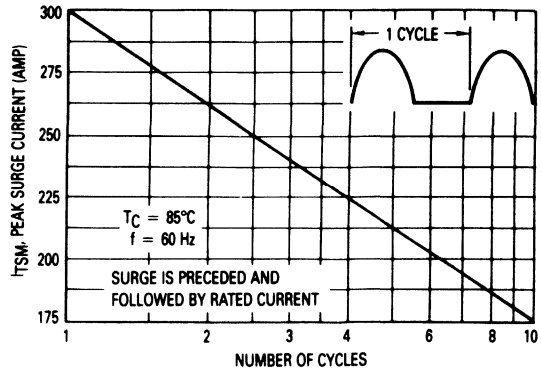


Figure 4. Maximum Non-Repetitive Surge Current

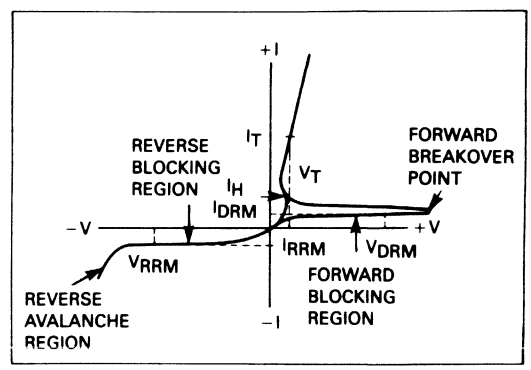


Figure 5. Characteristics and Symbols

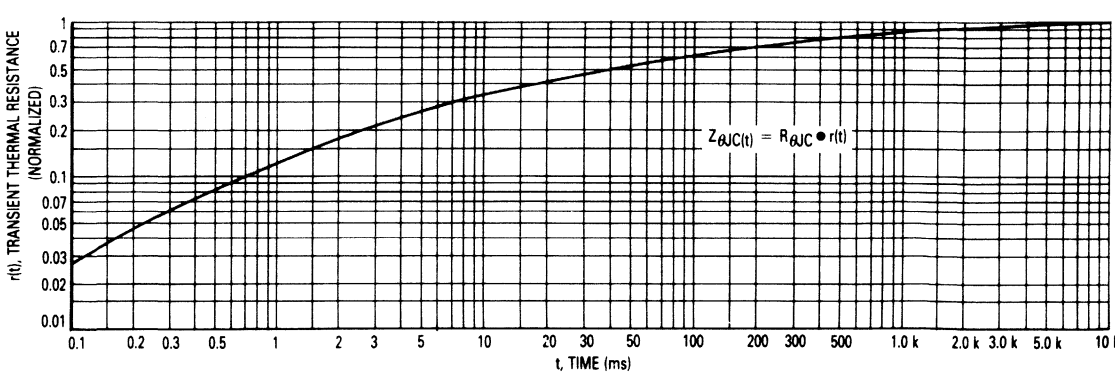


Figure 6. Thermal Response

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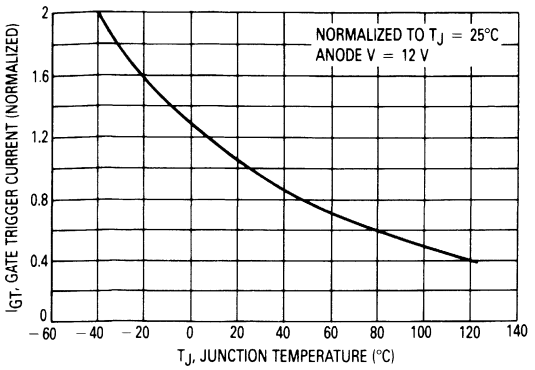


Figure 7. Gate Trigger Current versus Temperature

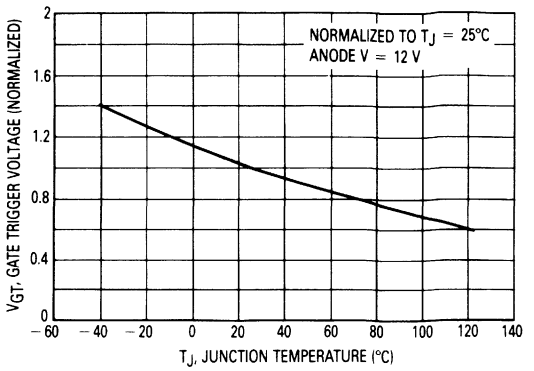


Figure 8. Gate Trigger Voltage versus Temperature

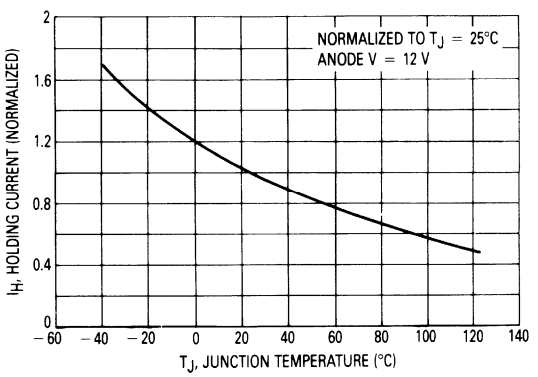


Figure 9. Holding Current versus Temperature

3

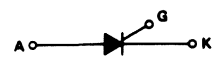
Thyristors
Silicon Controlled Rectifiers

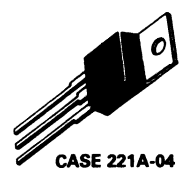
MCR264-2 thru MCR264-12

SCRs
40 AMPERES RMS
200 thru 1000 VOLTS

. . . designed for back-to-back SCR output devices for solid state relays or applications requiring high surge operation.

- Photo Glass Passivated Blocking Junctions for High Temperature Stability, Center Gate for Uniform Parameters
- 400 Amperes Surge Capability
- Blocking Voltage to 1000 Volts





CASE 221A-04
(TO-220AB)
STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage, Note 1	V_{RRM}		Volts
MCR264-2		50	
MCR264-3		100	
MCR264-4		200	
MCR264-6		400	
MCR264-8		600	
MCR264-10		800	
MCR264-12		1000	
Forward Current (T_C = 80°C) (All Conduction Angles)	$I_{T(RMS)}$ $I_{T(AV)}$	40* 25*	Amps
Peak Nonrepetitive Surge Current — 8.3 ms (1/2 Cycle, Sine Wave) 1.5 ms	I_{TSM}	400 450	Amps
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current (300 μs, 120 PPS)	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Note 1. V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

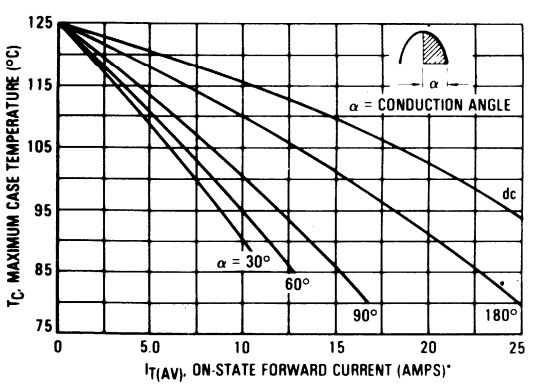
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 125°C)	V_{DRM}				Volts
MCR264-2		50	—	—	
MCR264-3		100	—	—	
MCR264-4		200	—	—	
MCR264-6		400	—	—	
MCR264-8		600	—	—	
MCR264-10		800	—	—	
MCR264-12		1000	—	—	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
Forward "On" Voltage, Note 1 (I_{TM} = 80 A)	V_{TM}	—	1.6	2	Volts
Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms, T_C = −40°C)	I_{GT}	—	15	50	mA
		—	30	90	
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	V_{GT}	—	1	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GD}	0.2	—	—	Volts
Holding Current (Anode Voltage = 12 Vdc)	I_H	—	30	60	mA
Turn-On Time (I_{TM} = 40 A, I_{GT} = 60 mAdc)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)	dv/dt	—	50	—	V/μs

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 1 — AVERAGE CURRENT DERATING



*This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents.

FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION

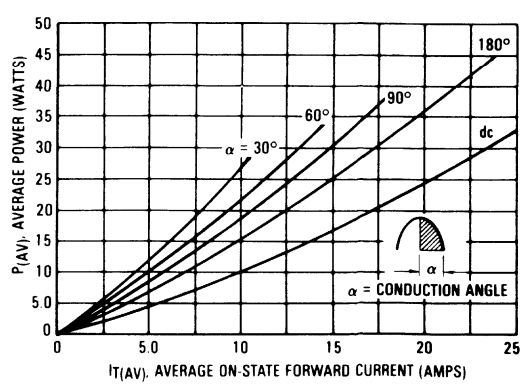


FIGURE 3 — GATE TRIGGER CURRENT

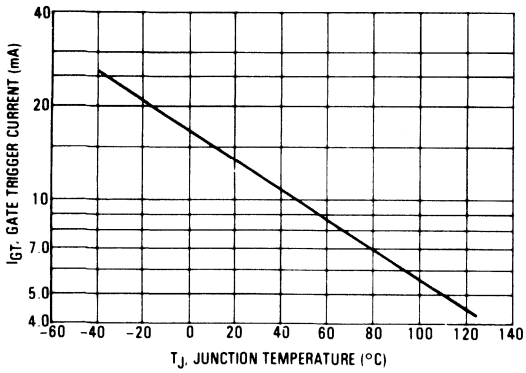


FIGURE 4 — NEW GATE TRIGGER VOLTAGE

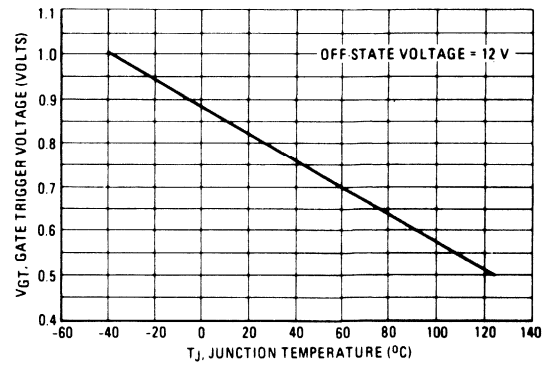


FIGURE 5 — HOLDING CURRENT

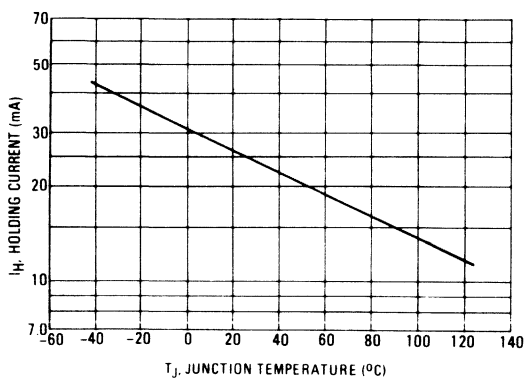


FIGURE 6 — TYPICAL FORWARD VOLTAGE

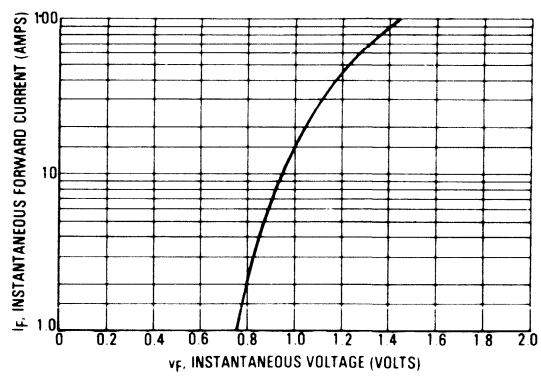
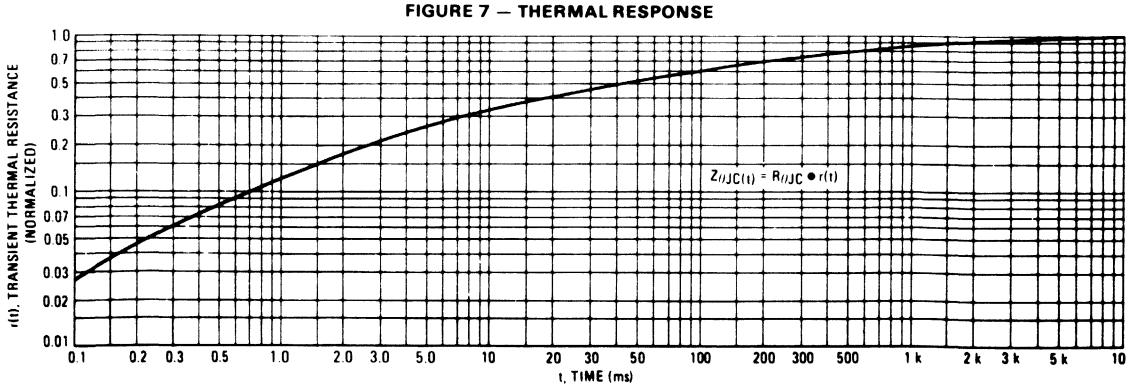


FIGURE 7 — THERMAL RESPONSE



3

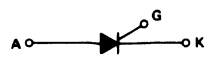
Thyristors
Silicon Controlled Rectifiers

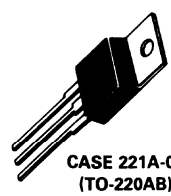
MCR265-2 thru MCR265-10

SCRs
55 AMPERES RMS
50 thru 800 VOLTS

. . . designed for inverse parallel SCR output devices for solid state relays, welders, battery chargers, motor controls or applications requiring high surge operation.

- Photo Glass Passivated Blocking Junctions for High Temperature Stability, Center Gate for Uniform Parameters
- 550 Amperes Surge Capability
- Blocking Voltage to 800 Volts





CASE 221A-04
(TO-220AB)
STYLE 3

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage, Note 1	V_{RRM}		Volts
MCR265-2		50	
MCR265-3		100	
MCR265-4		200	
MCR265-6		400	
MCR265-8		600	
MCR265-10		800	
Forward Current (T_C = 70°C) (All Conduction Angles)	$I_{T(RMS)}$ $I_{T(AV)}$	55 35	Amps
Peak Nonrepetitive Surge Current — 8.3 ms (1/2 Cycle, Sine Wave)	I_{TSM}	550	Amps
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current (300 μs, 120 PPS)	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Note 1. V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.9	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 125°C)	V_{DRM}				Volts
MCR265-2		50	—	—	
MCR265-3		100	—	—	
MCR265-4		200	—	—	
MCR265-6		400	—	—	
MCR265-8		600	—	—	
MCR265-10		800	—	—	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	2	mA
Forward "On" Voltage, Note 1 (I_{TM} = 110 A)	V_{TM}	—	1.5	1.9	Volts
Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	I_{GT}	—	20	50	mA
(T_C = −40°C)		—	40	90	
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)	V_{GT}	—	1	1.5	Volts
Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GD}	0.2	—	—	Volts
Holding Current (Anode Voltage = 12 Vdc)	I_H	—	30	75	mA
Turn-On Time (I_{TM} = 55 A, I_{GT} = 200 mAdc)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated V_{DRM}, Exponential Waveform)	dv/dt	—	50	—	V/μs

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 — AVERAGE CURRENT DERATING

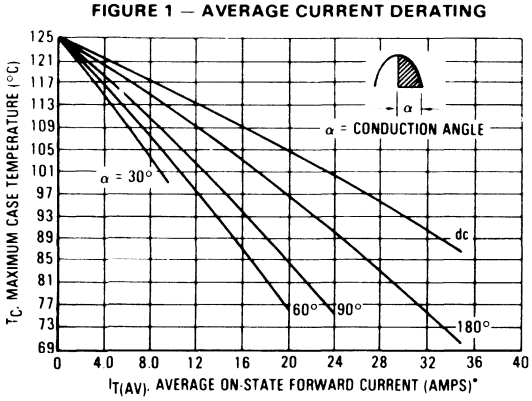
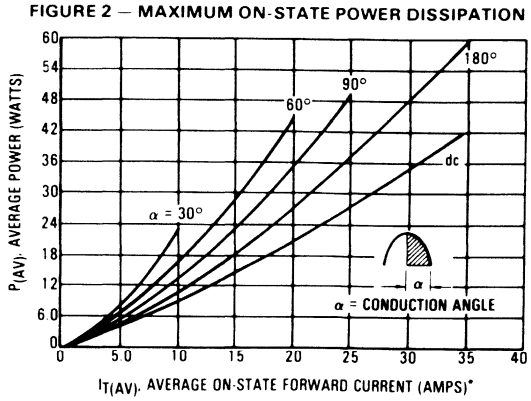


FIGURE 2 — MAXIMUM ON-STATE POWER DISSIPATION



* This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device is to be used at high sustained currents.

FIGURE 3 — GATE TRIGGER CURRENT

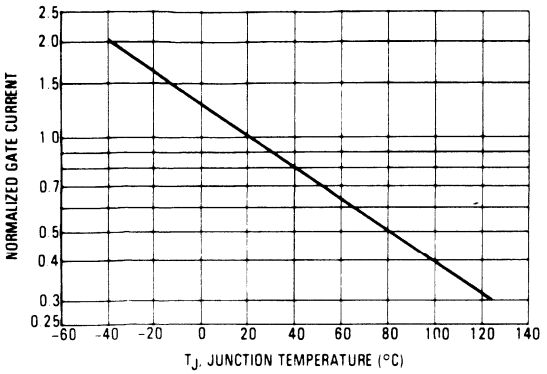


FIGURE 4 — GATE TRIGGER VOLTAGE

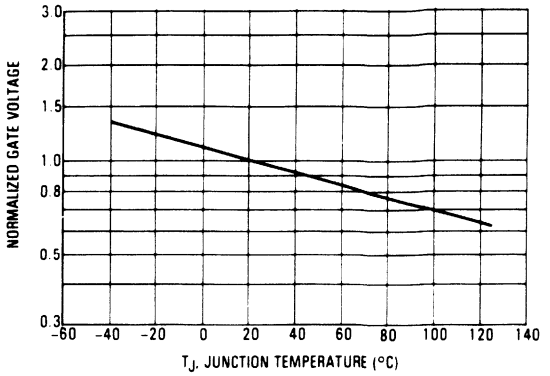


FIGURE 5 — HOLDING CURRENT

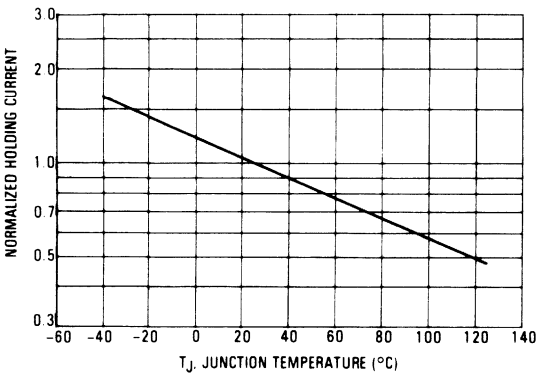


FIGURE 6 — ON-STATE CHARACTERISTICS

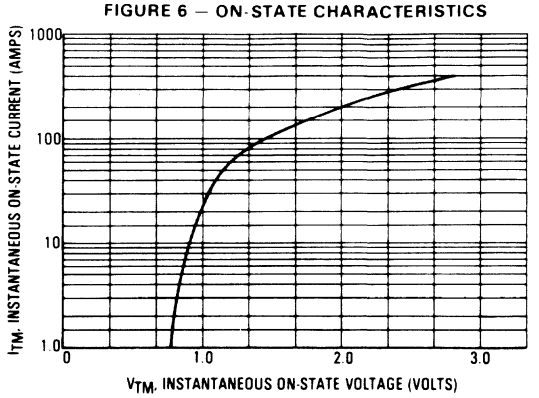
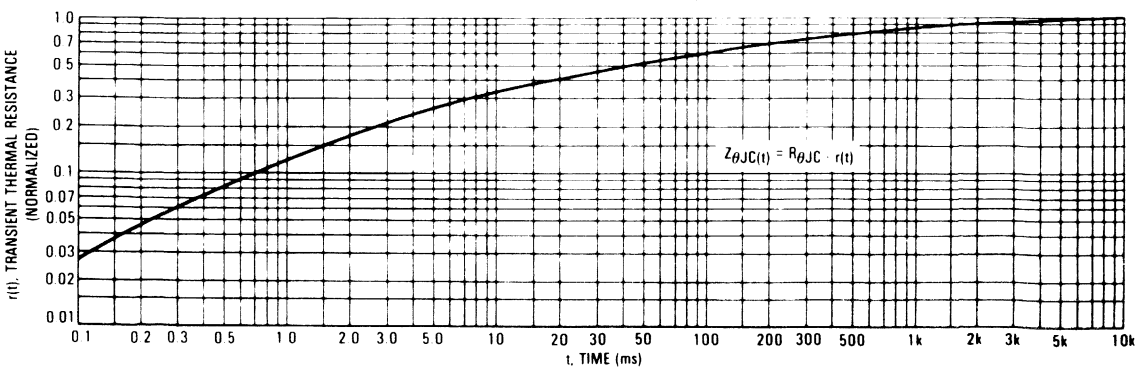


FIGURE 7 — THERMAL RESPONSE



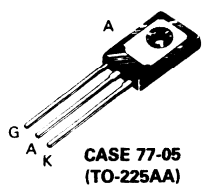
Plastic Silicon Controlled Rectifiers

MCR506 Series

SCRs
6 AMPERES RMS
50 thru 600 VOLTS

. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability.



CASE 77-05
(TO-225AA)
STYLE 2

3

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Reverse Blocking Voltage, Note 1	MCR506-2 -3 -4 -6 -8	V_{RRM}	50 100 200 400 600	Volts
RMS Forward Current (All Conduction Angles)		$I_{T(RMS)}$	6	Amp
Average Forward Current (T_C = 93°C)		$I_{T(AV)}$	3.82	Amp
Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz, T_J = −40 to 110°C)		I_{TSM}	40	Amp
Circuit Fusing Considerations (T_J = −40 to 110°C, t = 1 to 8.3 ms)		I^2t	2.6	A^2s
Peak Gate Power		P_{GM}	0.5	Watt
Average Gate Power		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GM}	0.2	Amp
Peak Reverse Gate Voltage		V_{RGM}	6	Volts
Operating Junction Temperature Range		T_J	−40 to 110	°C
Storage Temperature Range		T_{stg}	−40 to 150	°C
Mounting Torque (Note 2)		—	6	in. lb.

Notes: 1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.

2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heat sink contact pad are common. (See AN290 B)

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 110°C) MCR506-2	V_{DRM}	60	—	—	Volts
-3		100	—	—	
-4		200	—	—	
-6		400	—	—	
-8		600	—	—	
Peak Forward Blocking Current (Rated V_{DRM}, T_J = 110°C)	I_{DRM}	—	—	200	μA
Peak Reverse Blocking Current (Rated V_{RRM}, T_J = 110°C)	I_{RRM}	—	—	200	μA
Forward "On" Voltage (I_{TM} = 12 A Peak)	V_{TM}	—	—	1.9	Volts
Gate Trigger Current (Continuous dc)	I_{GT}				μA
(V_{AK} = 7 Vdc, R_L = 100 ohms)		—	—	200	
(V_{AK} = 7 Vdc, R_L = 100 ohms, T_C = −40°C)		—	—	500	
Gate Trigger Voltage (Continuous dc) (V_{AK} = 7 Vdc, R_L = 100 ohms, T_C = 25°C)	V_{GT}	—	—	1	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 ohms, T_J = 110°C)	V_{GD}	0.2	—	—	Volts
Holding Current (V_{AK} = 7 Vdc, T_C = 25°C)	I_H	—	—	5	mA
Forward Voltage Application Rate (T_J = 110°C)	dv/dt	—	10	—	V/μs

3

FIGURE 1 — CURRENT DERATING

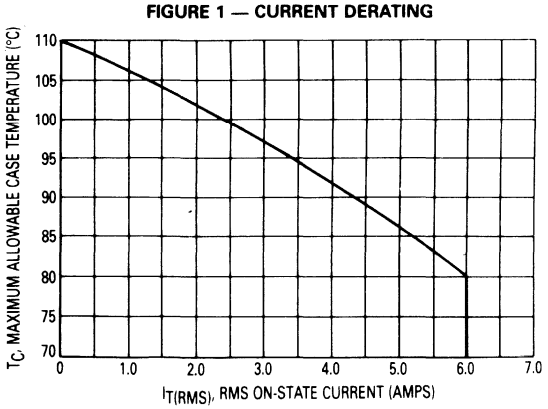
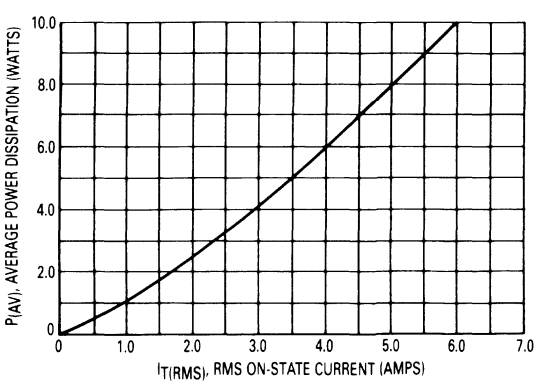


FIGURE 2 — POWER DISSIPATION



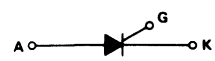
Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristor

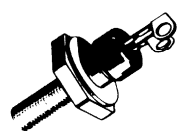
MCR729-5 thru MCR729-10

SCRs
5 AMPERES RMS
300 thru 800 VOLTS

. . . fast switching, high-voltage Silicon Controlled Rectifiers especially designed for pulse modulator applications in radar and other similar equipment.

- High-Voltage: V_{DRM} = 300 to 800 Volts
- Turn-On Times: in Nanosecond Range
- Repetitive Pulse Current to 100 Amps
- Stable Switching Characteristics Over an Operating Temperature Range From −65 to +105°C
- Pulse Repetition Rates as High as 10,000 pps





CASE 63-03
(TO-64)
STYLE 1

3

MAXIMUM RATINGS (T_J = 105°C unless otherwise noted.)

Characteristic	Symbol	Value	Unit
Peak Repetitive Forward Blocking Voltage, Note 1	V_{DRM}		Volts
MCR729-5		300	
-6		400	
-7		500	
-8		600	
-9		700	
-10		800	
Peak Repetitive Reverse Blocking Voltage, Note 1	V_{RRM}	50	Volts
Forward Current RMS	$I_{T(RMS)}$	5	Amps
Average Forward Power	$P_{F(AV)}$	5	Watts
Peak Repetitive On-State Control (PW = 10 μs)	I_{TRM}	100	Amps
Peak Forward Gate Power	P_{GFM}	20	Watts
Average Forward Gate Power	$P_{GF(AV)}$	1	Watt
Peak Forward Gate Current	I_{GFM}	5	Amps
Peak Forward Gate Voltage	V_{GFM}	10	Volts
Peak Reverse Gate Voltage	V_{GRM}	10	Volts
Operating Junction Temperature Range	T_J	−65 to +105	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque		15	in. lb.

Note 1. Ratings apply for zero or negative gate voltages. Devices shall not have a positive bias to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward and reverse blocking voltages such that the applied voltage exceeds the ratings.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_C = 105°C	I_{DRM}, I_{RRM}	—	0.2	2	mA
Gate Trigger Current (Continuous dc) (V_D = 7 Vdc, R_L = 100 ohms)	I_{GT}	—	10	50	mAdc
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 100 ohms)	V_{GT}	—	0.8	1.5	Volts
Holding Current (V_D = 7 Vdc, gate open)	I_H	3	15	—	mA
Forward On Voltage (I_{TM} = 5 A, PW ≤ 1 ms, Duty Cycle ≤ 1%)	V_{TM}	—	—	2.6	Volts
Dynamic Forward On Voltage (0.5 μs after 50% pt, I_G = 200 mA, V_D = Rated V_{DRM}, $i_{F(pulse)}$ = 30 Amps)	v_{TM}	—	15	25	Volts
Turn-On Time (t_d + t_r) (I_G = 200 mA, V_D = Rated V_{DRM})	t_{on}				ns
(i_{TM} = 30 Amps peak)		—	200	—	
(i_{TM} = 100 Amps peak)		—	400	—	
Turn-On Time Variation (T_C = +25°C to +105°C and −65°C to +25°C, I_{TM} = 30 A)	t_{on}	—	±500	—	ns
Pulse Turn-Off Time ($i_{F(pulse)}$ = 30 Amps, $I_{reverse}$ = 0) (Inductive charging circuit)	t_{rec}	—	15	—	μs
Forward Voltage Application Rate (Linear Rate of Rise) (V_D = Rated V_{DRM}, gate open, T_C = 105°C)	dv/dt	50	—	—	V/μs
Thermal Resistance (Junction to Case)	θ_{JC}	—	—	4	°C/W

3

Silicon Controlled Rectifier
Reverse Blocking Triode Thyristor

MCR1718-5 thru MCR1718-8

SCRs
25 AMPERES RMS
300 thru 600 VOLTS

. . . fast switching, high-voltage thyristors especially designed for pulse modulator applications.

- High-Voltage Capability from 300 to 600 Volts
- Repetitive Pulse Current to 1000 Amps
- Pulse Repetition as High as 4000 pps
- Current Application Rate as High as 1000 A/μs

CASE 263-04
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Forward or Reverse Blocking Voltage, Note 1 MCR1718-5 -6 -7 -8	V_{DRM} V_{RRM}	 300 400 500 600	Volts
Peak Reverse Blocking Voltage (Transient) (Non-Recurrent 5 ms (max)) MCR1718-5 -6 -7 -8	V_{RSM}	 400 500 600 700	Volts
Forward Current RMS	$I_{T(RMS)}$	25	Amps
Peak Forward Surge Current (1–10 μs Pulse Width)	I_{TSM}	1000	Amps
Current Application Rate (up to 1000 A peak)	di/dt	1000	A/μs
Circuit Fusing (T_J = −65 to +125°C; t ≤ 1 ms)	I^2t	250	A^2s
Dynamic Average Power (T_C = 65°C)	$P_{F(AV)}$	30	Watts
Peak Gate Power — Forward	P_{GM}	20	Watts
Average Gate Power — Forward	$P_{G(AV)}$	1	Watt
Peak Gate Current — Forward	I_{GM}	5	Amps

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage.

(cont.)

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Peak Gate Voltage	V_{GM}	10	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 125°C		—	—	8	mA
Forward "On" Voltage (I_{TM} = 25 Adc)	V_{TM}	—	1.1	1.3	Volts
Dynamic Forward On Voltage (I_{GT} = 500 mA, I_{pulse} = 500 Amps) (1 μs after start (10% pt.) of I_{pulse})	v_{TM}	—	30	—	
(5 μs after start (10% pt.) of I_{pulse})		—	5	—	
Gate Trigger Current (Continuous dc) (V_D = 7 Vdc, R_L = 50 Ohms)	I_{GT}	—	10	50	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 50 Ohms)	V_{GT}	—	0.8	1.5	Volts
(V_D = Rated V_{DRM}, R_L = 50 Ohms, T_J = 125°C)	V_{GD}	0.25	—	—	
Holding Current (V_D = 7 Vdc, Gate Open)	I_H	5	15	—	mA
(V_D = 7 Vdc, Gate Open, T_J = 125°C)		—	6	—	
Circuit Commutated Turn-Off Time (I_F = 500 A, I_R = 10 A, dv/dt = 20 V/μs V_D = Rated V_{DRM}, V_R = Rated V_{RRM}) (Conductive Charging Circuit — Circuit dependent)	t_q	—	20	—	μs
Critical Exponential Rate of Rise (Gate Open, T_J = 125°C, V_D = Rated V_{DRM})	dv/dt	—	100	—	V/μs

3

Silicon Controlled Rectifiers

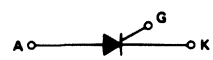
Reverse Blocking Triode Thyristors

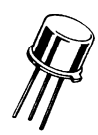
MCR1906 Series

SCRs
1.6 AMPERES RMS
50 thru 400 VOLTS

These devices are glassivated planar construction designed for applications in control systems and sensing circuits where low-level gating and holding characteristics are necessary.

- Low-Level Gate Characteristics — I_{GT} = 1 mA (Max) @ T_C = 25°C
- Low Holding Current — I_H = 5 mA (Max) @ T_C = 25°C
- Glass-to-Metal Bond for Maximum Hermetic Seal





CASE 79-04
(TO-205AD)
STYLE 3

MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Repetitive Peak Reverse Blocking Voltage MCR1906-2 MCR1906-3 MCR1906-4 MCR1906-6 MCR1906-8	V_{RRM}	 50 100 200 400 600	Volts
RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amp
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_J = −40 to +110°C) Preceded and followed by rated current and voltage	I_{TSM}	15	Amps
Peak Gate Power	P_{GM}	0.1	Watt
Average Gate Power	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current	I_{GM}	0.1	Amp
Peak Gate Voltage	V_{GM}	6	Volts
Operating Junction Temperature Range	T_J	−65 to +110	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Solder Temperature (>1/16" From Case, 10 s max)	—	+230	°C

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (R_{GK} = 1000 Ohms)	MCR1906-2	V_{DRM}	50	—	—	Volts
	MCR1906-3		100	—	—	
	MCR1906-4		200	—	—	
	MCR1906-6		400	—	—	
	MCR1906-8		600	—	—	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, R_{GK} = 1000 Ohms)	T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
	T_J = 110°C		—	—	500	μA
Peak On-State Voltage (Pulsed, 1 ms max, Duty Cycle ≤ 1%) (I_F = 1 Adc peak)		V_{TM}	—	—	1.75	Volt
Gate Trigger Current (Continuous dc) (V_{AK} = 7 V, R_L = 100 ohms)		I_{GT}	—	—	1	mAdc
Gate Trigger Voltage (Continuous dc)		V_{GT}				Volt
(V_{AK} = 7 V, R_L = 100 ohms)			—	—	1	
(V_{AK} = Rated V_{DRM}, R_L = 100 ohms, R_{GK} = 1000 Ohms, T_J = 110°C)			0.1	—	—	
Holding Current (V_{AK} = 7 V, R_{GK} = 1000 ohms)		I_H	—	—	5	mA
Turn-On Time		t_{gt}				μs
(I_{GT} = 10 mA, I_F = 1 A)			—	0.8	—	
(I_{GT} = 20 mA, I_F = 1 A)			—	0.6	—	
Turn-Off Time (I_F = 1 A, I_R = 1 A, dv/dt = 20 V/μs, T_J = 110°C)		t_q	—	10	—	μs

3

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE REFERENCE

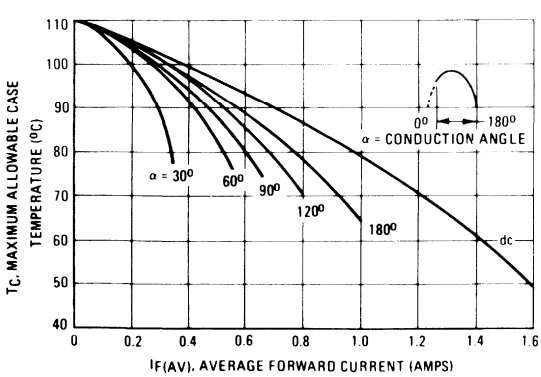
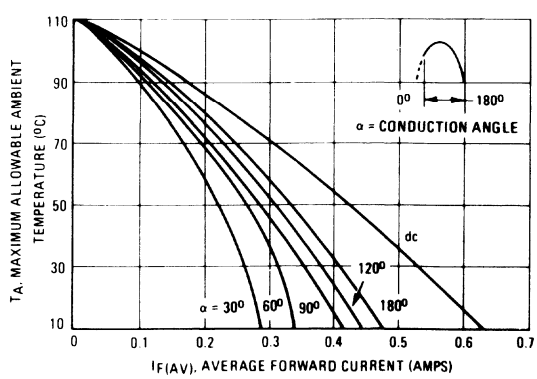


FIGURE 2 – AMBIENT TEMPERATURE REFERENCE



Silicon Controlled Rectifier

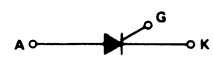
Reverse Blocking Triode Thyristor

MCR3818 Series
MCR3918 Series

SCRs
25 AMPERES RMS
50 thru 800 VOLTS

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Supplied in Either Pressfit or Stud Package
- High Surge Current Rating — I_{TSM} = 240 Amps
- Low On-State Voltage — 1.2 V (Typ) @ I_{TM} = 20 Amps
- Practical Level Triggering and Holding Characteristics — 40 mA (Max) and 50 mA (Max) @ T_C = 25°C



CASE 174-04
(TO-203)
STYLE 1
MCR3818 Series

CASE 175-03
STYLE 1
MCR3918 Series

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage, Note 1	V_{DRM} or V_{RRM}		Volts
MCR3818, MCR3918-2		50	
-3		100	
-4		200	
-6		400	
-8		600	
-10		800	
Non-Repetitive Reverse Blocking Voltage	V_{RSM}		Volts
MCR3818, MCR3918-2		75	
-3		150	
-4		300	
-6		500	
-8		700	
-10		900	
On-State Current RMS	$I_{T(RMS)}$	20	Amps
Average On-State Current (T_C = 67°C)	$I_{T(AV)}$	13	Amps
Circuit Fusing (T_J = −40 to +100°C, t ≤ 8.3 ms)	I^2t	235	A^2s
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_J = −40 to +100°C)	I_{TSM}	240	Amps
Peak Gate Power (Maximum Pulse Width = 10 μs)	P_{GM}	5	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current (Maximum Pulse Width = 10 μs)	I_{GM}	2	Amps

Note 1. V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. These devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

3

MAXIMUM RATINGS — continued

Rating	Symbol	Value	Unit
Peak Gate Voltage	V_{GM}	10	Volts
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Stud Torque		30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$			°C/W
Pressfit Package		1	1.5	
Stud Package		1.1	1.6	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	10	μA
T_J = 100°C		—	5	mA
Gate Trigger Current (Continuous dc)	I_{GT}			mA
(V_D = 7 Vdc, R_L = 100 Ω)		—	40	
(V_D = 7 Vdc, R_L = 100 Ω, T_C = −40°C)		—	75	
Gate Trigger Voltage (Continuous dc)	V_{GT}			Volts
(V_D = 7 Vdc, gate open)		—	1.5	
(V_D = 7 Vdc, R_L = 100 Ω, T_C = −40°C)		—	2.5	
(V_D = Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)		0.2	—	
Peak On-State Voltage (Pulse Width = 1 ms max, duty cycle ≤ 1%)	V_{TM}			Volts
(I_{TM} = 20 A)		—	1.5	
(I_{TM} = 41 A)		—	1.7	
Holding Current	I_H			mA
(V_D = 7 Vdc, gate open)		—	50	
(V_D = 7 Vdc, gate open, T_C = −40°C)		—	90	
		Typical		
Gate Controlled Turn-On Time (t_d + t_r) (I_{TM} = 20 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	1		μs
Circuit Commutated Turn-Off Time	t_q			μs
(I_{TM} = 10 A, I_R = 10 A)		20		
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C)		30		
(V_D = V_{DRM} = rated voltage) (dv/dt = 30 V/μs)				
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Wave Form, Gate open, T_J = 100°C)	dv/dt	50		V/μs

3

EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – GATE TRIGGER CURRENT

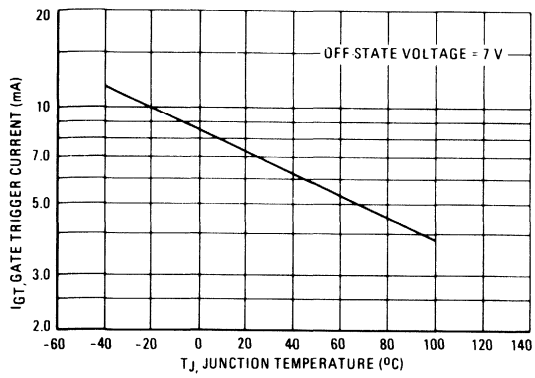
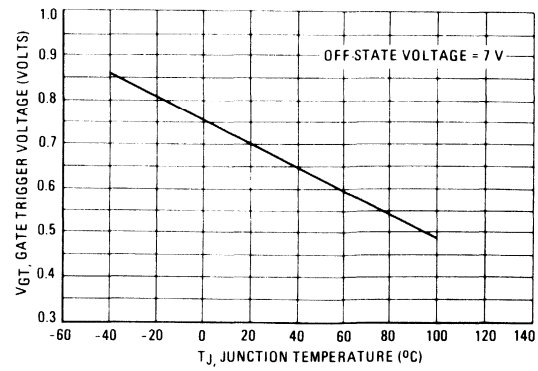


FIGURE 2 – GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-REPETITIVE SURGE CURRENT

FIGURE 3 – 60 Hz SURGES

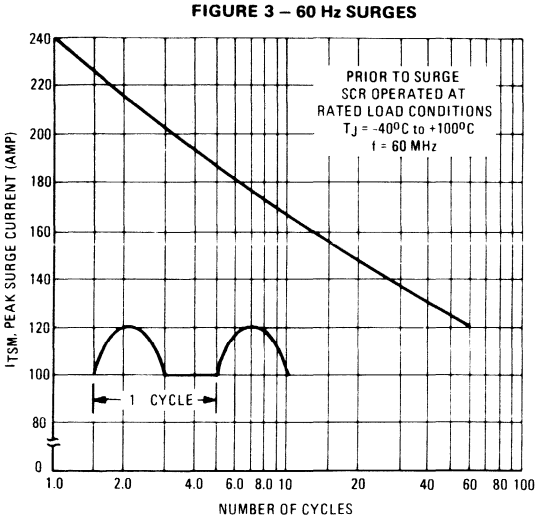


FIGURE 4 – SUB-CYCLE SURGES

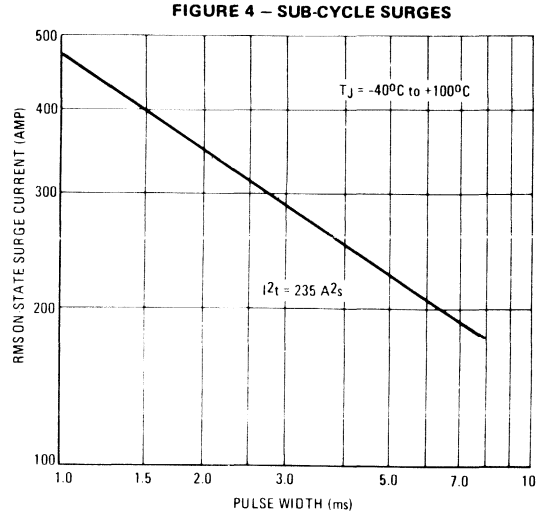


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FIGURE 5 – GATE TRIGGER CHARACTERISTICS

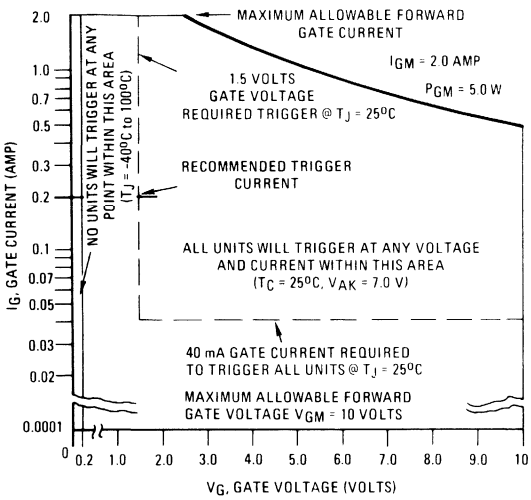
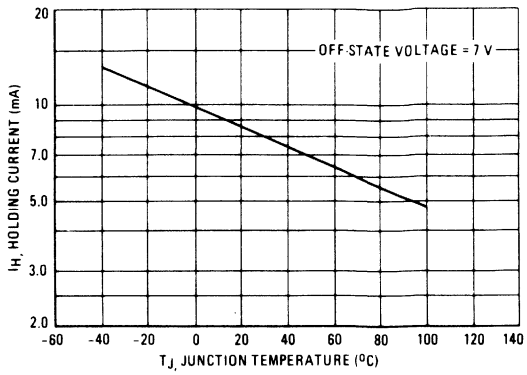


FIGURE 6 – EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT



DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

FIGURE 7 – AVERAGE CURRENT DERATING

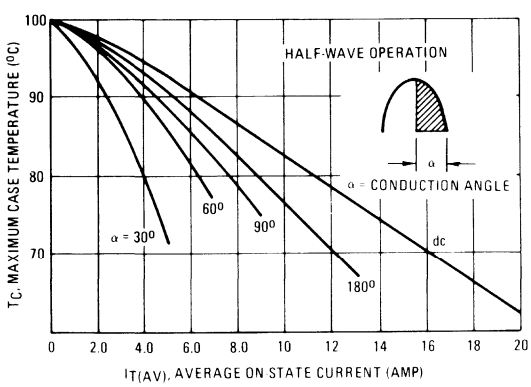


FIGURE 8 – ON-STATE POWER DISSIPATION

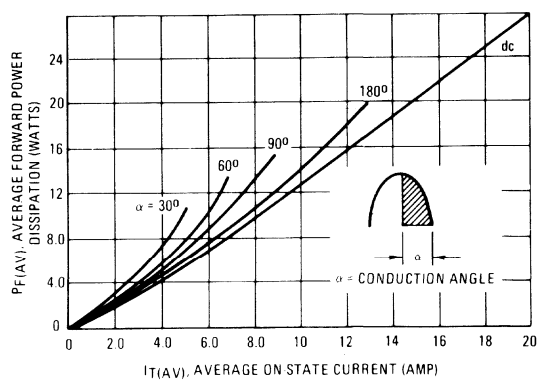


FIGURE 9 – ON-STATE CHARACTERISTICS

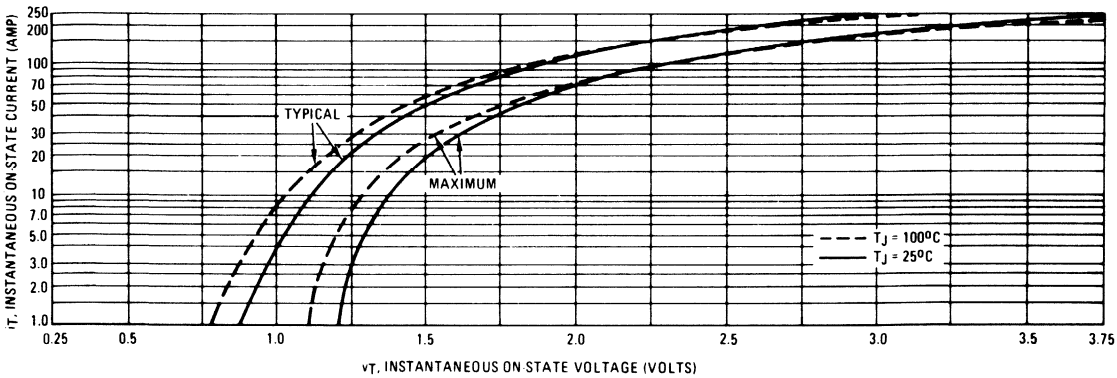


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

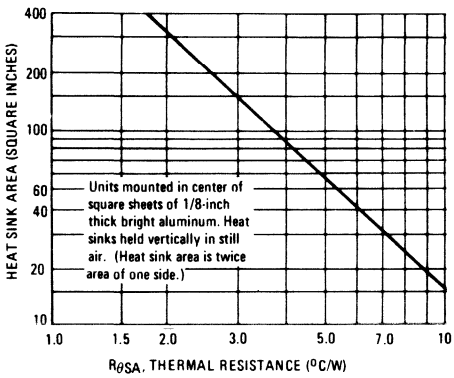
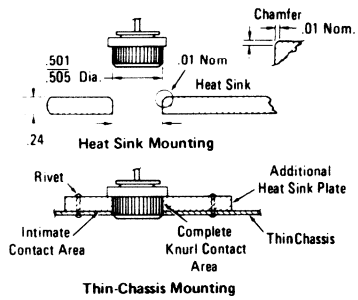


FIGURE 11 – MOUNTING DETAILS FOR PRESSFIT THYRISTORS



The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the rectifier during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the rectifier case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heat sink material. Recommended hardnesses are: copper – less than 50 on the Rockwell F scale; aluminum – less than 65 on the Brinell scale. A heat sink as thin as 1/8″ may be used, but the interface thermal resistance will increase in proportion to the reduction of contact area. A thin chassis requires the addition of a back-up plate.

3

Silicon Controlled Rectifier
Reverse Blocking Triode Thyristor

MCR3835 Series
MCR3935 Series

SCRs
35 AMPERES RMS
50 thru 800 VOLTS

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 350 Amps
- Low Forward "On" Voltage — 1.2 V (Typ) @ I_{TM} = 35 Amps
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit or Stud Package
- Glass Passivated Junctions for Maximum Reliability

CASE 174-04
(TO-203)
STYLE 1
MCR3835 Series

CASE 175-03
STYLE 1
MCR3935 Series

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage	V_{DRM}		Volts
Note 1 MCR3835-2	V_{RRM}	50	
-8		600	
-10		800	
MCR3935-2		50	
-3		100	
-4		200	
-6		400	
-8		600	
-10		800	
Peak Non-Repetitive Reverse Blocking Voltage	V_{RSM}		Volts
(t ≤ 5 ms) MCR3835-2		35	
-8		700	
-10		900	
MCR3935-2		75	
-3		150	
-4		300	
-6		500	
-8		700	
-10		900	
Forward Current RMS	$I_{T(RMS)}$	35	Amps
Peak Surge Current (One Cycle, 60 Hz, T_J = −40 to +125°C)	I_{TSM}	350	Amps
Circuit Fusing (T_J = −40 to +100°C, t = 1 to 8.3 ms)	I^2t	510	A^2s
Peak Gate Power	P_{GFM}	5	Watts
Average Gate Power	$P_{GF(AV)}$	0.5	Watt
Peak Forward Gate Current	I_{GFM}	2	Amps
Peak Gate Voltage — Forward	V_{GFM}	10	Volt
Reverse	V_{GRM}	10	
Operating Junction Temperature Range	T_J	−40 to +125	°C

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Storage Temperature Range	T_{stg}	−40 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
MCR3835		1.2	
MCR3935		1.3	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 100°C		—	1	5	mA
Forward "On" Voltage (I_{TM} = 35 A Peak)	V_{TM}	—	1.2	1.5	Volts
Gate Trigger Current (Continuous dc) (V_D = 7 V, R_L = 100 Ω)	I_{GT}	—	10	40	mA
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_D = 7 V, R_L = 100 Ω)		—	0.7	1.5	
(V_D = Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)	V_{GD}	0.2	—	—	
Holding Current (V_D = 7 V, gate open)	I_H	—	10	50	mA
Turn-On Time (t_d + t_r) (I_{TM} = 35 Adc, I_{GT} = 40 mAdc)	t_{on}	—	1	—	μs
Turn-Off Time	t_q				μs
(I_{TM} = 10 A, I_R = 10 A)		—	20	—	
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C)		—	30	—	
Forward Voltage Application Rate (V_D = Rated V_{DRM}, T_J = 100°C)	dv/dt	—	50	—	V/μs

3

FIGURE 1 – CURRENT DERATING

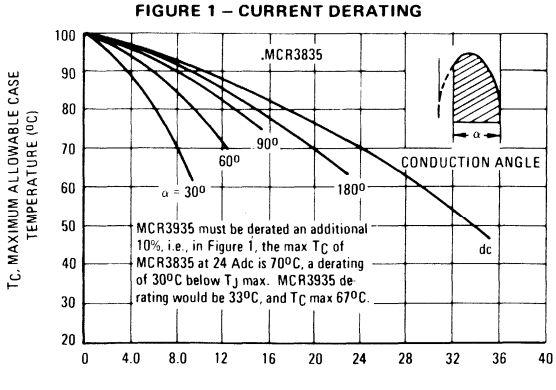


FIGURE 2 – TYPICAL POWER DISSIPATION

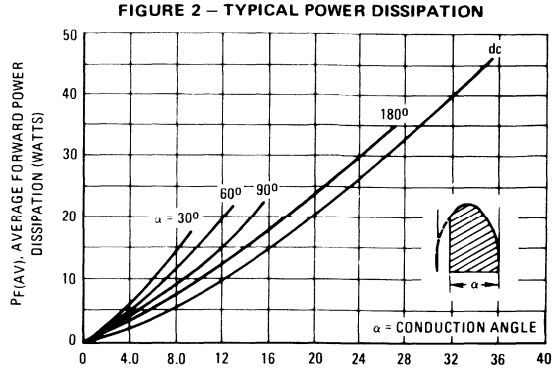


FIGURE 3 – TYPICAL GATE TRIGGER CURRENT

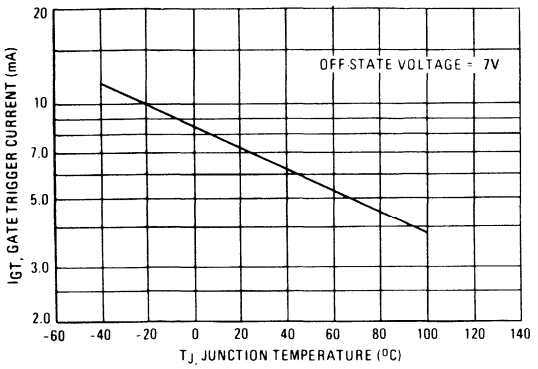
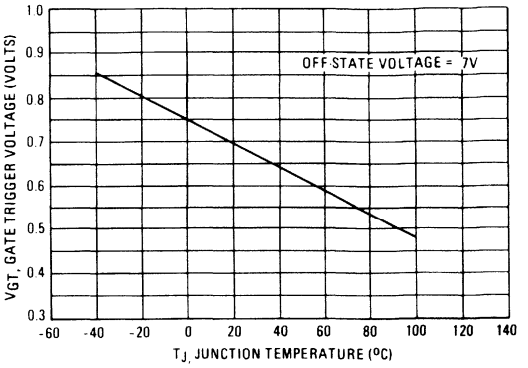


FIGURE 4 – TYPICAL GATE TRIGGER VOLTAGE



3

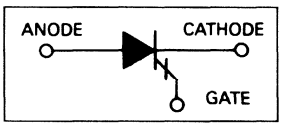
Gate Turn-Off Thyristors

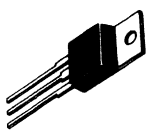
MGTO1000
MGTO1200

GTOs
18 AMPERES RMS
1000 and 1200 VOLTS

The GTO is a family of asymmetric gate turn-off thyristors designed primarily for dc power switching applications such as motor drives, switching power supplies, inverters, or wherever a need exists for high surge current capabilities and fast switching speeds.

- Fast Turn-Off With Reverse Gate Pulse
- High Voltage — V_{DRXM} = 1000 and 1200 Volts
- Momentary Forward Pulse For Turn-On
- Minimizes Drive Losses
- Interdigitated Emitter Geometry Aids Turn-On Current Spreading and Improves Turn-On di/dt
- Clip and Current Spreading Ring for Reliable High Surge Capability — I_{TSM} = 200 A





CASE 221A-04
(TO-220AB)
STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = −40 to +125°C, 1/2 Sine Wave 50 to 60 Hz) Note 1	V_{DRXM}	1000 1200	Volts
Repetitive Peak Reverse Voltage, Gate Open (T_J = −40 to +125°C), Note 2	V_{RRM}	15	Volts
Repetitive Peak Reverse Gate Voltage, Note 3	V_{GRM}	15	Volts
On-State Current at T_C = 65°C (1/2 Cycle Sine Wave, 50 to 60 Hz)	$I_{T(RMS)}$	18	Amps
Peak Nonrepetitive Surge Current (8.3 ms Conduction, Half Sine Wave T_C = 65°C)	I_{TSM}	200	Amps
Circuit Fusing (T_J = −40 to +125°C, t = 8.3 ms)	I^2t	167	A^2s
Repetitive Controllable On-State Current, Note 4	I_{TCM}	50	Amps
Nonrepetitive Maximum Interruptable On-State Current, Note 5	I_{TCSM}	70	Amps
Peak Forward Gate Power	P_{GFM}	10	Watts
Average Forward Gate Power	$P_{GF(AV)}$	3	Watts
Peak Reverse Gate Power	P_{GRM}	400	Watts
Average Reverse Gate Power	$P_{GR(AV)}$	5	Watts
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Notes: 1. V_{DRXM} for all types can be applied on a continuous basis without damage. Ratings apply for R = 39 Ω or shorted gate conditions or negative voltage on the gate. Devices should not be tested for blocking voltage such that the supply voltage exceeds the rating of the device.
2. This is an asymmetric anode shorted part with a blocking gate-cathode junction. The ability to support a reverse voltage depends on the gate-cathode terminal conditions. Gate-cathode reverse bias increases V_{RRM}.
3. Instantaneous voltage at turn-off may exceed rated V_{GRM} provided P_{GRM} is not exceeded.
4. V_D Maximum Peak = V_{DRXM} − 300 V, T_J < 125°C, L_G = 2 μH, V_{GR} = 12 V (See Figure 2)
   C_S = 0.1 μF for MGTO1000
   C_S = 0.05 μF for MGTO1200
5. V_D Maximum Peak = V_{DRXM} − 300 V, T_J < 125°C, L_G = 2 μH, V_{GR} = 12 V (See Figure 2)
   C_S = 0.2 μF for MGTO1000
   C_S = 0.1 μF for MGTO1200

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted), Note 1

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, R_{GK} = 39 Ω, T_J = 125°C)	I_{DRM}	—	—	5	mA
Peak On-State Voltage (I_{TM} = 50 A, Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%, I_{GT} = 300 mAdc)	V_{TM}	—	2.7	3.1	Volts
Peak Gate Trigger Current (V_D = 12 Vdc, R_L = 1.4 Ω, Pulse Width ≥ 10 μs)	I_{GTM}	—	60	300	mA
Peak Gate Trigger Voltage (V_D = 12 Vdc, R_L = 1.4 Ω, Pulse Width ≥ 10 μs)	V_{GTM}	—	0.8	1.5	Volts
Reverse Gate Leakage Current (V_{GRM} = 15 V, T_J = 125°C)	I_{GRM}	—	—	5	mA
Latching Current (PW = 300 μs, f = 60 Hz, Gate Pulse = 1 A, 10 μs, V_D = 12 Vdc)	I_L	—	1	—	Adc
Holding Current (PW = 300 μs, f = 60 Hz, Gate Pulse = 1 A, 10 μs, Anode Pulse = 6 A, 100 μs, V_D = 12 Vdc)	I_H	—	700	—	mA

SWITCHING CHARACTERISTICS (T_J = 25°C unless otherwise noted)

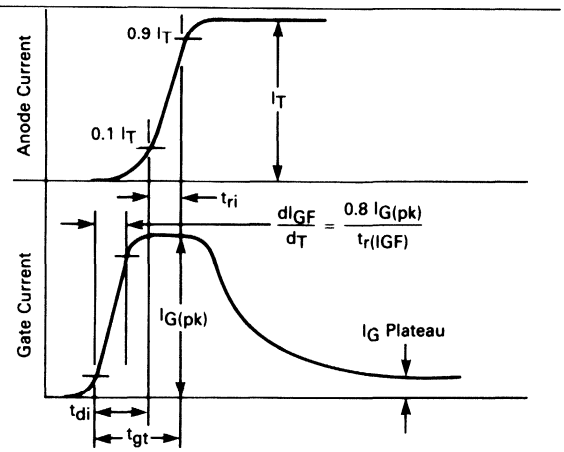
RESISTIVE TURN-ON SWITCHING						
Gate Turn-On Time	V_D = 600 V, I_T = 50 A $I_{G(pk)}$ = 6 A, C_S = 0.1 μF dig/dt ≥ 7 A/μs See Figure 1 and Table 1(A)	t_{gt}	—	1.5	—	μs
Turn-On Delay Time		t_{di}	—	0.6	—	
Rise Time		t_{ri}	—	0.9	—	
INDUCTIVE TURN-OFF SWITCHING						
Gate Tun-Off Time	$V_{D(pk)}$ = 700 V, I_T = 50 A, V_{GR} = 12 V $I_{G(pk)}$ = 6 A L_G = 2 μH, C_S = 0.1 μF See Figure 2 and Table 1(B)	t_{gq}	—	3	—	μs
Storage Time		T_{si}	—	2.6	—	
Fall Time		T_{fi}	—	0.4	—	
GATE TURN-OFF CHARGE						
Gate Charge	$V_{D(pk)}$ = 700 V, I_T = 50 A V_{GR} = 12 V L_G = 2 μH, C_S = 0.1 μF See Table 1(B)	Q_{GQ}	—	35	—	μC
Peak Reverse Gate Current		I_{GQ}	—	17	—	A
Peak Tail Current		I_{TLP}	—	5	—	
STATIC dv/dt						
Critical Exponent of Rise Time	$V_{(pk)}$ = V_{DRM} − 400 V R_{GK} = 39 Ω, T_J = 125°C Linear Waveform	dv/dt	—	10,000	—	V/μs

Note 1. This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat-sinking is used at sustained currents (see derating curves).

TABLE 1 — TERMS, SYMBOLS AND DEFINITIONS FOR SWITCHING WITH GTO'S

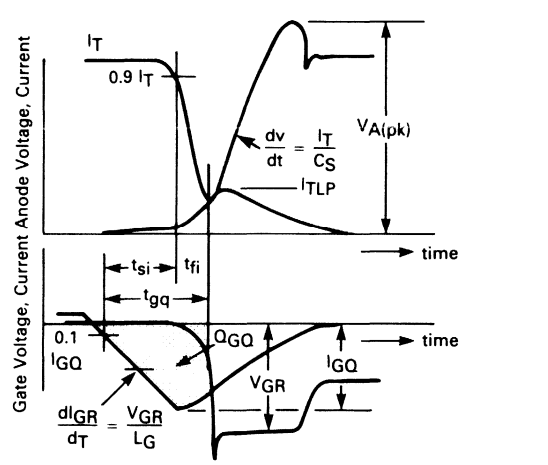
NOTE: The parameters are shown on two separate graphs for clarity.

Terms	Symbols	Definitions
RESISTIVE TURN-ON SWITCHING		
Turn-On Time	t_{gt}	
Delay Time	t_{di}	
Rise Time	t_{ri}	



(A)

INDUCTIVE TURN-OFF SWITCHING		
Gate Controlled Turn-Off Time	t_{gq}	
Current Storage Time	t_{si}	
Current Fall Time	t_{fi}	
Turn-Off Gate Charge	Q_{GQ}	
Peak Tail Current	I_{TLP}	

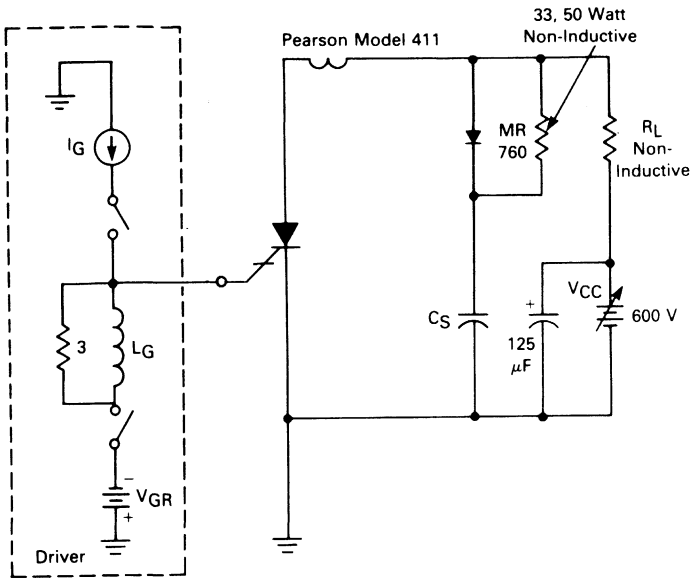


(B)

t_{si} — current storage time 10% I_{GR} to 90% I_T
t_{fi} — current fall time 90% I_T to I_{TLP} inflection point
t_{gq} — gate controlled turn-off time (t_{si} + t_{fi})
t_{di} — current delay time. 10% $I_{G(pk)}$ to 10% I_T
t_{ri} — current rise time. 10% I_T to 90% I_T
t_{gt} — turn-on time (t_{di} + t_{ri})

3

FIGURE 1 — RESISTIVE SWITCHING TEST CIRCUIT (TURN-ON)

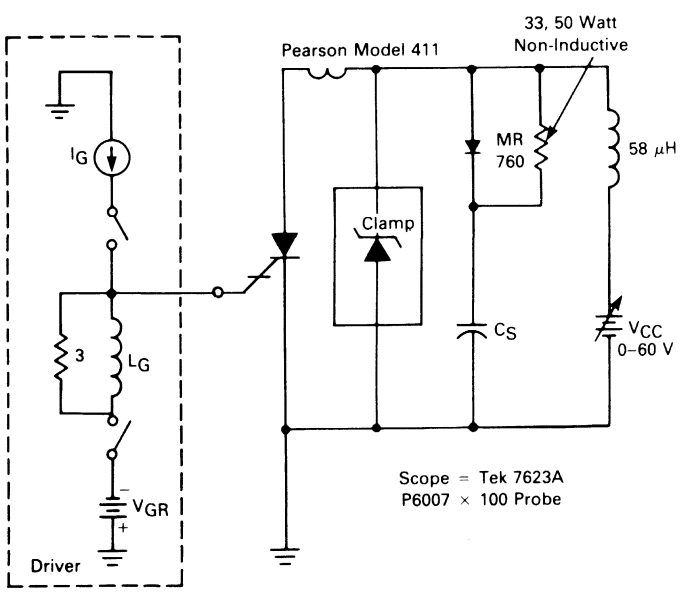


V_{GR} = 12 V
I_T = 50 A Peak
$I_{G(pk)}$ = 6.0 A $di_g/dt \geq 7.0$ A/μs
L_G = 2.0 μH
C_S = 0.1 μF
V_{CC} = Specified Value
PW = 150 μs
f = 10 Hz

Adjust R_L as required for I_T peak.

3

FIGURE 2 — INDUCTIVE SWITCHING TEST CIRCUIT (TURN-OFF)



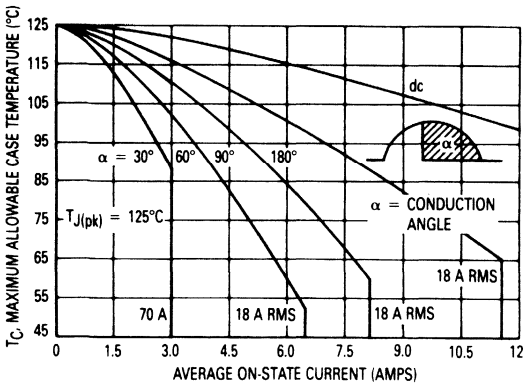
V_{GR} = 12 V
I_T = 50 A Peak
*L_G = 2.0 μH
C_S as specified
PW = 150 μs
f = 10 Hz
Adjust V_{CC} for specified I_T

*L_G: 1 Layer Air Core
2 3/4" OD 45 Turns No. 14 AWG

Clamp: MOSORB Transient Suppressor Zener Series Stack, 1N6292 or 1.5KE75 adjusted for specified $V_{(pk)}$

These circuits are used to evaluate the GTO maximum ratings and switching characteristics

FIGURE 3 — 50–60 Hz HALF WAVE CURRENT DERATING



NOTE: Sine wave and rectangular chopper curves allow estimation of heat sink requirements at low frequencies (50 or 60 Hz) where switching losses are low compared to conduction losses. Heat sink sizes should be based on conduction angles that include the worst case peak current as well as the longest conduction time. Operation at high frequencies should also be evaluated using the pulsed rating curves. Surge operation with high power pulses may require determination of the pulse power, energy, and peak T_J rise to achieve safe turn-off.

FIGURE 4 — 50–60 Hz FULL WAVE CURRENT DERATING

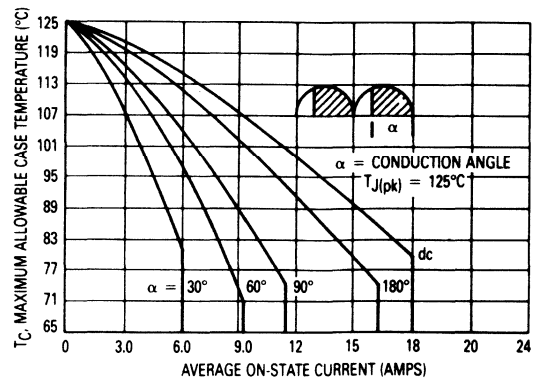


FIGURE 5 — CURRENT DERATING 50–60 Hz RECTANGULAR WAVEFORM

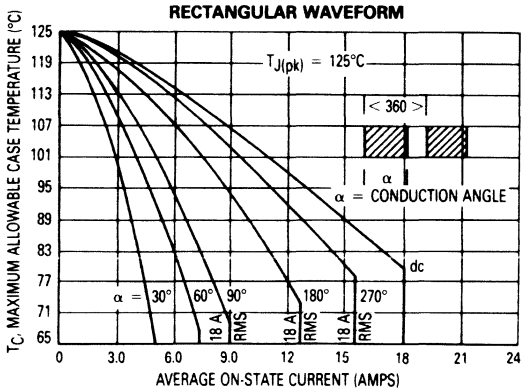


FIGURE 6 — HALF WAVE 50–60 Hz POWER DISSIPATION

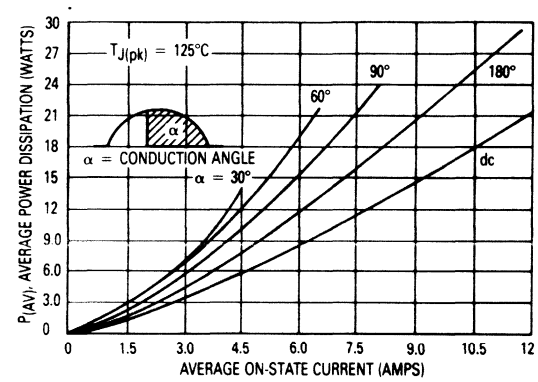


FIGURE 7 — FULL WAVE 50–60 Hz POWER DISSIPATION

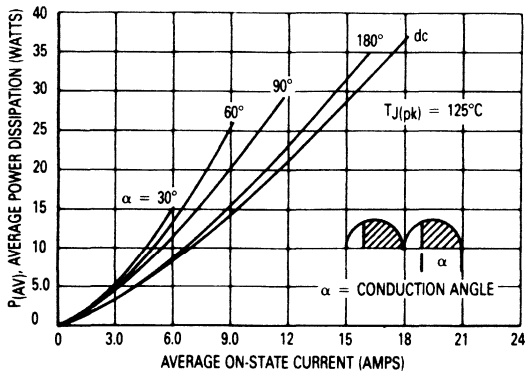


FIGURE 8 — POWER DISSIPATION versus FORWARD CURRENT RECTANGULAR WAVEFORM

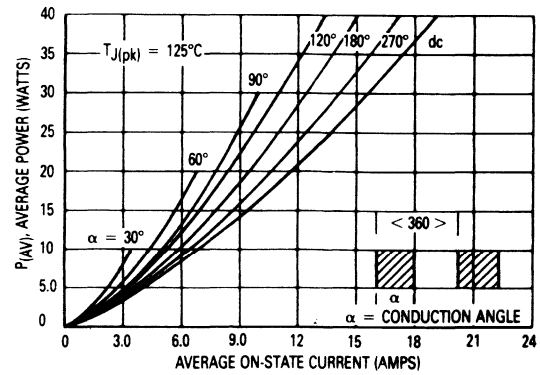


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FIGURE 9 — FIRING CHARACTERISTICS

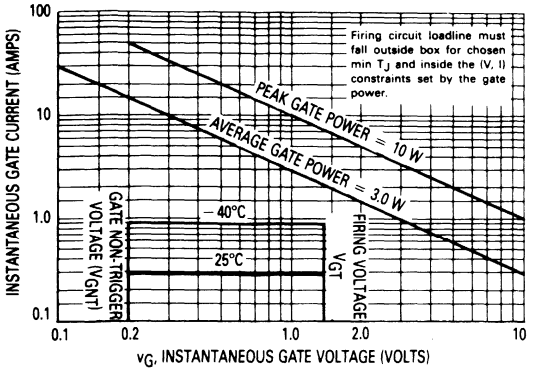


FIGURE 10 — NONREPETITIVE SURGE CHARACTERISTICS

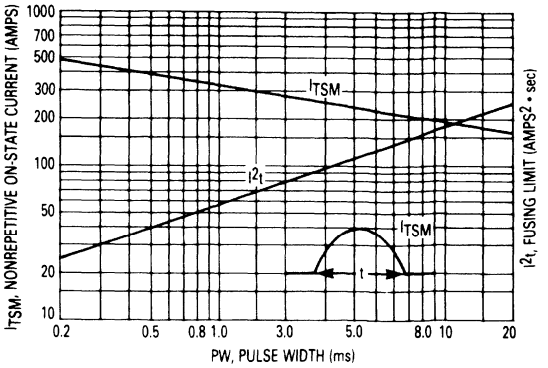
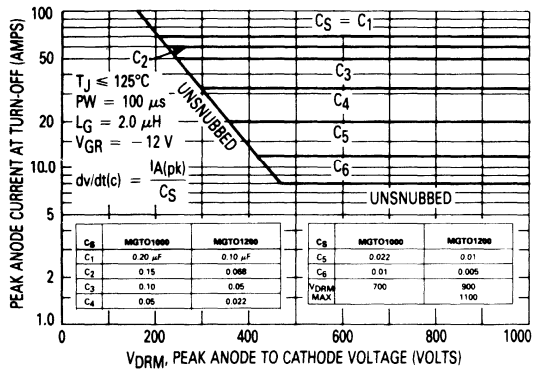


FIGURE 11 — MAXIMUM INTERRUPTABLE CURRENT



C_S	MGTO1000	MGTO1200
C_1	0.20 μF	0.10 μF
C_2	0.15	0.068
C_3	0.10	0.05
C_4	0.05	0.022

C_S	MGTO1000	MGTO1200
C_5	0.022	0.01
C_6	0.01	0.005
V_{DRM} MAX	700	900 1100

NOTE: In bridge inverter configurations the upper and lower snubber capacitors are in parallel, permitting a snubber $\geq \frac{C_S}{2}$ when stray inductance is kept low. Unsnubbed operation is not recommended although high currents at low voltages can be switched, given well defined load conditions. The use of a small snubber insures that the worst case dv/dt stress is known.

FIGURE 12 — MAXIMUM FORWARD VOLTAGE versus CURRENT

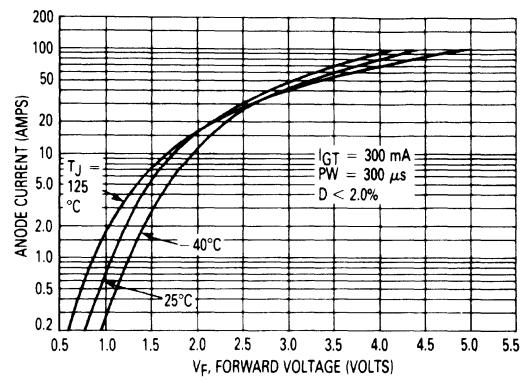


FIGURE 13 — TYPICAL GATE TRIGGER CURRENT

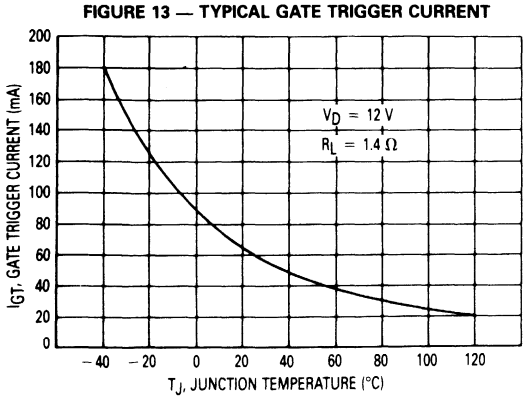


FIGURE 14 — TYPICAL GATE TRIGGER VOLTAGE

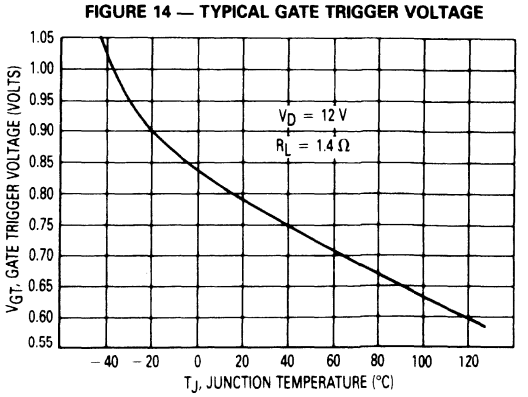


FIGURE 15 — THERMAL RESPONSE

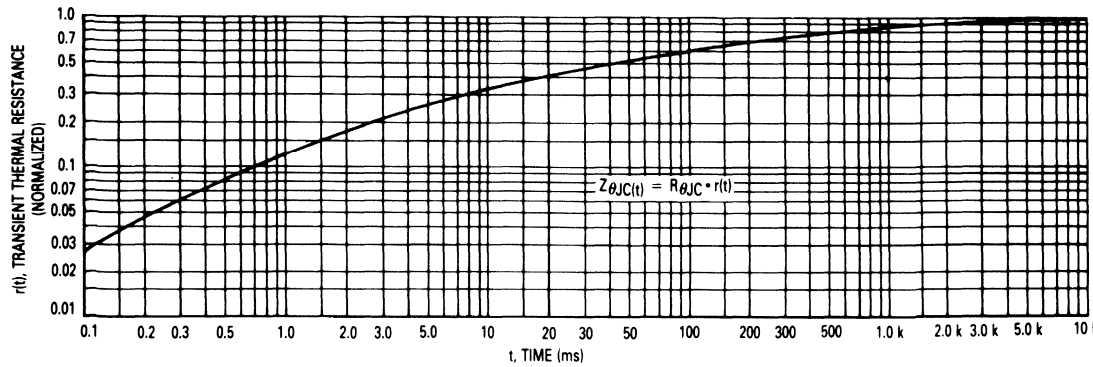


FIGURE 16 — TYPICAL LATCHING CURRENT

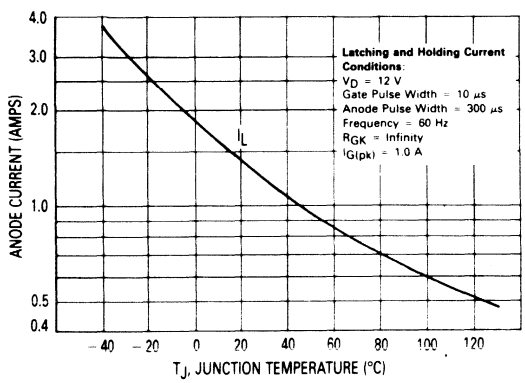


FIGURE 17 — TYPICAL TURN-OFF DYNAMICS

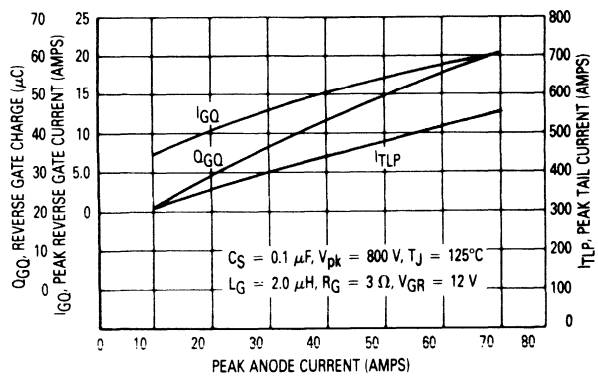


FIGURE 18 — TYPICAL TURN-OFF SWITCHING SPEED

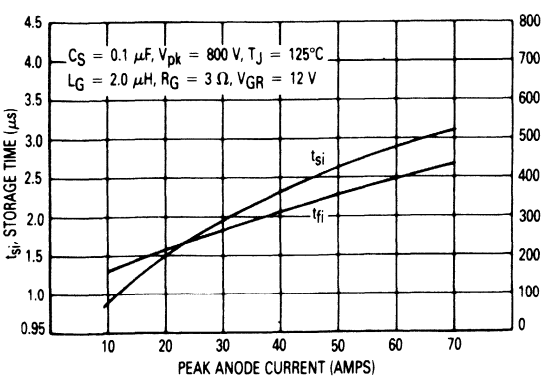


FIGURE 19 — CONDUCTION ENERGY PER PULSE

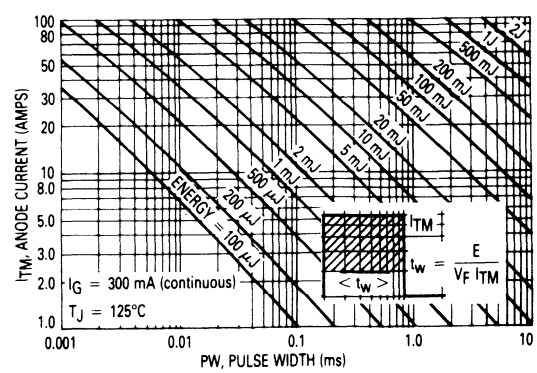


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FIGURE 20 — ENERGY PER PULSE AT TURN-ON

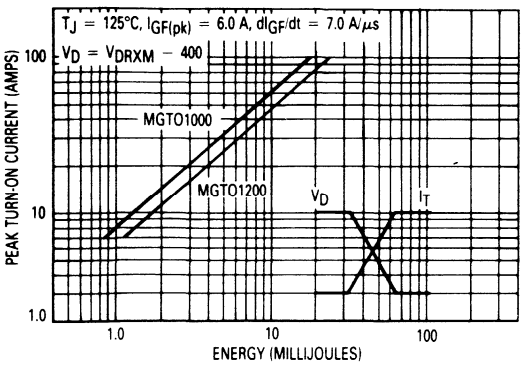


FIGURE 21 — MGTO1000, 1000M TURN-OFF ENERGY (INDUCTIVE LOAD)

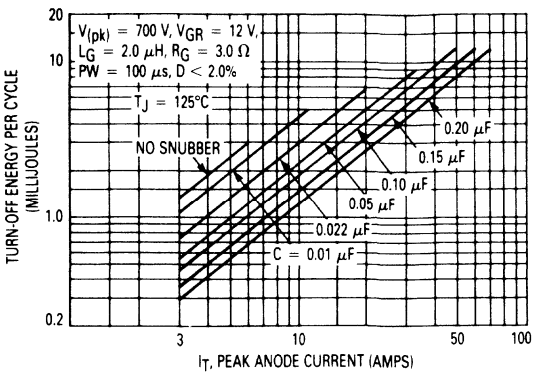


FIGURE 22 — MGTO1200, 1200M, TURN-OFF ENERGY (INDUCTIVE LOAD)

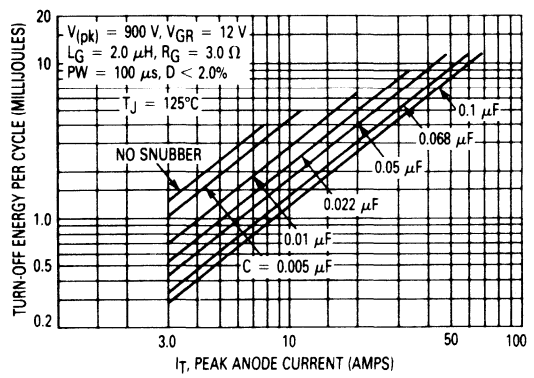
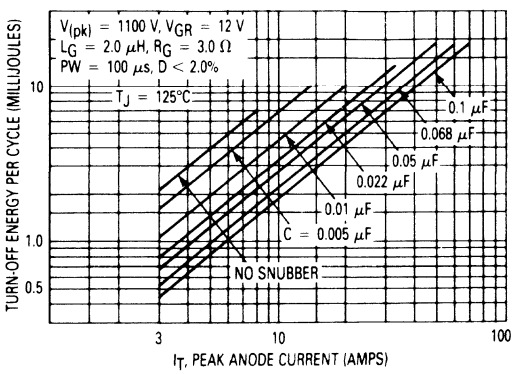


FIGURE 23 — MGTO1400, 1400M, TURN-OFF ENERGY (INDUCTIVE LOAD)



3

Plastic Sidac High Voltage Bilateral Trigger

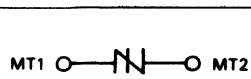
Plastic Sidac High Voltage Bilateral Trigger — High Voltage Triggers

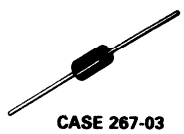
MK1V115
MK1V125
MK1V135

SIDACs
1 AMPERE RMS
104 thru 135 VOLTS

. . . designed for direct interface with the ac power line. Upon reaching the breakover voltage in each direction, the device switches from a blocking state to a low voltage on-state. Conduction will continue like an SCR until the main terminal current drops below the holding current. The plastic axial lead package provides high pulse current capability at low cost. Glass passivation insures reliable operation. Applications are:

- High Pressure Sodium Vapor Lighting
- Strobes and Flashers
- Ignitors
- High Voltage Regulators
- Line Transient Clippers
- Pulse Generators





CASE 267-03
SURMETIC 50
PLASTIC AXIAL
STYLE 1

3

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Repetitive Breakover Voltage	$V_{(BO)}$			Volts
MK1V-115		104	115	
MK1V-125		110	125	
MK1V-135		120	135	
Off-State Repetitive Voltage	V_{DRM}	—	±90	Volts
On-State RMS Current (All Conduction Angles)	$I_{T(RMS)}$	—	1	Amp
On-State Surge Current (Nonrepetitive) (60 Hz One Cycle Sine Wave, Peak Value)	I_{TSM}	—	20	Amps
Operating Junction Temperature Range	T_J	−40	+125	°C
Storage Temperature Range	T_{stg}	−40	+150	°C
Lead Solder Temperature (Lead Length ≥ 1/16" from case, 10 s Max)	—	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	15	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	—	45	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; both directions.)

Characteristic	Symbol	Min	Typ	Max	Unit
Breakover Current (60 Hz Sine Wave)	$I_{(BO)}$	—	—	200	μA
Repetitive Peak Off-State Current (60 Hz Sine Wave, V = V_{DRM})	I_{DRM}	—	—	10	μA
Repetitive Peak On-State Current (T_C = 25°C, Pulse Width = 10 μs, Repetition Frequency, f = 1 kHz)	I_{TRM}	—	20	—	Amps
Forward "On" Voltage (I_{TM} = 1 A peak)	V_{TM}	—	1.1	1.5	Volts
Dynamic Holding Current (60 Hz Sine Wave, R_S = 0.1 kΩ)	I_H	—	—	100	mA
Switching Resistance	R_S	0.1	—	—	kΩ
Maximum Rate of Change of On-State Current	di/dt	—	50	—	A/μs

CURRENT DERATING

FIGURE 1 — MAXIMUM CASE TEMPERATURE

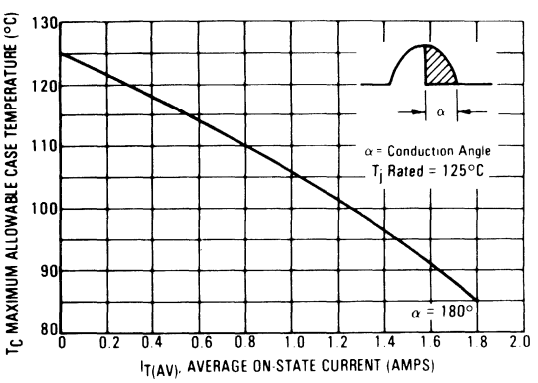


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE

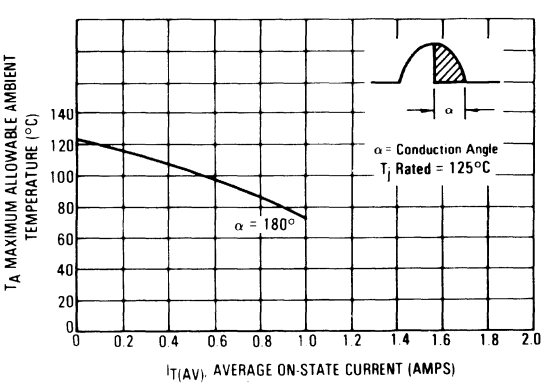


FIGURE 3 — TYPICAL FORWARD VOLTAGE

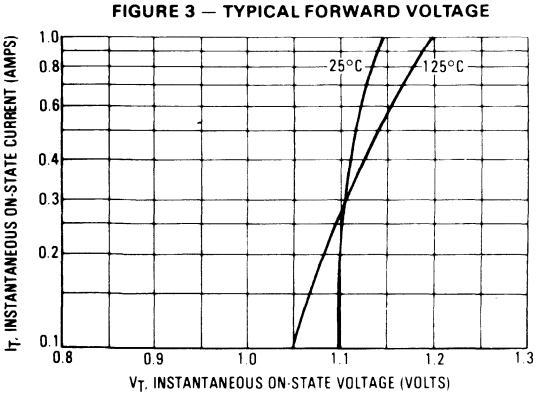
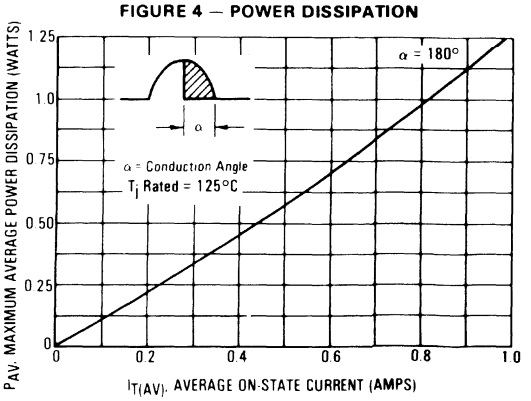
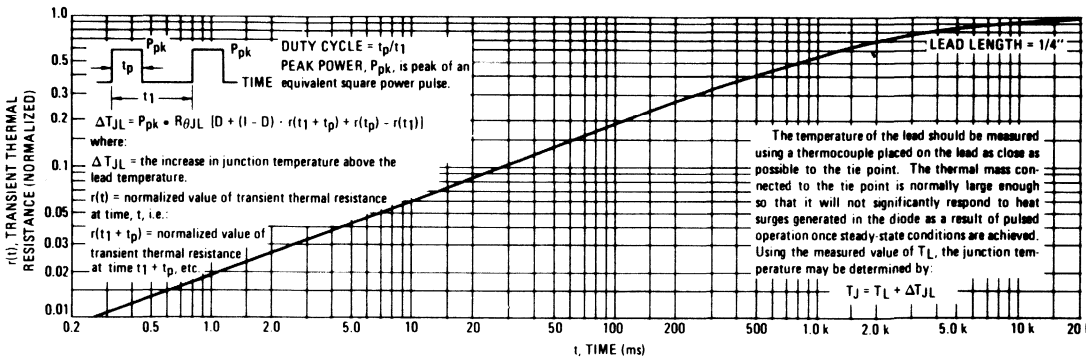


FIGURE 4 — POWER DISSIPATION



THERMAL CHARACTERISTICS

FIGURE 5 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 — BREAKOVER CURRENT

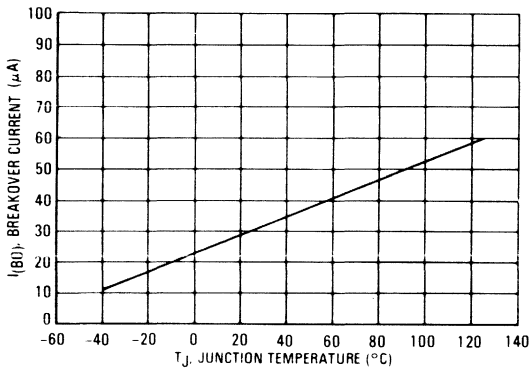


FIGURE 7 — HOLDING CURRENT

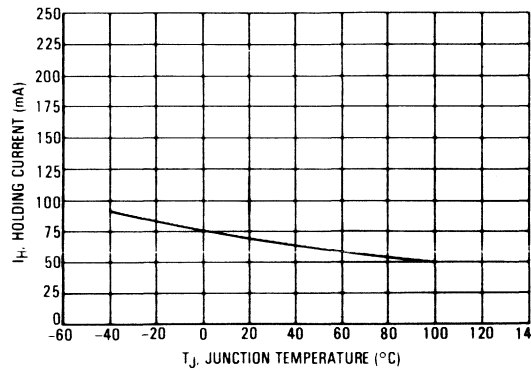
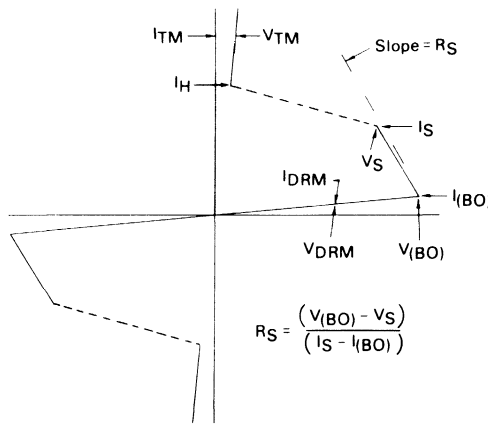


FIGURE 8 — V-1 CHARACTERISTICS



Plastic Sidac High Voltage Bilateral Trigger

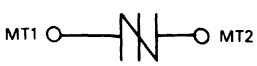
Plastic Sidac High Voltage Bilateral Trigger — High Voltage Triggers

MK1V240
MK1V260
MK1V270

SIDACs
1 AMPERE RMS
240 thru 270 VOLTS

. . . designed for direct interface with the ac power line. Upon reaching the breakover voltage in each direction, the device switches from a blocking state to a low voltage on-state. Conduction will continue like an SCR until the main terminal current drops below the holding current. The plastic axial lead package provides high pulse current capability at low cost. Glass passivation insures reliable operation. Applications are:

- High Pressure Sodium Vapor Lighting
- Strobes and Flashers
- Ignitors
- High Voltage Regulators
- Pulse Generators



CASE 267-03
SURMETIC 50
PLASTIC AXIAL
Polarity denoted by cathode band

3

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Off-State Repetitive Voltage	V_{DRM}	—	±180	Volts
On-State Current RMS (T_L = 100°C, LL = 3/8", 60 Hz Sine Wave Conduction Angle = 180°)	$I_{T(RMS)}$	—	1	Amp
On-State Surge Current (Nonrepetitive) (60 Hz One Cycle Sine Wave, Peak Value)	I_{TSM}	—	20	Amps
Operating Junction Temperature Range	T_J	−40	+125	°C
Storage Temperature Range	T_{stg}	−40	+150	°C
Lead Solder Temperature (Lead Length ≥ 1/16" from Case, 10 s Max)	—	—	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Thermal Resistance, Junction to Lead (LL = 3/8")	$R_{\theta JL}$	—	15	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; both directions.)

Characteristic	Symbol	Min	Typ	Max	Unit
Breakover Voltage	$V_{(BO)}$				Volts
MK1V240		220	—	250	
MK1V260		240	—	270	
MK1V270		250	—	280	
Breakover Current (60 Hz Sine Wave)	$I_{(BO)}$	—	—	200	μA
Repetitive Peak Off-State Current (60 Hz Sine Wave, V = V_{DRM})	I_{DRM}	—	—	10	μA
Forward "On" Voltage (I_{TM} = 1 A peak)	V_{TM}	—	1.1	1.5	Volts
Dynamic Holding Current (60 Hz Sine Wave, R_S = 0.1 kΩ)	I_H	—	—	100	mA
Switching Resistance	R_S	0.1	—	—	kΩ
Maximum Rate of Change of On-State Current	di/dt	—	50	—	A/μs

CURRENT DERATING

FIGURE 1 — MAXIMUM LEAD TEMPERATURE

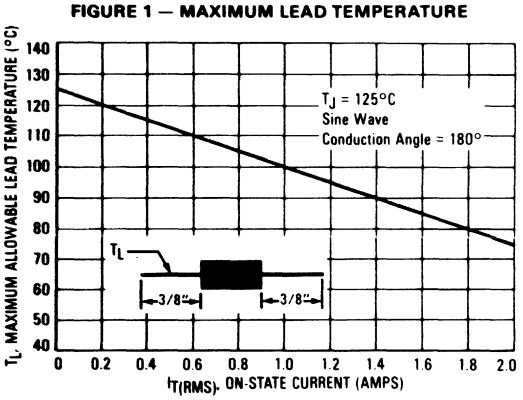


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE

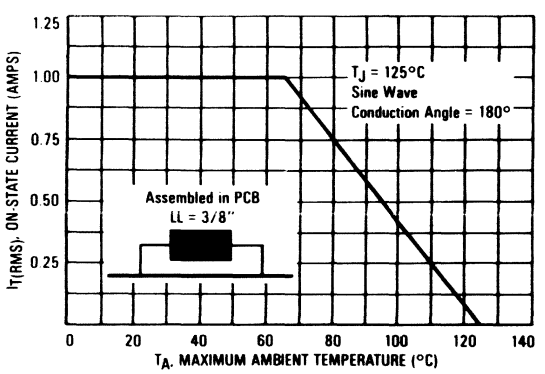


FIGURE 3 — TYPICAL ON-STATE VOLTAGE

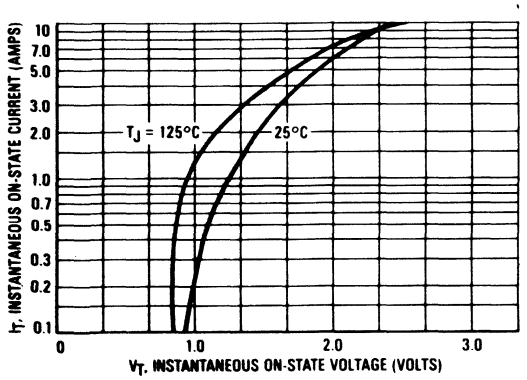
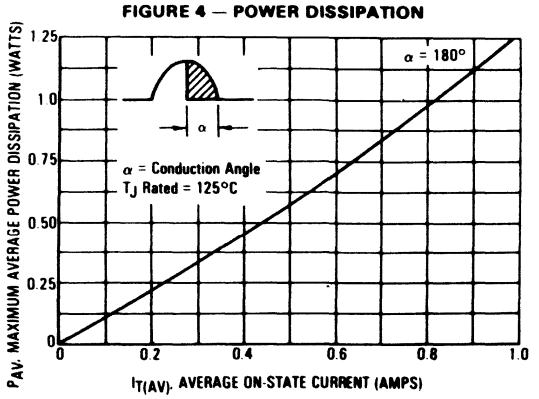


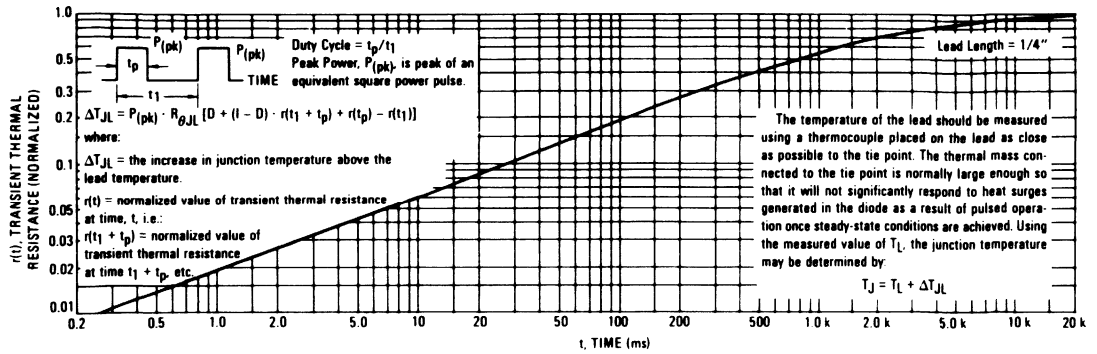
FIGURE 4 — POWER DISSIPATION



3

THERMAL CHARACTERISTICS

FIGURE 5 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 — BREAKOVER VOLTAGE

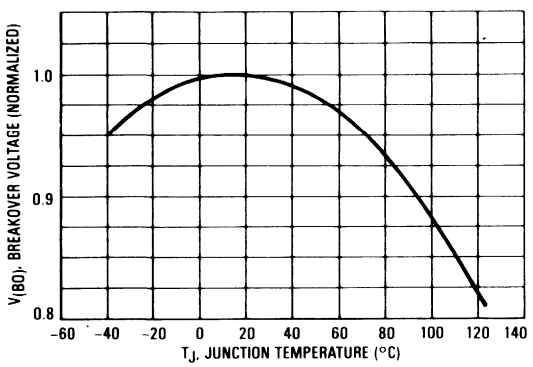


FIGURE 7 — HOLDING CURRENT

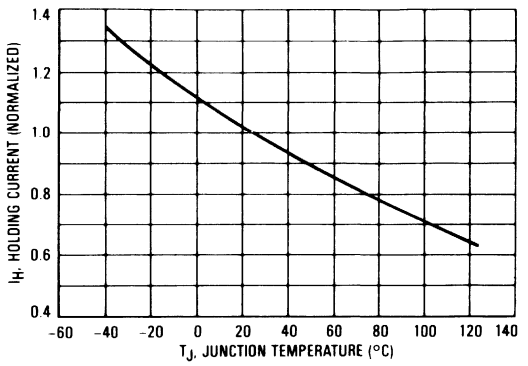


FIGURE 8 — PULSE RATING CURVE

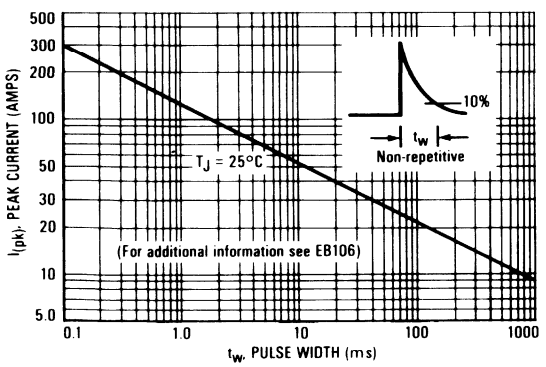
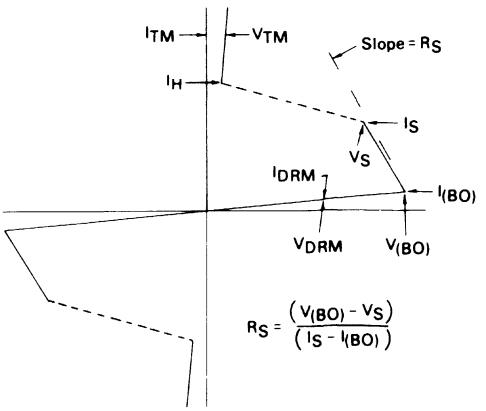


FIGURE 9 — V-1 CHARACTERISTICS



Plastic Sidac High Voltage Bilateral Trigger

Plastic Sidac High Voltage Bilateral Trigger — High Voltage Triggers

MKP9V120
MKP9V130
MKP9V240
MKP9V260
MKP9V270

SIDACs
0.9 AMPERES RMS
120 thru 270 VOLTS

. . . designed for direct interface with the ac power line. Upon reaching the breakover voltage in each direction, the device switches from a blocking state to a low voltage on-state. Conduction will continue like an SCR until the main terminal current drops below the holding current. The plastic axial lead package provides high pulse current capability at low cost. Glass passivation insures reliable operation. Applications are:

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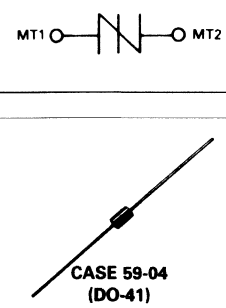
- Strobes and Flashers
- Ignitors
- High Voltage Regulators
- Pulse Generators



CASE 59-04
(DO-41)
STYLE 1
Polarity denoted by cathode band

3

MAXIMUM RATINGS

Rating	Symbol	MKP9V120 MKP9V130	MKP9V240 MKP9V260 MKP9V270	Unit
Off-State Repetitive Voltage	V_{DRM}	±90	±180	Volts
On-State Current RMS (T_L = 80°C, LL = 3/8", conduction angle = 180°, 60 Hz Sine Wave)	$I_{T(RMS)}$	0.9		Amp
On-State Surge Current (Nonrepetitive) (60 Hz One Cycle Sine Wave, Peak Value)	I_{TSM}	4		Amps
Operating Junction Temperature Range	T_J	−40 to +125		°C
Storage Temperature Range	T_{stg}	−40 to +150		°C
Lead Solder Temperature (Lead Length ≥ 1/16" from case, 10 s max)	—	230		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Unit	
Thermal Resistance, Junction to Lead LL = 3/8"	$R_{\theta JL}$	40	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; both directions.)

Characteristic		Symbol	Min	Typ	Max	Unit
Breakover Voltage		V_{BO}				Volts
	MKP9V120		110	—	125	
	MKP9V130		120	—	135	
	MKP9V240		220	—	250	
	MKP9V260		240	—	270	
	MKP9V270		250	—	280	
Repetitive Peak Off-State Current (60 Hz Sine Wave, V = V_{DRM})		I_{DRM}	—	—	5	μA
	T_J = 125°C		—	—	50	
Forward "On" Voltage (I_T = 1 A)		V_{TH}	—	1.3	1.5	Volts
Dynamic Holding Current (60 Hz Sine Wave)		I_H	—	—	100	mA
Switching Resistance		R_S	0.1	—	—	kΩ
Breakover Current (60 Hz Sine Wave)		I_{BO}			200	μA
Maximum Rate of Change of On-State Current	MKP9V120, 130	di/dt	—	90	—	A/μs
	MKP9V240, 260, 270		—	50	—	

FIGURE 1 — MAXIMUM LEAD TEMPERATURE

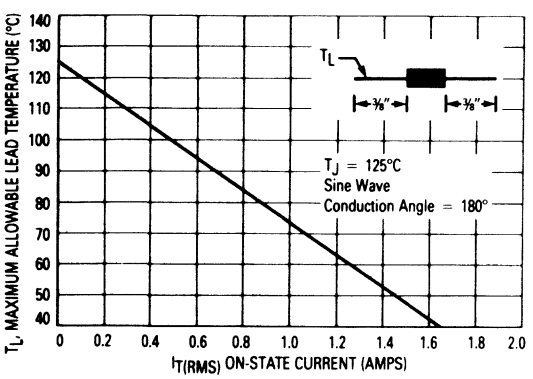


FIGURE 2 — MAXIMUM AMBIENT TEMPERATURE

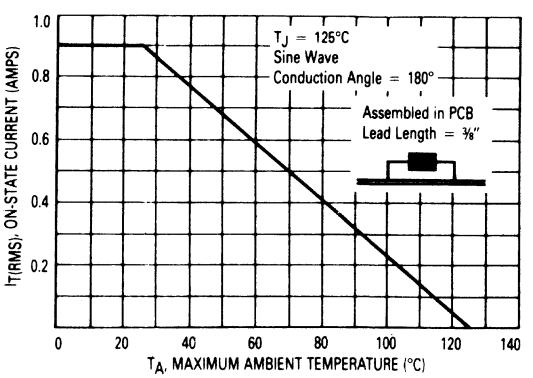


FIGURE 3 — TYPICAL ON-STATE VOLTAGE

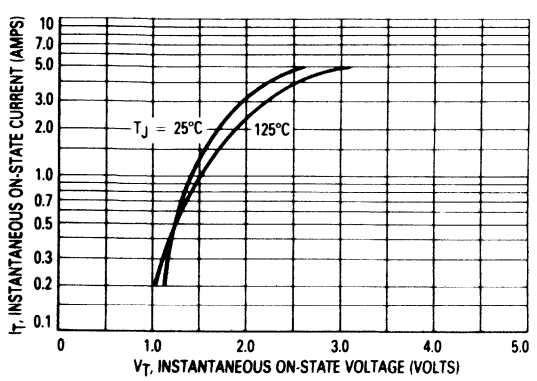
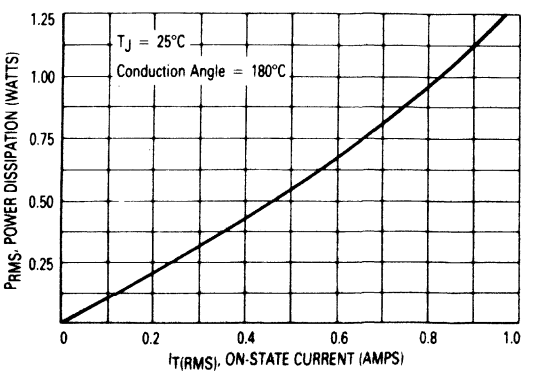
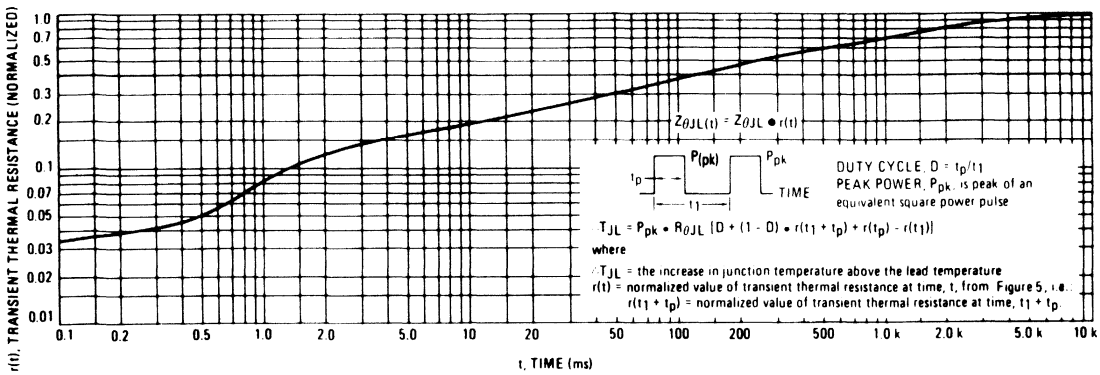


FIGURE 4 — POWER DISSIPATION



THERMAL CHARACTERISTICS

FIGURE 5 — THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 — BREAKOVER VOLTAGE

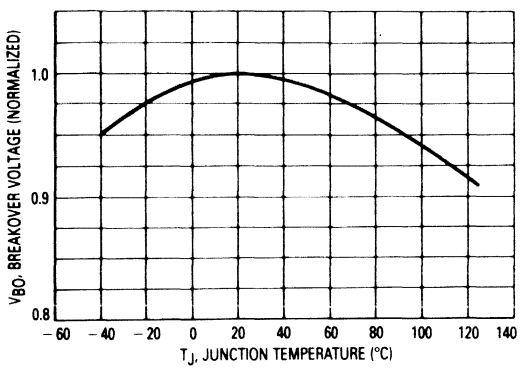


FIGURE 7 — HOLDING CURRENT

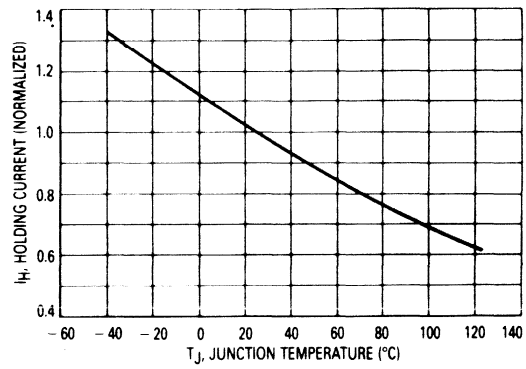


FIGURE 8 — PULSE RATING CURVE

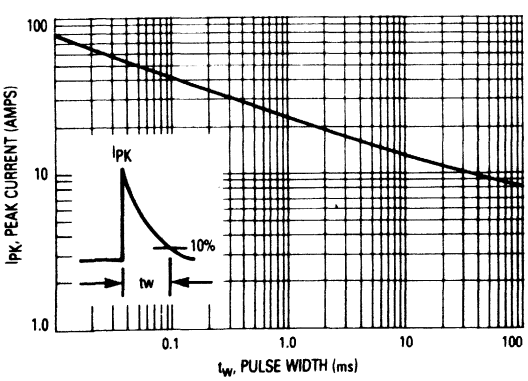
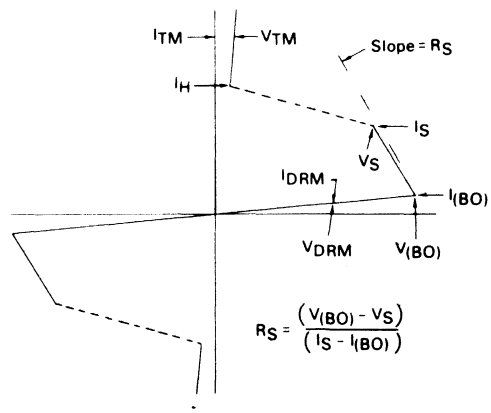


FIGURE 9 — V-I CHARACTERISTICS

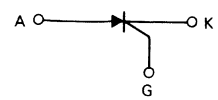


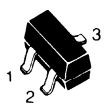
3

Silicon Controlled Rectifiers

MMBS5060
MMBS5061
MMBS5062

SCRs
30 thru 100 VOLTS





CASE 318-02/03
STYLE 14

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Forward Current Avg. (T_C = +67°C)		I_F	510	mA
Peak Forward Gate Voltage		V_{GFM}	5	V
Peak Forward Blocking Voltage RG = 1 k	 MMBS5060 MMBS5061 MMBS5062	V_{FXM}	 30 60 100	V

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board,* T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	556	°C/mW
Total Device Dissipation Alumina Substrate,** T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	417	°C/mW
Junction and Storage Temperature	T_J, T_{stg}	150	°C

*FR-5 = 1 x 0.75 x 0.62 in.
**Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate Trigger Voltage (R_L = 100 Ω, R_{GC} = 1 kΩ, T_C = 125°C)	Anode Voltage = MMBS5060 = 30 V MMBS5061 = 60 V MMBS5062 = 100 V	V_{GNT}	0.1	—	V
Peak Forward Blocking Current (R_{GC} = 1 kΩ, T_C = 125°C)	V_{FXM} = MMBS5060 = 30 V MMBS5061 = 60 V MMBS5062 = 100 V	I_{FXM}	—	50	μA
Peak Reverse Blocking Current (R_{GC} = 1 kΩ, T_C = 125°C)	V_{RXM} = MMBS5060 = 30 V MMBS5061 = 60 V MMBS5062 = 100 V	I_{RXM}	—	50	μA
Forward Voltage* (I_F = 1.2 A Peak)		V_F	—	1.7	V
Gate Trigger Current** (R_{GC} = 1 kΩ, V_{AC} = 7 V, R_L = 100 Ω)		I_{GT}	—	200	μA
Gate Trigger Voltage (R_{GC} = 1 kΩ, V_{AC} = 7 V, R_L = 100 Ω)		V_{GT}	—	0.8	V
Holding Current (V_{AC} = 7 V, R_{GC} = 1 kΩ)		I_H	—	5	mA

*PW ≤ 1 ms, D.C. ≤ 1%.
**RGC current not included in measurement.

6-Pin DIP Optoisolators
Triac Driver Output

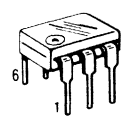
MOC3041
MOC3042
MOC3043

6-PIN DIP OPTOISOLATORS TRIAC DRIVER OUTPUT 400 VOLTS

These devices consist of gallium arsenide infrared emitting diodes optically coupled to a monolithic silicon detector performing the function of a Zero Voltage Crossing bilateral triac driver.

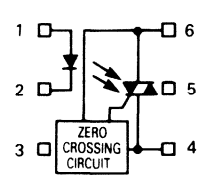
They are designed for use with a triac in the interface of logic systems to equipment powered from 240 Vac lines, such as solid-state relays, industrial controls, motors, solenoids and consumer appliances, etc.

- Simplifies Logic Control of 240 Vac Power
- Zero Voltage Crossing
- High Breakdown Voltage: V_{DRM} = 400 V Min
- High Isolation Voltage: V_{ISO} = 7500 V Guaranteed
- Small, Economical, 6-Pin DIP Package
- dv/dt of 2000 V/μs Typ, 1000 V/μs Guaranteed
- UL Recognized, File No. E54915
- VDE approved per standard 0883/6.80 (Certificate number 41853), with additional approval to DIN IEC380/VDE0806, IEC435/VDE0805, IEC65/VDE0860, VDE0110b, covering all other standards with equal or less stringent requirements, including IEC204/VDE0113, VDE0160, VDE0832, VDE0833, etc. 883
- Special lead form available (add suffix "T" to part number) which satisfies VDE0883/6.80 requirement for 8 mm minimum creepage distance between input and output solder pads.
- Various lead form options available. Consult "Optoisolator Lead Form Options" data sheet for details.



CASE 730A-02
PLASTIC
STYLE 6

COUPLER SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE DO NOT CONNECT
6. MAIN TERMINAL

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE			
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Output Driver Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT DRIVER			
Off-State Output Terminal Voltage	V_{DRM}	400	Volts
Peak Repetitive Surge Current (PW = 100 μs, 120 pps)	I_{TSM}	1	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C
Junction Temperature Range	T_J	−40 to +100	°C
Ambient Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Soldering Temperature (10 s)	—	260	°C

(1) Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT LED					
Reverse Leakage Current (V_R = 6 V)	I_R	—	0.05	100	μA
Forward Voltage (I_F = 30 mA)	V_F	—	1.3	1.5	Volts
OUTPUT DETECTOR (I_F = 0 unless otherwise noted)					
Leakage with LED Off, Either Direction (Rated V_{DRM}, Note 1)	I_{DRM1}	—	2	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)	V_{TM}	—	1.8	3	Volts
Critical Rate of Rise of Off-State Voltage (Note 3)	dv/dt	1000	2000	—	V/μs
COUPLED					
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3 V, Note 2)	I_{FT}				mA
MOC3041		—	—	15	
MOC3042		—	—	10	
MOC3043		—	—	5	
Holding Current, Either Direction	I_H	—	100	—	μA
Isolation Voltage (f = 60 Hz, t = 1 sec)	V_{ISO}	7500	—	—	Vac(pk)
ZERO CROSSING					
Inhibit Voltage (I_F = Rated I_{FT}, MT1-MT2 Voltage above which device will not trigger.)	V_{IH}	—	5	20	Volts
Leakage in Inhibited State (I_F = Rated I_{FT}, Rated V_{DRM}, Off State)	I_{DRM2}	—	—	500	μA

3

Notes: 1. Test voltage must be applied within dv/dt rating.
2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (15 mA for MOC3041, 10 mA for MOC3042, 5 mA for MOC3043) and absolute max I_F (60 mA).
3. This is static dv/dt. See Figure 7 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.

TYPICAL ELECTRICAL CHARACTERISTICS

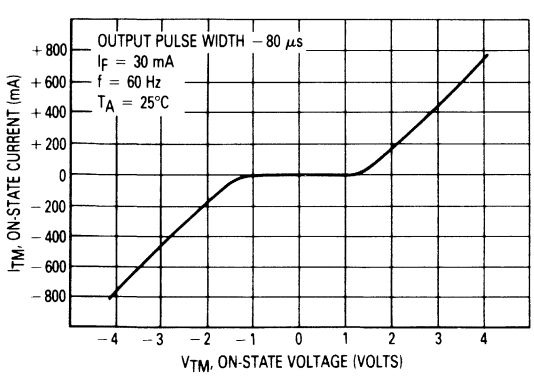


Figure 1. On-State Characteristics

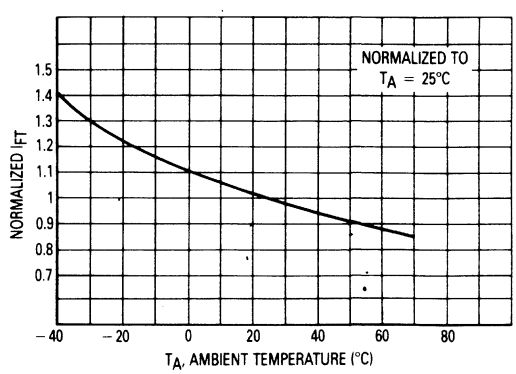


Figure 2. Trigger Current versus Temperature

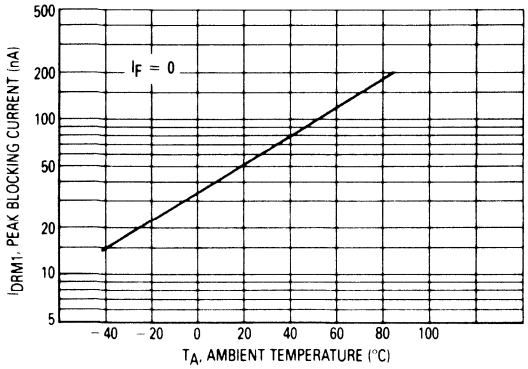


Figure 3. I_{DRM1}, Peak Blocking Current versus Temperature

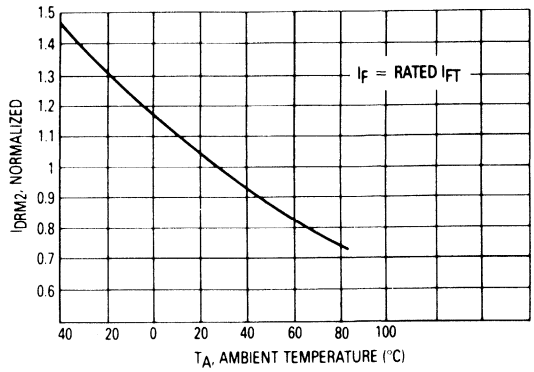


Figure 4. I_{DRM2}, Leakage in Inhibit State versus Temperature

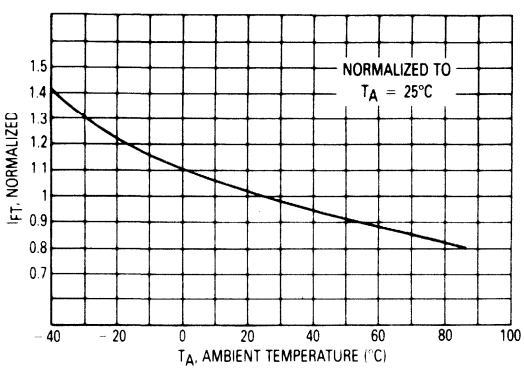


Figure 5. Trigger Current versus Temperature

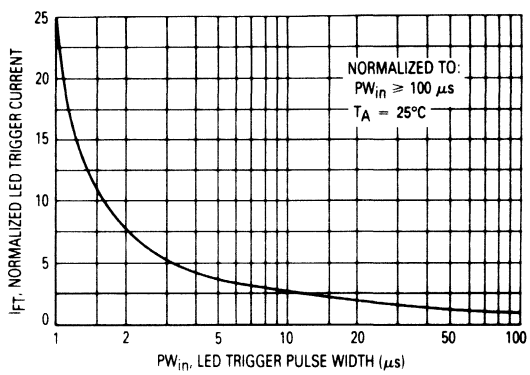
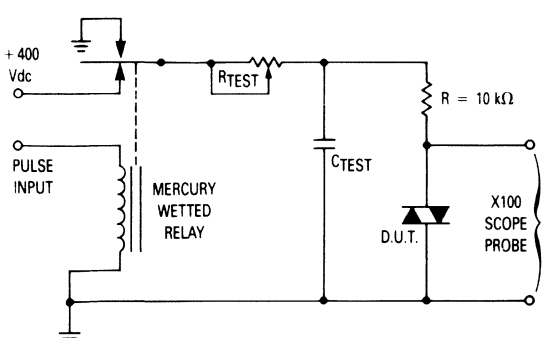
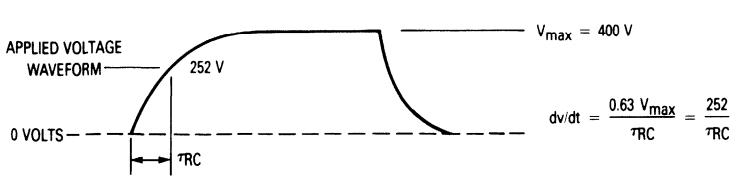


Figure 6. LED Current Required to Trigger versus LED Pulse Width

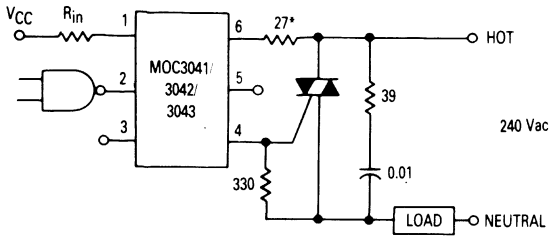


1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.



$$dv/dt = \frac{0.63\ V_{max}}{\tau_{RC}} = \frac{252}{\tau_{RC}}$$

Figure 7. Static dv/dt Test Circuit

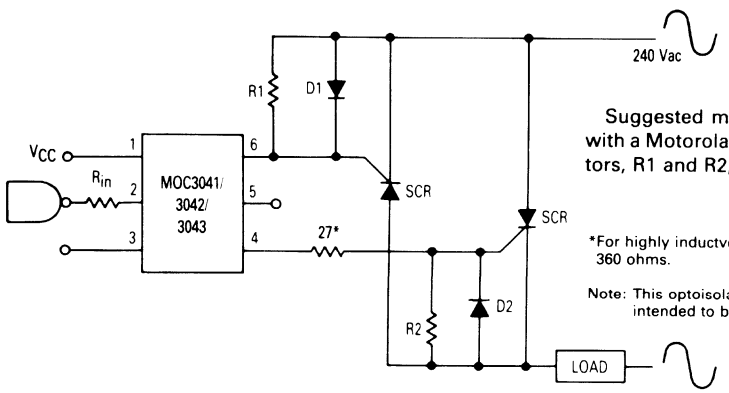


*For highly inductive loads (power factor < 0.5), change this value to 360 ohms.

Typical circuit for use when hot line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 5 mA for the MOC3043, 10 mA for the MOC3042, or 15 mA for the MOC3041. The 39 ohm resistor and 0.01 μF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.

Figure 8. Hot-Line Switching Application Circuit



Suggested method of firing two, back-to-back SCR's, with a Motorola triac driver. Diodes can be 1N4001; resistors, R1 and R2, are optional 330 ohms.

*For highly inductve loads (power factor < 0.5), change this value to 360 ohms.

Note: This optoisolator should not be used to drive a load directly. It is intended to be a trigger device only.

Figure 9. Inverse-Parallel SCR Driver Circuit

3

6-Pin DIP Optoisolators
Triac Driver Output

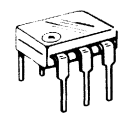
MOC3061
MOC3062
MOC3063

6-PIN DIP OPTOISOLATORS TRIAC DRIVER OUTPUT 600 VOLTS

These devices consist of gallium arsenide infrared emitting diodes optically coupled to monolithic silicon detectors performing the functions of Zero Voltage Crossing bilateral triac drivers.

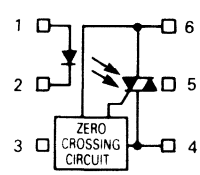
They are designed for use with a triac in the interface of logic systems to equipment powered from 240 Vac lines, such as solid-state relays, industrial controls, motors, solenoids and consumer appliances, etc.

- Simplifies Logic Control of 240 Vac Power
- Zero Voltage Crossing
- High Breakdown Voltage: V_{DRM} = 600 V Min
- High Isolation Voltage: V_{ISO} = 7500 V Min
- Small, Economical, 6-Pin DIP Package
- Same Pin Configuration as MOC3041 Series
- UL Recognized, File No. E54915
- dv/dt of 1500 V/μs Typ, 600 V/μs Guaranteed
- VDE approved per standard 0883/6.80 (Certificate number 41853), with additional approval to DIN IEC380/VDE0806, IEC435/VDE0805, IEC65/VDE0860, VDE0110b, covering all other standards with equal or less stringent requirements, including IEC204/VDE0113, VDE0160, VDE0832, VDE0833, etc. 883
- Special lead form available (add suffix "T" to part number) which satisfies VDE0883/6.80 requirement for 8 mm minimum creepage distance between input and output solder pads.
- Various lead form options available. Consult "Optoisolator Lead Form Options" data sheet for details.



CASE 730A-02
PLASTIC
STYLE 6

COUPLER SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE DO NOT CONNECT
6. MAIN TERMINAL

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE			
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Output Driver Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT DRIVER			
Off-State Output Terminal Voltage	V_{DRM}	600	Volts
Peak Repetitive Surge Current (PW = 100 μs, 120 pps)	I_{TSM}	1	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C
Junction Temperature Range	T_J	−40 to +100	°C
Ambient Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Soldering Temperature (10 s)	—	260	°C

(1) Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT LED					
Reverse Leakage Current (V_R = 6 V)	I_R	—	0.05	100	μA
Forward Voltage (I_F = 30 mA)	V_F	—	1.3	1.5	Volts
OUTPUT DETECTOR (I_F = 0)					
Leakage with LED Off, Either Direction (Rated V_{DRM}, Note 1)	I_{DRM1}	—	60	500	nA
Critical Rate of Rise of Off-State Voltage (Note 3)	dv/dt	600	1500	—	V/μs
COUPLED					
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3 V, Note 2)	I_{FT}				mA
MOC3061		—	—	15	
MOC3062		—	—	10	
MOC3063		—	—	5	
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA, I_F = Rated I_{FT})	V_{TM}	—	1.8	3	Volts
Holding Current, Either Direction	I_H	—	100	—	μA
Inhibit Voltage (MT1-MT2 Voltage above which device will not trigger.) (I_F = Rated I_{FT})	V_{INH}	—	5	20	Volts
Leakage in Inhibited State (I_F = Rated I_{FT}, Rated V_{DRM}, Off State)	I_{DRM2}	—	—	500	μA
Isolation Voltage (f = 60 Hz, t = 1 sec)	V_{ISO}	7500	—	—	Vac(pk)

Notes: 1. Test voltage must be applied within dv/dt rating.
2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (15 mA for MOC3061, 10 mA for MOC3062, 5 mA for MOC3063) and absolute max I_F (60 mA).
3. This is static dv/dt. See Figure 7 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.

3

TYPICAL CHARACTERISTICS

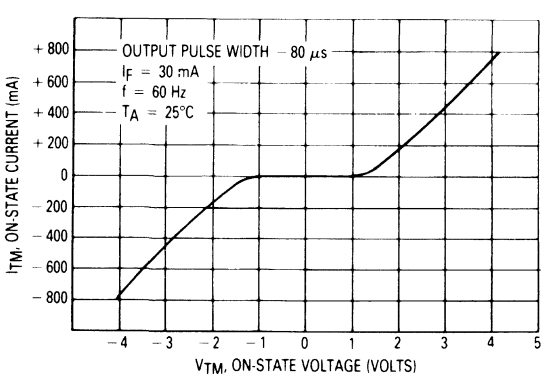


Figure 1. On-State Characteristics

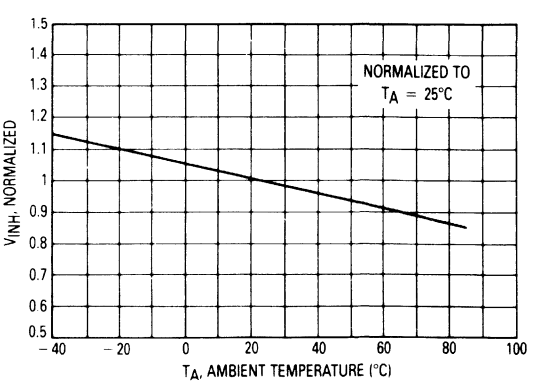


Figure 2. Inhibit Voltage versus Temperature

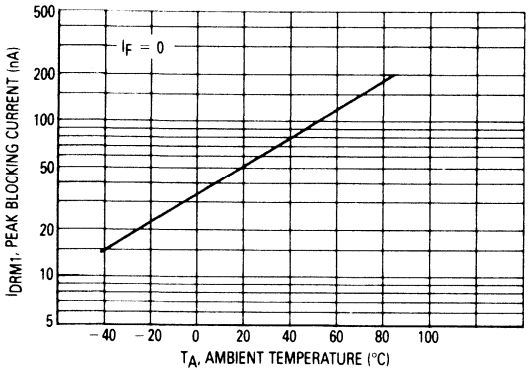


Figure 3. Leakage with LED Off versus Temperature

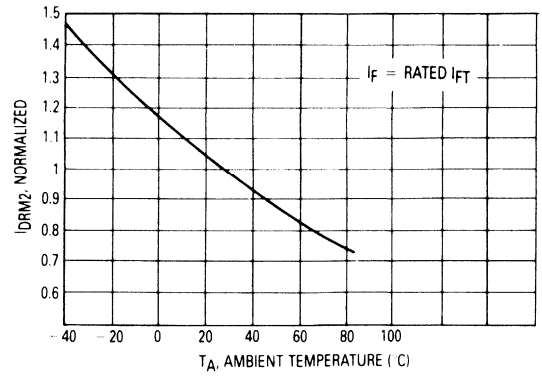


Figure 4. I_{DRM2}, Leakage in Inhibit State versus Temperature

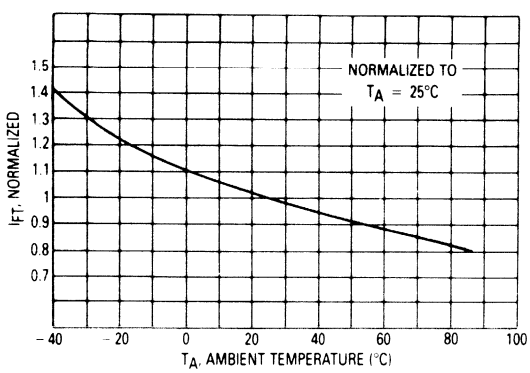


Figure 5. Trigger Current versus Temperature

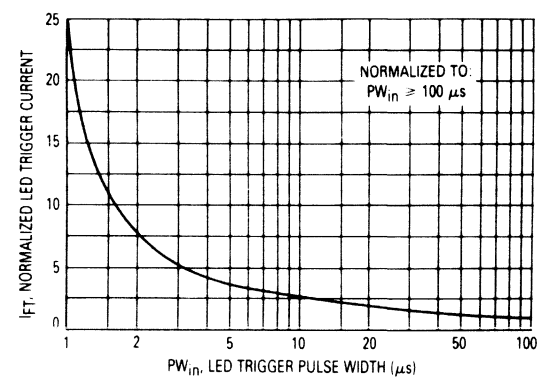
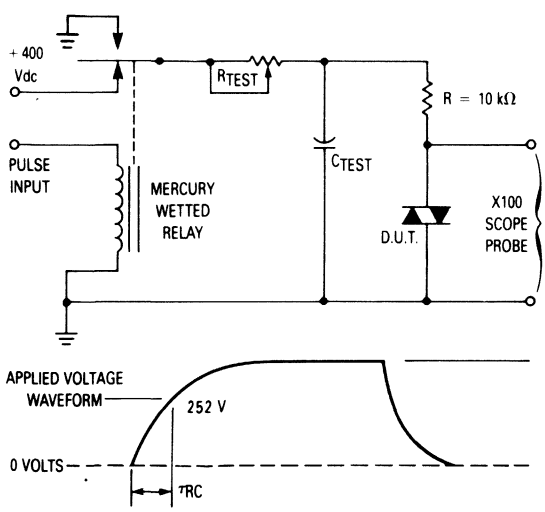


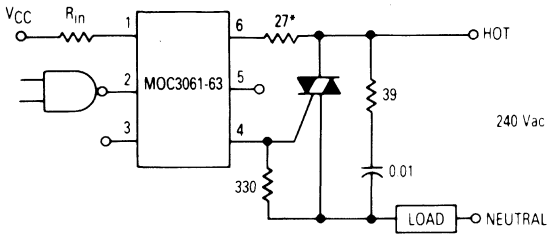
Figure 6. LED Current Required to Trigger versus LED Pulse Width



$$dv/dt = \frac{0.63\ V_{max}}{\tau_{RC}} = \frac{378}{\tau_{RC}}$$

1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

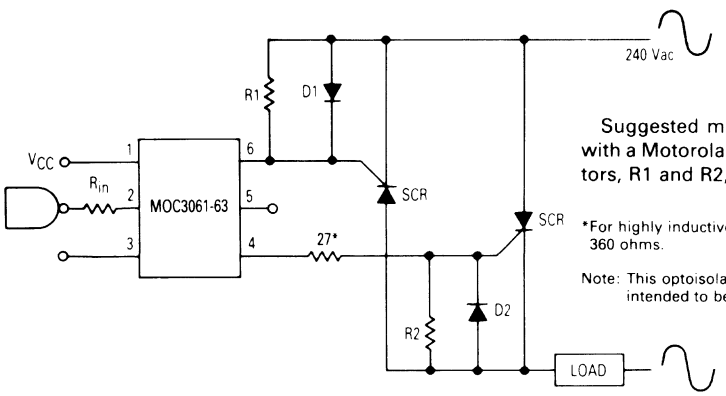
Figure 7. Static dv/dt Test Circuit



Typical circuit for use when hot line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 15 mA for the MOC3061, 10 mA for the MOC3062, and 5 mA for the MOC3063. The 39 ohm resistor and 0.01 μF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.

Figure 8. Hot-Line Switching Application Circuit



Suggested method of firing two, back-to-back SCR's, with a Motorola triac driver. Diodes can be 1N4001; resistors, R1 and R2, are optional 330 ohms.

*For highly inductive loads (power factor <. 0.5), change this value to 360 ohms.

Note: This optoisolator should not be used to drive a load directly. It is intended to be a trigger device only.

Figure 9. Inverse-Parallel SCR Driver Circuit

3

6-Pin DIP Optoisolators
Triac Driver Output

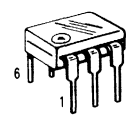
MOC3081
MOC3082
MOC3083

OPTOISOLATORS
ZERO CROSSING
TRIAC DRIVERS
800 VOLTS

These devices consist of gallium arsenide infrared emitting diodes optically coupled to monolithic silicon detectors performing the functions of Zero Voltage Crossing bilateral triac drivers.

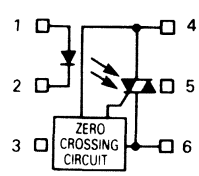
They are designed for use with a triac in the interface of logic systems to equipment powered from 240 Vac lines, such as solid-state relays, industrial controls, motors, solenoids and consumer appliances, etc.

- Simplifies Logic Control of 240 Vac Power
- Zero Voltage Crossing
- High Breakdown Voltage: V_{DRM} = 800 V Min
- High Isolation Voltage: V_{ISO} = 7500 V Min
- Small, Economical, 6-Pin DIP Package
- Same Pin Configuration as MOC3031/3041/3061 Series
- UL Recognized, File No. E54915
- dv/dt of 1500 V/μs Typ, 600 V/μs Guaranteed
- VDE approved per standard 0883/6.80 (Certificate number 41853), with additional approval to DIN IEC380/VDE0806, IEC435/VDE0805, IEC65/VDE0860, VDE110b, covering all other standards with equal or less stringent requirements, including IEC204/VDE0113, VDE0160, VDE0832, VDE0833, etc. 883
- Special lead form available (add suffix "T" to part number) which satisfies VDE0883/6.80 requirement for 8 mm minimum creepage distance between input and output solder pads
- Various lead form options available. Consult "Optoisolator Lead Form Options" data sheet for details



CASE 730A-02
PLASTIC
STYLE 6

COUPLER SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE DO NOT CONNECT
6. MAIN TERMINAL

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE			
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Output Driver Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT DRIVER			
Off-State Output Terminal Voltage	V_{DRM}	800	Volts
Peak Repetitive Surge Current (PW = 100 μs, 120 pps)	I_{TSM}	1	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage, Note 1 (Peak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C

Note 1. Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

(continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LED CHARACTERISTICS					
Reverse Leakage Current (V_R = 6 V)	I_R	—	0.05	100	μA
Forward Voltage (I_F = 30 mA)	V_F	—	1.3	1.5	Volts
OUTPUT DETECTOR (I_F = 0)					
Leakage with LED Off, Either Direction (V_{DRM} = 800 V, Note 1)	I_{DRM1}	—	80	500	nA
Critical Rate of Rise of Off-State Voltage, Note 3	dv/dt	600	1500	—	V/μs
COUPLED					
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3 V, Note 2)	I_{FT}				mA
MOC3081		—	—	15	
MOC3082		—	—	10	
MOC3083		—	—	5	
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA, I_F = Rated I_{FT})	V_{TM}	—	1.8	3	Volts
Holding Current, Either Direction	I_H	—	100	—	μA
Inhibit Voltage (MT1-MT2 Voltage above which device will not trigger) (I_F = Rated I_{FT})	V_{INH}	—	5	20	Volts
Leakage in Inhibited State (I_F = Rated I_{FT}, V_{DRM} = 800 V, Off State)	I_{DRM2}	—	300	500	μA

Notes: 1. Test voltage must be applied within dv/dt rating.
2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (15 mA for MOC3081, 10 mA for MOC3082, 5 mA for MOC3083) and absolute max I_F (60 mA).
3. This is static dv/dt. See Figure 7 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.

3

TYPICAL CHARACTERISTICS

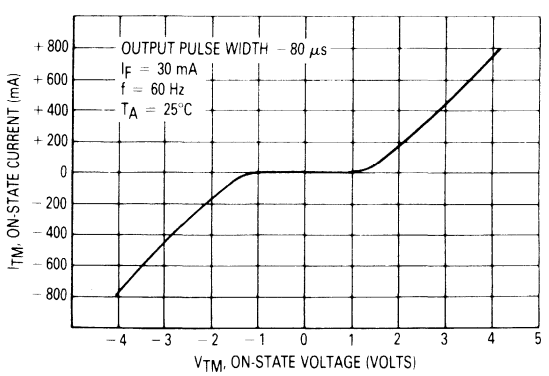


Figure 1. On-State Characteristics

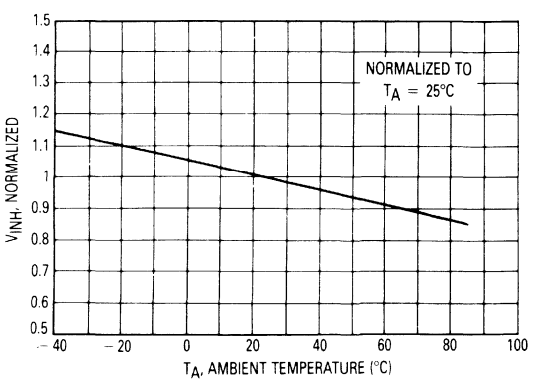


Figure 2. Inhibit Voltage versus Temperature

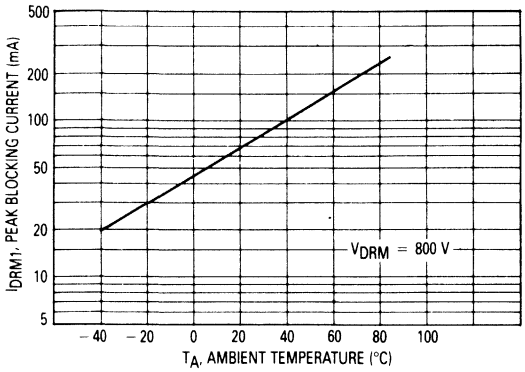


Figure 3. Leakage with LED Off versus Temperature

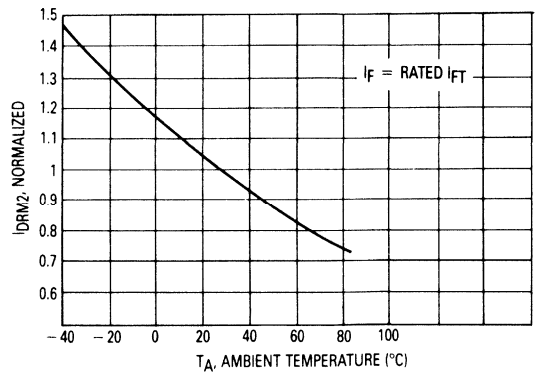


Figure 4. I_{DRM2}, Leakage in Inhibit State versus Temperature

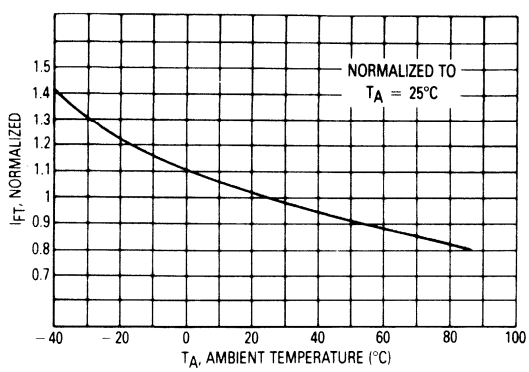


Figure 5. Trigger Current versus Temperature

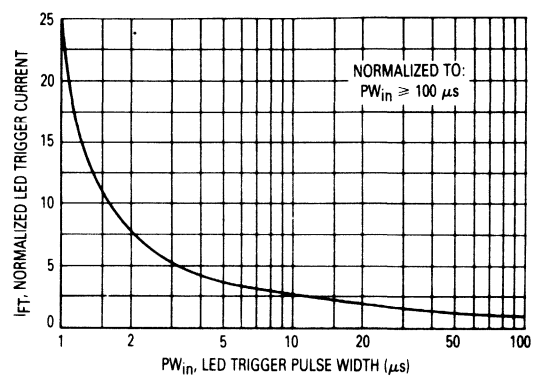
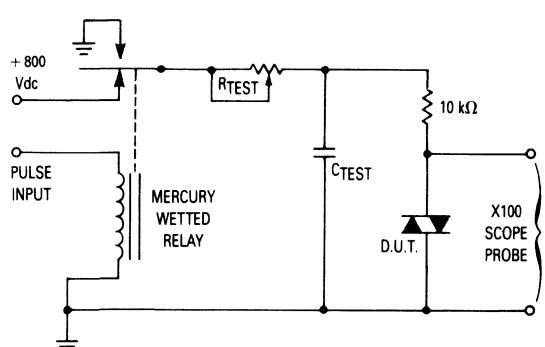


Figure 6. LED Current Required to Trigger versus LED Pulse Width



1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

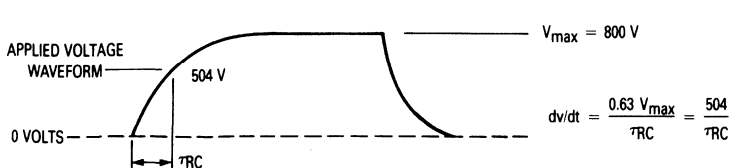
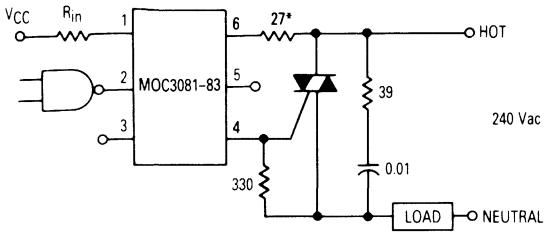


Figure 7. Static dv/dt Test Circuit

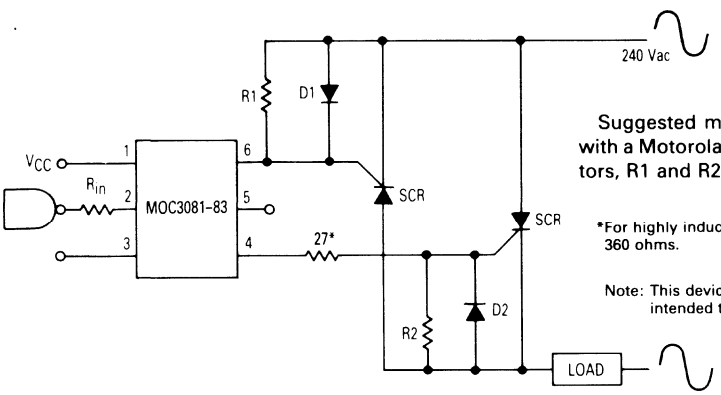


*For highly inductive loads (power factor < 0.5), change this value to 360 ohms.

Typical circuit for use when hot line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 15 mA for the MOC3081, 10 mA for the MOC3082, and 5 mA for the MOC3083. The 39 ohm resistor and 0.01 μF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.

Figure 8. Hot-Line Switching Application Circuit



Suggested method of firing two, back-to-back SCR's, with a Motorola triac driver. Diodes can be 1N4001; resistors, R1 and R2, are optional 330 ohms.

*For highly inductive loads (power factor < 0.5), change this value to 360 ohms.

Note: This device should not be used to drive a load directly. It is intended to be a trigger device only.

3

Figure 9. Inverse-Parallel SCR Driver Circuit

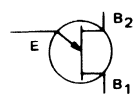
PN Unijunction Transistors

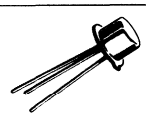
Silicon Annular Unijunction Transistors

. . . designed for economical, general purpose use in pulse, timing, oscillator and thyristor trigger circuits.

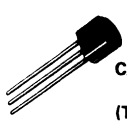
MU10
MU20

PN UJTs





CASE 22A-01
STYLE 1
MU20



CASE 29-04
STYLE 9
(TO-226AA)
MU10

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Power Dissipation, Note 1	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current, Note 2	i_e	1	Amp
Emitter Reverse Voltage	V_{EB2}	30	Volts
Interbase Voltage Based upon Power Dissipation at T_A = 25°C	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Notes: 1. Derate 3 mW/°C increase in ambient temperature.
2. Duty Cycle ≤ 1%, PRR = 10 PPS (See Figure 5).

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (Test Circuit Figure 4), Note 1 (V_{B2B1} = 10 V)	η	0.50	—	0.85	—
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)	r_{BB}	4	—	10	kΩ
Emitter Saturation Voltage, Note 2 (V_{B2B1} = 10 V, I_E = 50 mA)	$V_{EB1(sat)}$	—	2	—	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	—	—	50	mA
Emitter Reverse Current (V_{EB2} = 30 V, I_{B1} = 0)	I_{EB20}	—	—	1	μA
Peak-Point Emitter Current (V_{B2B1} = 25 V)	I_P	—	—	5	μA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 Ohms)	I_V	1	—	—	mA
Base-One Peak Pulse Voltage (Test Circuit Figure 3)	V_{OB1}	3	—	—	Volts

Notes: 1. η, intrinsic standoff ratio, is defined in terms of the peak-point voltage, Vp, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.45 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.

2. Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≤ 2% to avoid internal heating, which may result in erroneous readings.

3

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

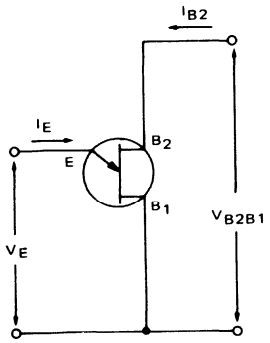


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES

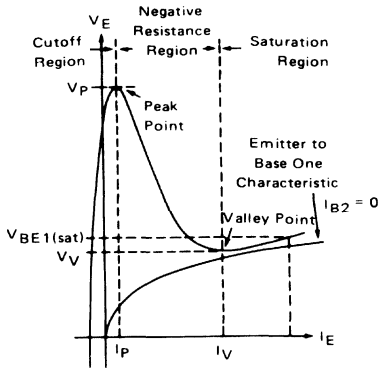


FIGURE 3 – V_{OB1} TEST CIRCUIT

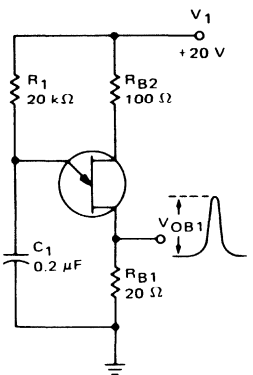
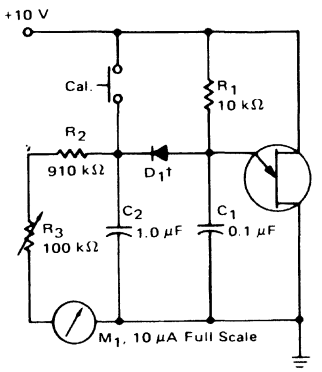
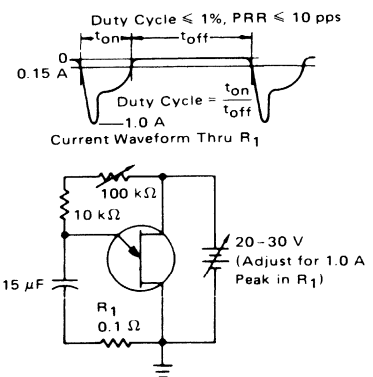


FIGURE 4 – η TEST CIRCUIT



† D_1 diode with the following characteristics:
$V_F = 0.45$ V @ $I_F = 10$ μA
$I_R \leq 2.0$ μA @ $V_R = 20$ V

FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM



PN Unijunction Transistors

Silicon Plastic Unijunction Transistors

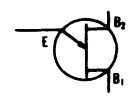
MU4891 thru MU4894

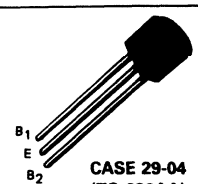
PN UJTs

. . . designed for military and industrial use in pulse, timing, triggering, sensing, and oscillator circuits. The annular process provides low leakage current, fast switching and low peak-point currents as well as outstanding reliability and uniformity.

Recommended usage includes:

- Long-time Delay Circuits — MU4894
- Silicon Controlled Rectifier Triggering Circuits — MU4893
- High-frequency Relaxation-Oscillator Circuits — MU4892
- General-Purpose Unijunction Applications — MU4891





CASE 29-04
(TO-226AA)
STYLE 9

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Power Dissipation, Note 1	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current, Note 2	i_e	1	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Storage Temperature Range	T_{stg}	−65 to +150	°C

Notes: 1. Derate 3 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by external circuitry. Interbase voltage (V_{B2B1}) limited by power dissipation,

$V_{B2B1} = \sqrt{R_{BB} \cdot P_D}$

2. Capacitance discharge current must fall to 0.37 Amp within 3 ms and PRR ≤ 10 PPS.

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V), Note 1	MU4892	η	0.51	—	0.69	—
	MU4891, MU4893		0.55	—	0.82	
	MU4894		0.74	—	0.86	
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)	MU4891, MU4892	R_{BB}	4	7	9.1	k ohms
	MU4893, MU4894		4	7	12	
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = −65°C to +100°C)		αR_{BB}	0.1	—	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA), Note 2		$V_{EB1(sat)}$	—	2.5	4	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	10	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		I_{EB2O}	—	5	10	nA
Peak Point Emitter Current (V_{B2B1} = 25 V)	MU4891	I_P	—	0.6	5	μA
	MU4892, MU4893		—	0.6	2	
	MU4894		—	0.6	1	
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 Ohms), Note 2	MU4891, MU4893, MU4894	I_V	2	4	—	mA
	MU4892		2	3	—	
Base-One Peak Pulse Voltage (Note 3, Figure 3)	MU4891, MU4892, MU4894	V_{OB1}	3	5	—	Volts
	MU4893		6	8	—	

3

Notes:

1. Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop (≈0.5 V @ 10 μA)

2. Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.
3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

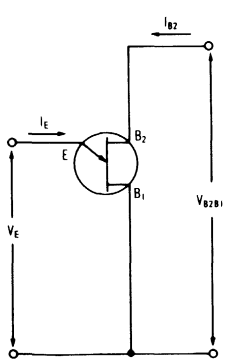


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES

(Exaggerated to Show Details)

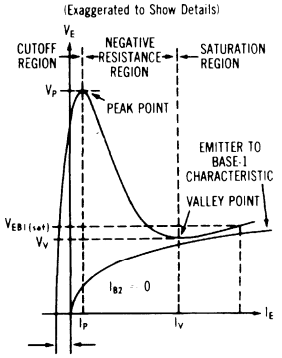
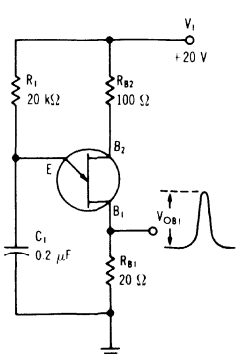


FIGURE 3 — V_{OB1} TEST CIRCUIT

(Typical Relaxation Oscillator)



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SCRs
10 AMPERES RMS
50 thru 800 VOLTS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
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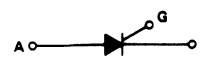
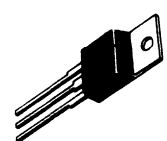




CASE 221A-04
(TO-220AB)
STYLE 3

3

MAXIMUM RATINGS

Rating			Symbol	Value	Unit
Peak Repetitive Reverse Voltage, Note 1 Peak Repetitive Off-State Voltage			V_{RRM} V_{DRM}		Volts
	S2800	F		50	
		A		100	
		B		200	
		D		400	
		M		600	
		N		800	
Non-Repetitive Peak Reverse Voltage Non-Repetitive Off-State Voltage			V_{RSM} V_{DSM}		Volts
	S2800	F		75	
		A		125	
		B		250	
		D		500	
		M		700	
		N		900	
RMS Forward Current (All Conduction Angles)	T_C = 75°C		$I_{T(RMS)}$	10	Amps
Peak Forward Surge Current (1 Cycle, Sine Wave, 60 Hz, T_C = 80°C)			I_{TSM}	100	Amps
Circuit Fusing Considerations (T_J = −65 to +100°C, t = 1 to 8.3 ms)			I^2t	40	A^2s
Forward Peak Gate Power (t ≤ 10 μs)			P_{GM}	16	Watts
Forward Average Gate Power			$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range			T_J	−40 to +100	°C
Storage Temperature Range			T_{stg}	−40 to +150	°C

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}) T_C = 25°C T_C = 100°C	I_{DRM}, I_{RRM}	— —	— —	10 2	μA mA
Instantaneous On-State Voltage (I_{TM} = 30 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_T	—	1.7	2	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 30 Ohms)	I_{GT}	—	8	15	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 30 Ohms)	V_{GT}	—	0.9	1.5	Volts
Holding Current (Gate Open, V_D = 12 Vdc, I_T = 150 mA)	I_H	—	10	20	mA
Gate Controlled Turn-on Time (V_D = Rated V_{DRM}, I_{TM} = 2 A, I_{GR} = 80 mA)	t_{gt}	—	1.6	—	μs
Circuit Commutated Turn-Off Time (V_D = V_{DRM}, I_{TM} = 2 A, Pulse Width = 50 μs, dv/dt = 200 V/μs, di/dt = 10 A/μs, T_C = 75°C)	t_q	—	25	—	μs
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Rise, T_C = 100°C)	dv/dt	—	100	—	V/μs

3

FIGURE 1 – CURRENT DERATING

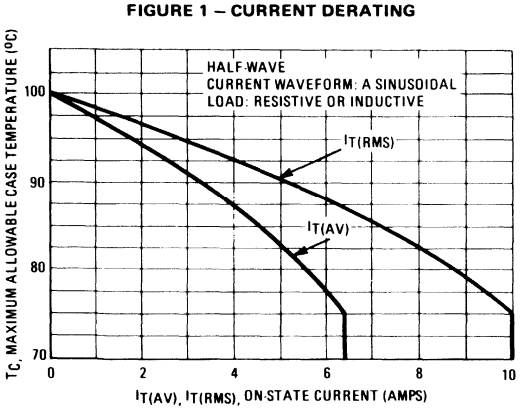
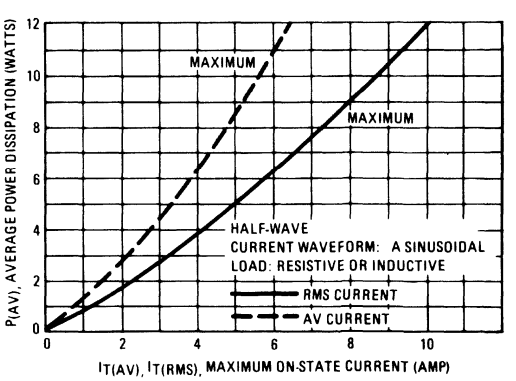


FIGURE 2 – POWER DISSIPATION



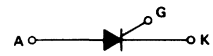
Thyristors
Silicon Controlled Rectifiers

S6200
S6210
S6220
Series

SCRs
20 AMPERES RMS
100 thru 600 VOLTS

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 200 Amps
- Low Forward "On" Voltage — 1.2 V (Typ) @ I_{TM} = 20 Amps
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud or Isolated Stud Package
- Glass Passivated Junctions for Maximum Reliability



CASE 174-04
(TO-203)
STYLE 1
S6200 SERIES

CASE 263-04
STYLE 1
S6210 SERIES

CASE 311-02
STYLE 1
S6220 SERIES

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 Repetitive Peak Reverse Voltage, Note 1 S6200, S6210, S6220 A S6200, S6210, S6220 B S6200, S6210, S6220 D S6200, S6210, S6220 M	V_{DROM} V_{RROM}	 100 200 400 600	Volts
Non-Repetitive Peak Off-State Voltage, Note 1 Non-Repetitive Peak Reverse Voltage, Note 1 S6200, S6210, S6220 A S6200, S6210, S6220 B S6200, S6210, S6220 D S6200, S6210, S6220 M	V_{DSOM} V_{DROM}	 150 250 500 700	Volts
RMS On-State Current (T_C = 75°C)	$I_{T(RMS)}$	20	Amps
Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceded and followed by rated current, T_C = 75°C)	I_{TSM}	200	Amps
Circuit Fusing Considerations (T_J = −65 to +100°C, t = 1 to 8.3 ms)	I^2t	170	A^2s
Peak Gate Power (10 μs Max)	P_{GM}	40	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range	T_J	−65 to +100	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case S6200 S6210, S6220	$R_{\theta JC}$	1.2 1.4	°C/W

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Intantaneous Forward Breakover Voltage (Gate Open, T_C = 100°C)		$V_{(BO)O}$				Volts
S6200, S6210, S6220	A		100	—	—	
S6200, S6210, S6220	B		200	—	—	
S6200, S6210, S6220	D		400	—	—	
S6200, S6210, S6220	M		600	—	—	
Peak Blocking Current (Rated V_{DROM} @ T_C = 100°C)	T_C = 25°C	I_{DOM}	—	—	10	μA
		I_{RROM}	—	—	2	mA
Peak On-State Voltage (I_T = 100 A Peak)		V_T	—	—	2.4	Volts
Gate Trigger Current (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 30 Ohms)		I_{GT}	—	—	15	mA
Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 30 Ohms)		V_{GT}	—	—	2	Volts
Holding Current (Either Direction) (Main Terminal Voltage = 12 Vdc, Gate Open)		I_{HO}	—	—	20	mA
Gate Controlled Turn-On Time (V_D = $V_{(BO)O}$, I_T = 30 A Peak, I_{GT} = 200 mA, Rise Time = 0.1 μs)		t_{gt}	—	2	—	μs
Critical Rate-of-Rise of Off-State Voltage (V_D = $V_{(BO)O}$, Exponential Voltage Rise, Gate Open, T_C = 100°C)		dv/dt				V/μs
S6200, S6210, S6220	A,D		10	100	—	
S6200, S6210, S6220	B		10	150	—	
S6200, S6210, S6220	M		10	75	—	

3

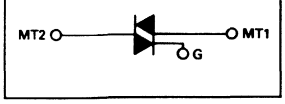
Triacs
Bidirectional Triode Thyristors

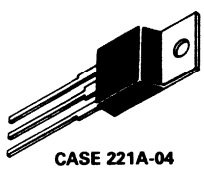
SC141
SC146

TRIACs
6 and 10 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Triggering Specified in Three Quadrants
- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability





CASE 221A-04
(TO-220AB)
STYLE 4

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Gate Open B SC141 D SC146 M N	V_{DRM}	 200 400 600 800	Volts
RMS On-State Current (T_C = 80°C) SC141 SC146	$I_{T(RMS)}$	 6 10	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz) SC141 SC146	I_{TSM}	 80 120	Amps
Circuit Fusing Considerations (t = 8.3 ms) SC141 SC146	I^2t	 26.5 60	A^2s
Peak Gate Power (Pulse Width = 10 μs)	P_{GM}	10	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current (Pulse Width = 10 μs)	I_{GM}	3.5	Amps
Peak Gate Voltage	V_{GM}	10	Volts
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
SC141		2.2	
SC146		1.5	

ELECTRICAL CHARACTERISTICS (T_C = +25°C, Either Polarity of MT2 to MT1 Voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = +100°C		—	—	0.5	mA
Peak On-State Voltage (Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}				Volts
SC141 I_{TM} = 8.5 A Peak		—	—	1.83	
SC146 I_{TM} = 14 A Peak		—	—	1.65	
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Gate Open-Circuited, Exponential Waveform T_C = +100°C	dv/dt	—	50	—	V/μs
Critical Rate-of-Rise of Commutating Off-State Voltage (1) ($I_{T(RMS)}$ = Rated $I_{T(RMS)}$, V_D = Rated V_{DRM}, Gate Open-Circuited T_C = +80°C	dv/dt(c)				V/μs
SC141 Commutating di/dt = 3.2 A/ms		4	—	—	
SC146 Commutating di/dt = 5.4 A/ms		4	—	—	
DC Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, Trigger Mode)	I_{GT}				mAdc
MT2(+), G(+); MT2(−), G(−); R_L = 100 Ohms		—	—	50	
MT2(+), G(−); R_L = 50 Ohms		—	—	50	
MT2(+), G(+); MT2(−), G(−); R_L = 50 Ohms T_C = −40°C		—	—	80	
MT2(+), G(−); R_L = 25 Ohms T_C = −40°C		—	—	80	
DC Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, Trigger Mode)	V_{GT}				Vdc
MT2(+), G(+); MT2(−), G(−); R_L = 100 Ohms		—	—	2.5	
MT2(+), G(−); R_L = 50 Ohms		—	—	2.5	
MT2(+), G(+); MT2(−), G(−); R_L = 50 Ohms T_C = −40°C		—	—	3.5	
MT2(+), G(−); R_L = 25 Ohms T_C = −40°C		—	—	3.5	
(V_D = Rated V_{DRM}; R_L = 1000 Ohms) All Polarities T_C = +100°C		0.2	—	—	
Holding Current (V_D = 24 Vdc, I_T = 0.5 A) (Pulse Width = 1 ms, Duty Cycle ≤ 2%) (Gate Trigger Source = 7 V, 20 Ohms) T_C = +25°C	I_H	—	—	50	mAdc
T_C = −40°C		—	—	100	
Latching Current (V_D = 24 Vdc) (Gate Trigger Source = 15 V, 100 Ohms, Trigger Mode)	I_L				mAdc
MT2(+), G(+); MT2(−), G(−)		—	—	100	
MT2(+), G(−)		—	—	200	
MT2(+), G(+); MT2(−), G(−) T_C = −40°C		—	—	200	
MT2(+), G(−) T_C = −40°C		—	—	400	

3

FIGURE 1 – RMS CURRENT DERATING

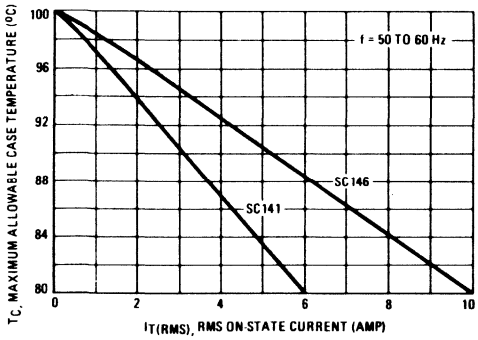
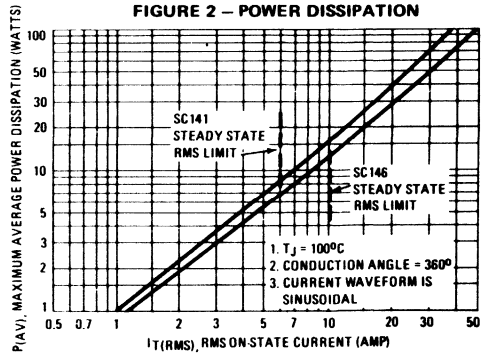


FIGURE 2 – POWER DISSIPATION



3

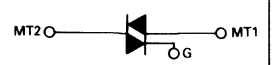
Triacs
Bidirectional Triode Thyristors

SC250
SC250( )3
SC251

TRIACs
15 AMPERES RMS
200 thru 600 VOLTS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 3 Quadrants



MAXIMUM RATINGS

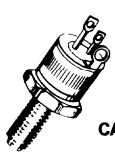
Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage SC251B, SC250B, SC250B3 SC251D, SC250D, SC250D3 SC251M, SC250M, SC250M3 SC251N, SC250N	V_{DRM}	 200 400 600 800	Volts
RMS On-State Current	$I_{T(RMS)}$	15	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amps
Circuit Fusing Considerations t = 1 ms t = 8.3 ms	I^2t	 20 41.5	A^2s
Peak Gate Power	P_{GM}	10	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Power (Pulse Width = 10 μs)	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +115	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case SC250, SC251 SC250( )3	$R_{\theta JC}$	 2 2.3	°C/W

CASE 174-04
(TO-203)
STYLE 3
SC251
PRESS FIT

CASE 175-03
STYLE 3
SC250
STUD



CASE 235-03
STYLE 2
SC250( )3
ISOLATED STUD

3

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted. Values apply for either polarity of Main Terminal 2. Characteristics referenced to Main Terminal 1.)

Characteristic	Symbol	Min.	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = +115°C		—	—	0.5	mA
Peak On-State Voltage (I_{TM} = 21 A, Pulse Width = 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.65	Volts
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Gate Open-Circuited, Exponential Waveform) T_C = +115°C	dv/dt	100	—	—	V/μs
Critical Rate-of-Rise of Commutating Off-State Voltage, Note 1 ($I_{T(RMS)}$ = Rated RMS On-State Current, V_D = V_{DRM}) (Gate Open-Circuited, Commutating di/dt = 8 A/ms)	dv/dt(c)				V/μs
SC250, SC251 T_C = +84°C		4	—	—	
SC250( )3 T_C = +78°C		4	—	—	
DC Gate Trigger Current (Continuous dc) (V_D = 12 Vdc)	I_{GT}				mAdc
MT2(+), G(+); MT2(−), G(−); R_L = 100 Ohms		—	—	50	
MT2(+), G(−); R_L = 50 Ohms		—	—	50	
DC Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, T_C = −40°C)	I_{GT}				mAdc
MT2(+), G(+); MT2(−), G(−); R_L = 50 Ohms		—	—	80	
MT2(+), G(−); R_L = 25 Ohms		—	—	80	
DC Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc)	V_{GT}				Vdc
MT2(+), G(+); MT2(−), G(−); R_L = 100 Ohms		—	—	2.5	
MT2(+), G(−); R_L = 50 Ohms		—	—	2.5	
DC Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, T_C = −40°C)	V_{GT}				Vdc
MT2(+), G(+); MT2(−), G(−); R_L = 50 Ohms		—	—	3.5	
MT2(+), G(−); R_L = 25 Ohms		—	—	3.5	
DC Gate Non-Trigger Voltage (V_D = Rated V_{DRM}, R_L = 1K Ohms, T_C = 115°C) All Trigger Modes	V_{GD}	0.20	—	—	Vdc
Holding Current (V_D = 24 Vdc, Peak Initiating Current = 0.5 A, Pulse Width = 0.1 to 10 ms, Gate Trigger) (Source = 7 V, 20 Ohms) T_C = +25°C	I_H	—	—	50	mAdc
T_C = −40°C		—	—	100	
Latching Current (V_D = 24 Vdc, Gate Trigger Source = 15 V, 100 Ohms, Pulse Width = 50 μs, 5 μs Maximum Rise and Fall Times) MT2(+), G(+); MT2(−), G(−); MT2(+), G(−) T_C = 25°C	I_L	—	—	100	mAdc
MT2(+), G(+); MT2(−), G(−); MT2(+), G(−) T_C = −40°C		—	—	200	

FIGURE 1 – CURRENT DERATING

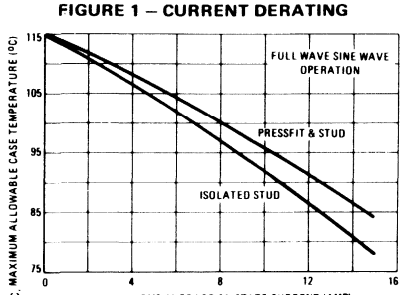
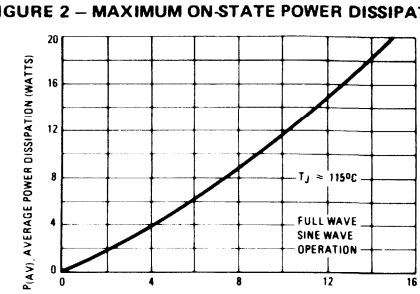


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION



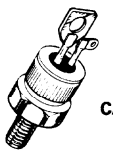
Triacs
Bidirectional Triode Thyristors

SC260
SC260( )3
SC261

TRIACs
25 AMPERES RMS
200 thru 600 VOLTS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 3 Quadrants



CASE 263-04
STYLE 2
SC260

CASE 310-02
STYLE 2
SC261

CASE 311-02
STYLE 2
SC260( )3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_C = −40°C to +115°C)	V_{DRM}		Volts
SC260B, SC260B3, SC261B		200	
SC260D, SC260D3, SC261D		400	
SC260M, SC260M3, SC261M		600	
RMS On-State Current	$I_{T(RMS)}$	25	Amps
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz)	I_{TSM}	250	Amps
Circuit Fusing Considerations	I^2t		A^2s
t = 1 ms		150	
t = 8.3 ms		260	
Peak Gate Power (Pulse Width = 10 μs)	P_{GM}	10	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Power	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	−40 to +115	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
SC260, SC261		1.8	
SC260( )3		1.95	

3

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted. Values apply for either polarity of Main Terminal 2 Characteristics referenced to Main Terminal 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = +115°C		—	—	1	mA
Peak On-State Voltage (I_{TM} = 35 A Peak, Pulse Width = 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	—	1.58	Volts
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Gate Open-Circuited, Exponential Waveform) T_C = +115°C	dv/dt	50	—	—	V/μs
Critical Rate-of-Rise of Commutating Off-State Voltage ($I_{T(RMS)}$ = Rated RMS On-State Current) (V_{DRM} = Rated Peak Off-State Voltage, Gate Open-Circuited, Commutating di/dt = 13.5 A/ms) T_C = +80°C	dv/dt(c)	5	—	—	V/μs
DC Gate Trigger Current (Continuous dc) (V_D = 12 Vdc)	I_{GT}				mAdc
MT2(+), G(+); MT2(−), G(−); R_L = 100 Ohms		—	—	50	
MT2(+), G(−); R_L = 50 Ohms		—	—	50	
DC Gate Trigger Current (Continuous dc) (V_D = 12 Vdc) T_C = −40°C	I_{GT}				mAdc
MT2(+), G(+); MT2(−), G(−); R_L = 50 Ohms		—	—	80	
MT2(+), G(−); R_L = 25 Ohms		—	—	80	
DC Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc)	V_{GT}				Vdc
MT2(+), G(+); MT2(−), G(−); R_L = 100 Ohms		—	—	2.5	
MT2(+), G(−); R_L = 50 Ohms		—	—	2.5	
DC Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc) T_C = −40°C	V_{GT}				Vdc
MT2(+), G(+); MT2(−), G(−); R_L = 50 Ohms		—	—	3.5	
MT2(+), G(−); R_L = 25 Ohms		—	—	3.5	
DC Gate Non-Trigger Voltage (V_D = Rated V_{DRM}, R_L = 1K Ohms, All Trigger Modes) T_C = 115°C	V_{GD}	0.25	—	—	Vdc
Holding Current (V_D = 24 Vdc, Peak Initiating Current = 0.5 A, Pulse Width = 0.1 to 10 ms, Gate Trigger Source = 7 V, 20 Ohms) T_C = +25°C	I_H	—	—	75	mAdc
T_C = −40°C		—	—	100	
Latching Current (V_D = 24 Vdc, Gate Trigger Source = 15 V, 100 Ohms, Pulse Width = 50 μs, 5 μs Maximum Rise and Fall Times)	I_L				mAdc
MT2(+), G(+); MT2(−), G(−) T_C = 25°C		—	—	100	
MT2(+), G(−) T_C = 25°C		—	—	200	
MT2(+), G(+); MT2(−), G(−) T_C = −40°C		—	—	200	
MT2(+), G(−) T_C = −40°C		—	—	400	

FIGURE 1 – CURRENT DERATING

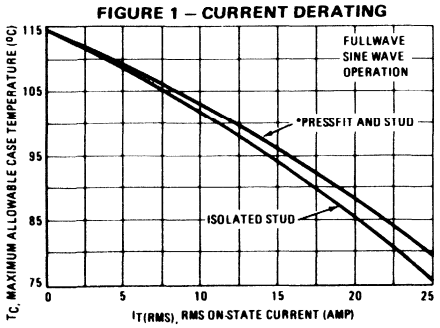
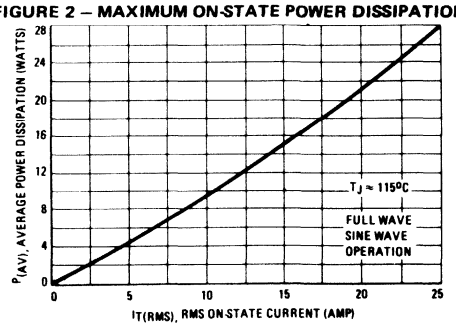


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION



3

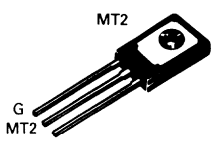
Sensitive Gate Triacs
Silicon Bidirectional Triode Thyristors

T2322
T2323
Series

SENSITIVE GATE TRIACs
2.5 AMPERES RMS
200 thru 600 VOLTS

. . . designed primarily for ac power switching. The gate sensitivity of these triacs permits the use of economical transistorized or integrated circuit control circuits, and it enhances their use in low-power phase control and load-switching applications.

- Very High Gate Sensitivity
- Low On-State Voltage at High Current Levels
- Glass-Passivated Chip for Stability
- Small, Rugged Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability



CASE 77-05
(TO-225AA)
STYLE 5

3

MAXIMUM RATINGS (Apply for T_J = −40 to 100°C unless otherwise noted.)

Rating	Suffix	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 T2322, T2323	B D M	V_{DRM}	200 400 600	Volts
RMS On-State Current (T_C = 70°C) (Full-cycle sine wave 50 to 60 Hz)		$I_{T(RMS)}$	2.5	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)		I_{TSM}	25	Amps
Circuit Fusing (t = 8.3 ms)		I^2t	2.6	A^2s
Peak Gate Power (1 μs)		P_{GM}	10	Watts
Average Gate Power (T_C = 60°C + 38.3 ms)		$P_{G(AV)}$	0.15	Watt
Peak Gate Current (1 μs)		I_{GM}	0.5	Amp
Operating Junction Temperature Range		T_J	−40 to +110	°C
Storage Temperature Range		T_{stg}	−40 to +150	°C
Mounting Torque (6-32 Screw), Note 2		—	8	in. lb.

Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting Torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heat-sink contact pad are common.

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C and either polarity of MT2 to MT1 voltage unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 100°C		—	0.2	0.75	mA
Peak On-State Voltage (I_{TM} = 10 A) T2323 Series	V_{TM}	—	1.7	2.6	Volts
T2322 Series		—	1.7	2.2	
Gate Trigger Current (Continuous dc) (All Modes) (V_D = 12 V, R_L = 30 Ω)	I_{GT}	—	—	10	mA
T2322 Series		—	—	25	
MT2(+), G(+); MT2(−), G(−) T2323 Series		—	—	40	
MT2(+), G(−); MT2(−), G(+) T2323 Series		—	—	—	
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 30 Ω, T_C = 25°C)	V_{GT}	—	1	2.2	Volts
(V_D = V_{DROM}, R_L = 125 Ω, T_C = 100°C)		0.15	—	—	
Holding Current (V_D = 12 V, I_{TM} = 150 mA, Gate Open)	I_H	—	15	30	mA
Gate-Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 10 A pk, I_G = 60 mA)	t_{gt}	—	1.8	2.5	μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 100°C)	dv/dt	10	100	—	V/μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 3.5 A pk, Commutating di/dt = 1.8 A/ms, Gate Unenergized, T_C = 90°C)	dv/dt(c)	1	4	—	V/μs

3

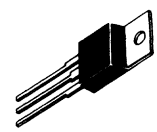
Triacs
Silicon Bidirectional Thyristors

T2500 Series

TRIACs
6 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability



CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +100°C) Gate Open T2500 B D M N	V_{DROM}	 200 400 600 800	Volts
On-State Current RMS (T_C = +80°C) (Full Cycle Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	6	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +80°C)	I_{TSM}	60	Amps
Circuit Fusing Considerations (T_J = −40 to +100°C, t = 1.25 to 10 ms)	I^2t	18	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 1 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.2	Watt
Peak Gate Trigger Current (Pulse Width = 10 μs)	I_{GTM}	4	Amps
Operating Junction Temperature Range	T_J	−40 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

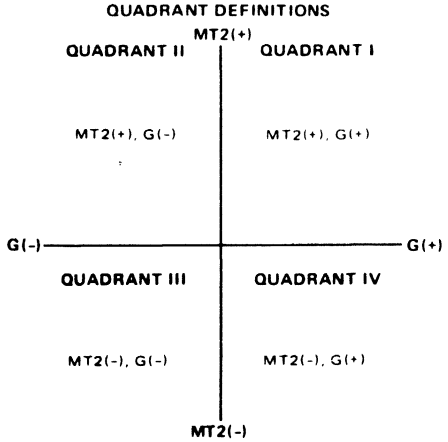
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 100°C	I_{DRM}, I_{RRM}	—	—	2	mA
Maximum On-State Voltage (Either Direction) (I_T = 30 A Peak)	V_{TM}	—	—	2	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 12 Ohms)	I_{GT}				mA
$V_{MT2(+)}$, $V_{G(+)}$		—	10	25	
$V_{MT2(+)}$, $V_{G(-)}$		—	20	60	
$V_{MT2(-)}$, $V_{G(-)}$		—	15	25	
$V_{MT2(-)}$, $V_{G(+)}$		—	30	60	
Gate Trigger Voltage (Continuous dc) (All Quadrants) (V_D = 12 Vdc, R_L = 12 Ohms)	V_{GT}	—	1.25	2.5	Volts
(V_D = V_{DROM}, R_L = 125 Ohms, T_C = 100°C)		0.2	—	—	
Holding Current (Either Direction) (Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 150 mA, T_C = 25°C)	I_{HO}	—	15	30	mA
Gate Controlled Turn-On Time (Rated V_{DROM}, I_T = 10 A, I_{GT} = 160 mA, Rise Time = 0.1 μs)	t_{gt}	—	1.6	—	μs
Critical Rate of Rise of Commutation Voltage (Rated V_{DROM}, $I_{T(RMS)}$ = 6 A, Commutating di/dt = 3.2 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	10	—	V/μs
Critical Rate of Rise of Off-State Voltage (Rated V_{DROM}, Exponential Voltage Rise, Gate Open, T_C = 100°C) T2500B	dv/dt	—	100	—	V/μs
T2500D,M,N		—	75	—	

3

QUADRANT DEFINITIONS



ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General	
PART NUMBER	MBS4991	MBS4992
V_S	6.0 – 10 V	7.5 – 9.0 V
I_S	350 μA Max	120 μA Max
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max
Temperature Coefficient	0.02%/°C Typ	

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

Silicon Bidirectional Triode Thyristors

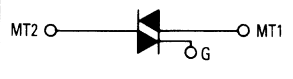
T2500FP Series

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Isolated Construction for Low Thermal Resistance, High Heat Dissipation and Durability

ISOLATED TRIACs THYRISTORS 6 AMPERES RMS 200–800 VOLTS

CASE 221C-02 STYLE 3



3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −40 to +100°C) Gate Open	V_{DROM}		Volts
T2500BFP		200	
T2500DFP		400	
T2500MFP		600	
T2500NFP		800	
On-State RMS Current (T_C = +80°C), Note 2 Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	6	Amps
Peak Nonrepetitive Surge Current (One Full Cycle, 60 Hz, T_C = +80°C)	I_{TSM}	100	Amps
Circuit Fusing Considerations (T_J = −40 to +100°C, t = 1.25 to 10 ms)	I^2t	41	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 1 μs)	P_{GM}	1	Watt
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.2	Watt
Peak Gate Trigger Current (Pulse Width = 10 μs)	I_{GTM}	4	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%)	V_{ISO}	1500	Volts
Operating Junction Temperature Range	T_J	−40 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case, Note 2	$R_{\theta JC}$	2.7	°C/W
Case to Sink	$R_{\theta CS}$	2.2 (typ)	
Junction to Ambient	$R_{\theta JA}$	60	

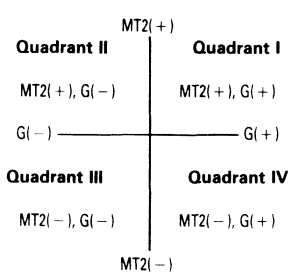
Notes: 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

Thermowatt is a trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) Rated V_{DROM} @ T_J = 100°C, Gate Open	I_{DROM}	—	—	2	mA
Maximum On-State Voltage (Either Direction) I_T = 30 A Peak	V_{TM}	—	—	2	Volts
Gate Trigger Current (Continuous dc) V_D = 12 Vdc, R_L = 12 Ohms $V_{MT2(+)}$, $V_{G(+)}$ $V_{MT2(+)}$, $V_{G(-)}$ $V_{MT2(-)}$, $V_{G(-)}$ $V_{MT2(-)}$, $V_{G(+)}$	I_{GT}	 — — — —	 10 20 15 30	 25 60 25 60	mA
Gate Trigger Voltage (Continuous dc) (All Quadrants) V_D = 12 Vdc, R_L = 12 Ohms V_D = V_{DROM}, R_L = 125 Ohms, T_C = 100°C, All Trigger Modes	V_{GT}	 — 0.2	 1.25 —	 2.5 —	Volts
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 150 mA, T_C = 25°C	I_{HO}	—	15	30	mA
Gate Controlled Turn-On Time Rated V_{DROM}, I_T = 10 A, I_{GT} = 160 mA, Rise Time = 0.1 μs	t_{gt}	—	1.6	—	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DROM}, $I_{T(RMS)}$ = 6 A, Commutating di/dt = 3.2 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(C)	—	10	—	V/μs
Critical Rate of Rise of Off-State Voltage Rated V_{DROM}, Exponential Voltage Rise, Gate Open, T_C = 100°C	dv/dt	—	100	—	V/μs

Quadrant Definitions



Trigger devices are recommended for gating on Triacs. They provide:
1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

Electrical Characteristics of Recommended Bidirectional Switches

Usage	General	
Part Number	MBS4991	MBS4992
V_S	6–10 V	7.5–9 V
I_S	350 μA Max	120 μA Max
V_{S1}–V_{S2}	0.5 V Max	0.2 V Max
Temperature Coefficient	0.02%/°C Typ	

3

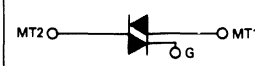
Triacs
Bidirectional Triode Thyristors

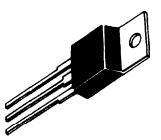
T2800
T2802
Series

TRIACs
8 AMPERES RMS
200 thru 600 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- T2800 — Four Quadrant Gating
  T2802 — Two Quadrant Gating





CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating			Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 (T_J = −40 to +100°C) Gate Open			V_{DROM}		Volts
	T2800, T2802	B		200	
		D		400	
		M		600	
RMS On-State Current (Conduction Angle = 360°)	(T_C = +80°C)		$I_{T(RMS)}$	8	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C)			I_{TSM}	100	Amps
Fusing Circuit (T_J = −40 to +100°C, t = 1.25 to 10 ms)			I^2t	50	A^2s
Peak Gate Power (Pulse Width = 1 μs)			P_{GM}	16	Watts
Average Gate Power			$P_{G(AV)}$	0.35	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)			I_{GTM}	4	Amps
Operating Junction Temperature Range			T_J	−40 to +100	°C
Storage Temperature Range			T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = 100°C		—	—	2	mA
Peak On-State Voltage (Either Direction) (I_T = 30 A Peak)	V_{TM}	—	1.7	2	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 12 Ohms)	I_{GT}				mA
$V_{MT2(+)}$, $V_{G(+)}$ T2800			10	25	
T2802			25	50	
$V_{MT2(+)}$, $V_{G(-)}$ T2800 Only		—	20	60	
$V_{MT2(-)}$, $V_{G(-)}$ T2800		—	15	25	
T2802		—	25	50	
$V_{MT2(-)}$, $V_{G(+)}$ T2800 Only		—	30	60	
Gate Trigger Voltage (Continuous dc) (All Polarities) (V_D = 12 Vdc, R_L = 100 Ohms)	V_{GT}	—	1.25	2.5	Volts
(R_L = 125 Ohms, V_D = V_{DRM}, T_C = 100°C)		0.2	—	—	
Holding Current (Either Direction) (V_D = 12 Vdc, Gate Open) T2800	I_{HO}	—	15	30	mA
(I_T = 125 mA) T2802		—	20	60	
Gate Controlled Turn-On Time (Rated V_{DROM}, I_T = 10 A, I_{GT} = 80 mA, Rise Time = 0.1 μs)	t_{gt}	—	1.6	—	μs
Critical Rate of Rise of Commutation Voltage (Rated V_{DRM}, $I_{T(RMS)}$ = 8 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	10	—	V/μs
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C)	dv/dt				V/μs
T2800 B		100	—	—	
T2802 D		75	—	—	
M		60	—	—	

3

FIGURE 1 – CURRENT DERATING

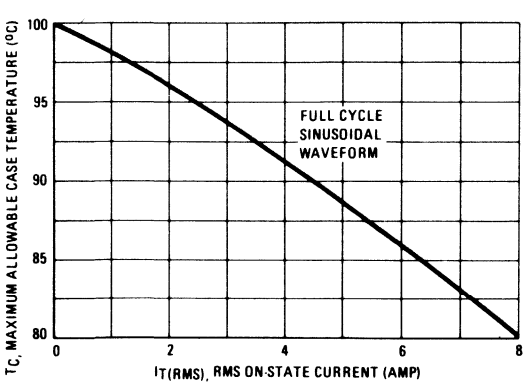
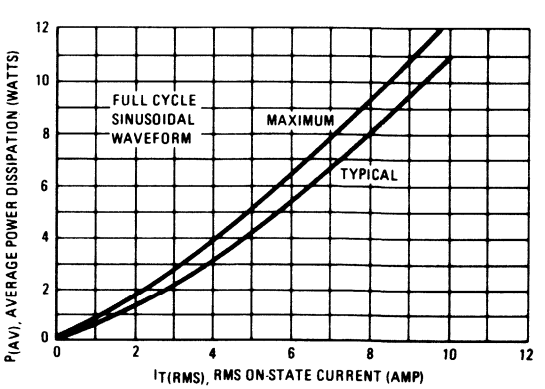


FIGURE 2 – POWER DISSIPATION



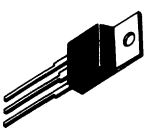
Triacs
Bidirectional Triode Thyristors

T2801 Series

TRIACs
6 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability



CASE 221A-04
(TO-220AB)
STYLE 4

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 (T_J = −40 to +100°C) Gate Open	V_{DRM}		Volts
T2801 B		200	
T2801 D		400	
T2801 M		600	
T2801 N		800	
RMS On-State Current (T_C = +80°C) (Conduction Angle = 360°)	$I_{T(RMS)}$	6	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	80	Amps
Fusing Circuit (T_J = −40 to +100°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)	P_{GM}	0.35	Watt
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amps
Operating Junction Temperature Range	T_J	−40 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C, Either Polarity of MT2 to MT1 Voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current T_J = 25°C (Rated V_{DRM}, Gate Open, T_J = 100°C)	I_{DRM}	— —	— —	10 2	μA mA
Peak On-State Voltage (I_{TM} = 30 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	2	3	Volts
Gate Trigger Current (Continuous dc), Note 1 (V_D = 12 Vdc, R_L = 12 Ohms)	I_{GT}	—	25	80	mA
Gate Trigger Voltage (Continuous dc), Note 1 (V_D = 12 Vdc, R_L = 12 Ohms) (V_D = V_{DRM}, R_L = 125 Ohms, T_C = 100°C)	V_{GT}	— 0.2	1.5 —	4 —	Volts
Holding Current (Either Direction) (V_D = 12 Vdc, Gate Open, Initiating Current = 150 mA)	I_H	—	100	—	mA
Turn-On Time (1) (V_D = Rated V_{DRM}, I_T = 10 A, I_{GT} = 80 mA, Rise Time = 0.1 μs)	t_{gt}	—	2.2	—	μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 6 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C)	dv/dt(c)	—	10	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C)	dv/dt				V/μs
T2801 B		50	—	—	
D		30	—	—	
M		10	—	—	
N		10	—	—	

Note 1. Applies for MT2(+), G(+), MT2(−), G(−).

3

FIGURE 1 – CURRENT DERATING

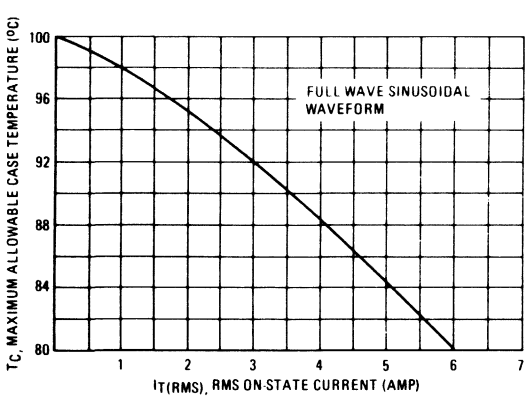
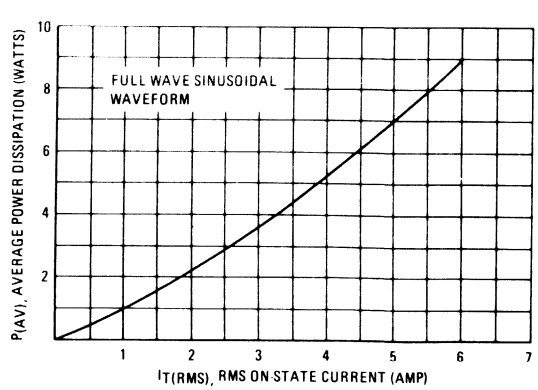


FIGURE 2 – POWER DISSIPATION



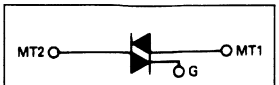
Triacs
Silicon Bidirectional Triode Thyristors

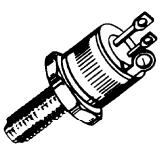
T4120 Series

TRIACs
15 AMPERES RMS
200 thru 800 VOLTS

. . . designed primarily for industrial and military applications for full wave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Isolated Stud Package
- Gate Triggering Guaranteed In All 4 Quadrants





CASE 235-03
STYLE 2

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 (T_J = −65 to +100°C) Gate Open	V_{DRM}		Volts
T4120 B		200	
D		400	
M		600	
N		800	
RMS On-State Current (Conduction Angle = 360°) T_C = +75°C	$I_{T(RMS)}$	15	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amps
Circuit Fusing (T_J = −65 to +100°C, t = 1.25 to 10 ms)	I^2t	50	A^2s
Peak Gate Power (Pulse Width = 1 μs)	P_{GM}	16	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amps
Operating Case Junction Temperature Range	T_C	−65 to +100	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, either polarity of MT2 to MT1 voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_C = 100°C		—	—	2	mA
Peak On-State Voltage (I_T = 21 A Peak)	V_{TM}	—	1.4	1.8	Volt
Gate Trigger Current (Continuous dc), Note 1 (V_D = 12 Vdc, R_L = 30 Ohms)	I_{GT}				mA
$V_{MT2(+)}$, $V_{G(+)}$; $V_{MT2(-)}$, $V_{G(-)}$		—	—	50	
$V_{MT2(+)}$, $V_{G(-)}$; $V_{MT2(-)}$, $V_{G(+)}$		—	—	80	
$V_{MT2(+)}$, $V_{G(+)}$; $V_{MT2(-)}$, $V_{G(-)}$, T_C = −65°C		—	—	150	
$V_{MT2(+)}$, $V_{G(-)}$; $V_{MT2(-)}$, $V_{G(+)}$, T_C = −65°C		—	—	200	
Gate Trigger Voltage (Continuous dc) (All Quadrants) (V_D = 12 Vdc, R_L = 30 Ohms)	V_{GT}				Volts
T_C = 25°C		—	—	2.5	
T_C = −65°C		—	—	4	
(V_D = Rated V_{DROM}, R_L = 125 Ohms, T_C = 100°C)		0.2	—	—	
Holding Current (V_D = 12 Vdc, Gate Open)	I_H				mA
(I_T = 500 mA) T_C = 25°C		—	—	75	
T_C = −65°C		—	—	300	
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 25 A Peak, I_{GT} = 160 mA, Rise Time = 0.1 μs)	t_{gt}	—	1.6	2.5	μs
Critical Rate of Rise of Commutation Voltage (Rated V_{DRM}, $I_{T(RMS)}$ = 15 A, Cummutating di/dt = 8 A/ms, Gate Unenergized, T_C = 75°C)	dv/dt(c)	2	10	—	V/μs
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C)	dv/dt				V/μs
T4120 B		30	150	—	
D		20	100	—	
M		10	75	—	
N		10	—	—	

Note 1. All Voltage polarities referenced to main terminal 1.

FIGURE 1 – CURRENT DERATING

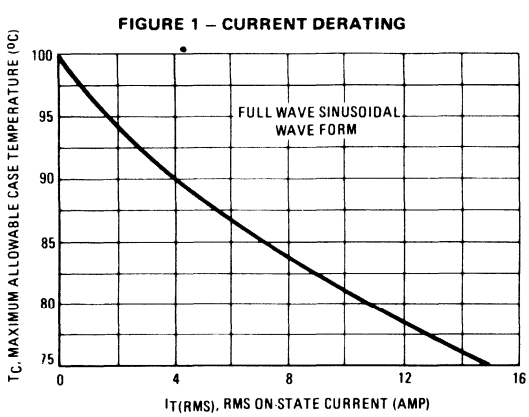
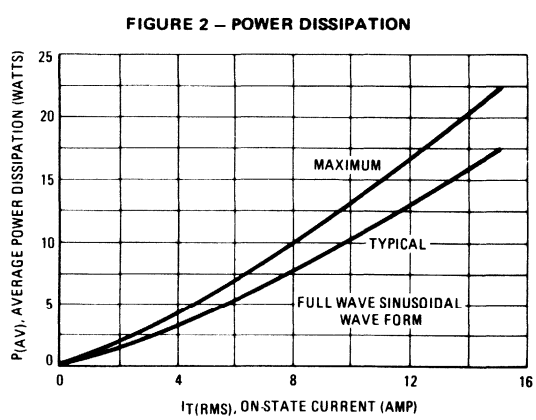


FIGURE 2 – POWER DISSIPATION



3

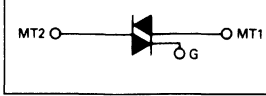
Triacs
Silicon Bidirectional Triode Thyristors

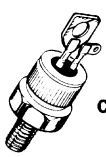
T6400
T6410
T6420
Series

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Press Fit Stud — T6400
  Stud — T6410
  Isolated Stud — T6420
- Gate Triggering Guaranteed in All 4 Quadrants

TRIACs
40 AMPERES RMS
200 thru 800 VOLTS





CASE 263-04
STYLE 2
T6410
STUD

CASE 310-02
STYLE 2
T6400
PRESS FIT

CASE 311-02
STYLE 2
T6420
ISOLATED STUD

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 (T_J = −65 to +110°c) Gate Open	V_{DRM}		Volts
T6400B, T6410B, T6420B		200	
T6400D, T6410D, T6420D		400	
T6400M, T6410M, T6420M		600	
T6400N, T6410N, T6420N		800	
On-State Current RMS (Conduction Angle = 360°) T_C (Pressfit) = 70°C, T_C (Stud) = 65°C	$I_{T(RMS)}$	40	Amps
Peak Surge Current (Non-Repetitive) (One Full Cycle, 60 Hz)	I_{TSM}	300	Amps
Circuit Fusing (T_J = −65 to +110°C, t = 1.25 to 10 ms)	I^2t	450	A^2s
Peak Gate Power (Pulse Width = 10 μs)	P_{GM}	40	Watts
Average Gate Power	$P_{G(AV)}$	0.75	Watt
Peak Gate Current (Pulse Width = 1 μs)	I_{GTM}	12	Amps
Operating Temperature Range	T_C	−65 to +110	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit	$R_{\theta JC}$	0.8	°C/W
Stud		0.9	
Isolated Stud		1	

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 110°C		—	—	4	mA
Maximum On-State Voltage (Either Direction) (I_T = 100 A Peak)	V_{TM}	—	1.5	2	Volts
Gate Trigger Current (Continuous dc), Note 1 (V_D = 12 Vdc, R_L = 30 Ohms	I_{GT}				mA
$V_{MT2(+)}$, $V_{G(+)}$		—	15	50	
$V_{MT2(+)}$, $V_{G(-)}$		—	30	80	
$V_{MT2(-)}$, $V_{G(-)}$		—	20	50	
$V_{MT2(-)}$, $V_{G(+)}$		—	40	80	
$V_{MT2(+)}$, $V_{G(+)}$, $V_{MT2(-)}$, $V_{G(-)}$, T_C = −65°C		—	—	125	
$V_{MT2(+)}$, $V_{G(-)}$, $V_{MT2(-)}$, $V_{G(+)}$, T_C = −65°C		—	—	240	
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 30 Ohms, T_C = 25°C	V_{GT}	—	1.35	2.5	Volts
T_C = −65°C		—	—	3.4	
(V_D = Rated V_{DRM}, R_L = 125 Ohms, T_C = 110°C)		0.2	—	—	
Holding Current (Either Direction) (V_D = 12 Vdc, Gate Open) (Initiating Current = 500 mA) T_C = 25°C	I_{HO}	—	25	60	mA
T_C = −65°C		—	—	100	
Gate Controlled Turn-On Time (Rated V_{DRM}, I_T = 60 A, I_{GT} = 200 mA, Rise Time = 0.1 μs)	t_{gt}	—	1.7	3	μs
Critical Rate of Rise of Commutation Voltage, On-State Conditions (di/dt = 22 A/ms, Gate Unenergized, V_D = Rated V_{DROM}, $I_{T(RMS)}$ = 40 A, T_C (Pressfit) = 70°C) T_C (Stud) = 65°C	dv/dt(c)	—	5	—	V/μs

Note 1. All voltage polarities referenced to main terminal 1.

3

FIGURE 1 – ON-STATE POWER DISSIPATION

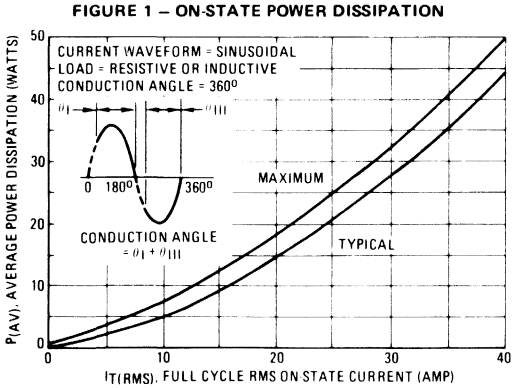
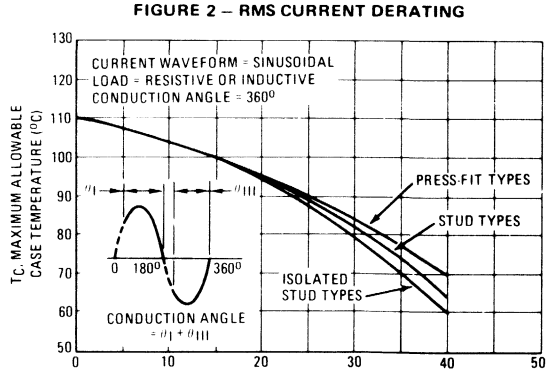


FIGURE 2 – RMS CURRENT DERATING



Triacs
Silicon Bidirectional Triode Thyristors

T6401
T6411
T6421
Series

. . . designed primarily for industrial and military applications for full wave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- Glass Passivated Junctions and Center Gate Fire
- Press Fit, Stud, Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Modes

TRIACs
30 AMPERES RMS
200 thru 800 VOLTS

CASE 263-04
STYLE 2
T6401
PRESS FIT

CASE 310-02
STYLE 2
T6411
STUD

CASE 311-02
STYLE 2
T6421
ISOLATED STUD

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = −65 to +100°C) Gate Open T6401B, T6411B, T6421B T6401D, T6411D, T6421D T6401M, T6411M, T6421M T6401N, T6411N, T6421N	V_{DRM}	 200 400 600 800	Volts
On-State Current RMS (Conduction Angle = 360°) $T_C \leq +65°C$	$I_{T(RMS)}$	30	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	300	Amps
Circuit Fusing (T_J = −65 to +100°C, t = 1.25 to 10 ms)	I^2t	450	A^2s
Peak Gate Power (Pulse Width = 1 μs)	P_{GM}	40	Watts
Average Gate Power	$P_{G(AV)}$	0.75	Watt
Peak Gate Current Pulse Width ≤ 1 μs)	I_{GTM}	2	Amps
Operating Case Temperature Range	T_C	−65 to +100	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit Stud Isolated Stud	$R_{\theta JC}$	0.8 0.9 1	°C/W

Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_J = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
T_J = 100°C		—	—	4	mA
Maximum On-State Voltage (Either Direction) (I_T = 100 A Peak)	V_{TM}	—	2.1	2.5	Volts
Gate Trigger Current (Continuous dc), Note 1 (V_D = 12 Vdc, R_L = 30 Ohms	I_{GT}				mA
$V_{MT2(+)}$, $V_{G(+)}$; $V_{MT2(-)}$, $V_{G(-)}$		—	20	50	
$V_{MT2(+)}$, $V_{G(-)}$; $V_{MT2(-)}$, $V_{G(+)}$		—	35	80	
Gate Trigger Voltage (Continuous dc) (All Trigger Modes) (V_D = 12 Vdc, R_L = 30 Ohms)	V_{GT}	—	1.35	2.5	Volts
(V_D = Rated V_{DRM}, R_L = 125 Ohms, T_C = 100°C)		0.2	—	—	
Holding Current (V_D = 12 Vdc, Gate Open) (I_T = 150 mA)	I_{HO}	—	—	60	mA
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 45 A, I_{GT} = 200 mA, Rise Time = 0.1 μs)	t_{gt}	—	1.7	3	μs
Critical Rate of Rise of Commutation Voltage, On-State Conditions (di/dt = 16 A/ms, Gate Unenergized, V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 30 A, T_C = Rated Value from Figure 1)	dv/dt(c)	3	20	—	V/μs
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Rise, T_C = 100°C)	dv/dt				V/μs
T6401B, T6411B, T6421B		40	—	—	
T6401D, T6411D, T6421D		25	—	—	
T6401M, T6411M, T6421M		20	—	—	
T6401N, T6411N, T6421N		20	—	—	

Note 1. All voltage polarities referenced to main terminal 1.

3

FIGURE 1 – CURRENT DERATING

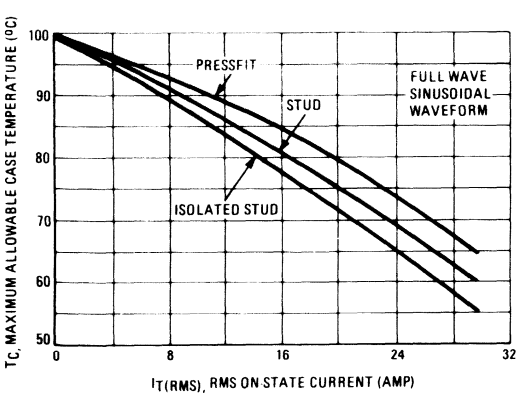
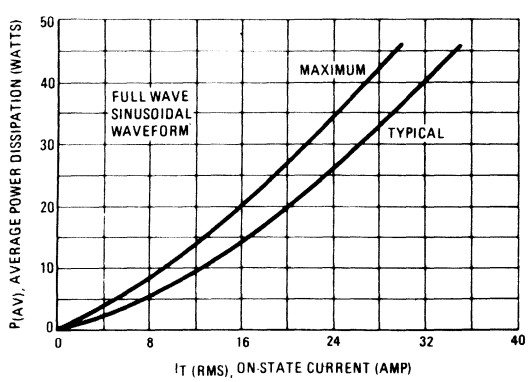


FIGURE 2 – POWER DISSIPATION



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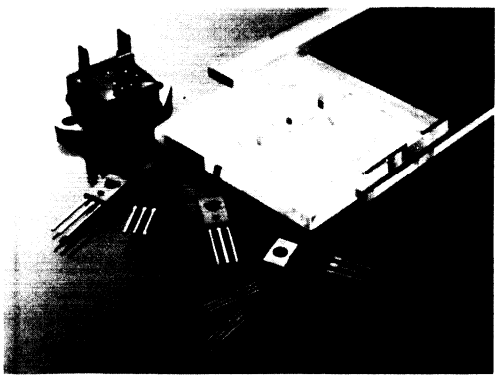
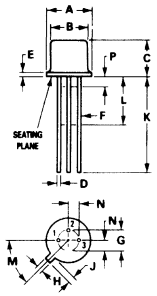


Outline Dimensions and Leadform Options

4

Outline Dimensions

CASE 22-03
TO-206AA (TO-18)
Styles 6, 13



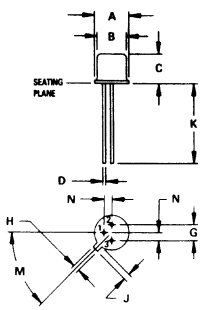
STYLE 6:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 13:
PIN 1. ANODE
2. GATE
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	—	0.762	—	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	—	1.27	—	0.050

All JEDEC notes and dimensions apply.

CASE 22A-01
Style 1

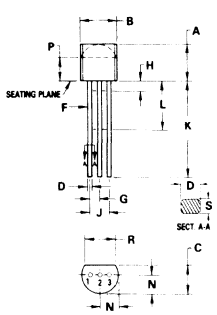


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. PIN 3 CONNECTED TO CASE

STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	—	0.500	—
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 29-04
TO-226AA (TO-92)
Styles 9, 10, 12, 16



NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

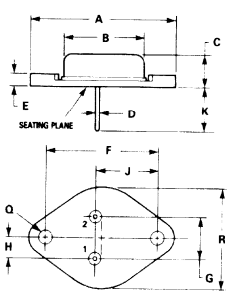
STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

CASE 54-05
Style 2

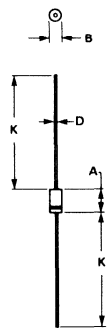


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.12	—	1.540
B	—	20.70	—	0.815
C	—	7.92	—	0.312
D	1.22	1.30	0.048	0.051
E	2.84	3.05	0.112	0.120
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	16.79	0.651	0.661
K	8.13	10.67	0.320	0.420
Q	3.84	4.09	0.151	0.161
R	—	26.16	—	1.030

STYLE 2 (THY):
PIN 1 GATE
2 CATHODE
CASE ANODE

4

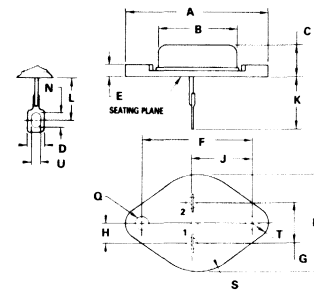
CASE 59-04



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO-41 OUTLINE SHALL APPLY.
2. POLARITY DENOTED BY CATHODE BAND.
3. LEAD DIAMETER NOT CONTROLLED WITHIN "F" DIMENSION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	—	1.100	—

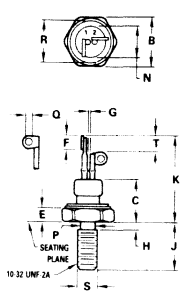
CASE 61-03
Style 1



STYLE 1:
PIN 1. GATE
2. CATHODE
CASE: ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.23	39.12	1.505	1.540
B	20.32	20.70	0.800	0.815
C	6.99	7.92	0.275	0.312
D	4.83	5.33	0.190	0.210
E	2.84	3.05	0.112	0.120
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	16.79	0.651	0.661
K	16.51	17.27	0.650	0.680
N	3.30	4.32	0.130	0.170
Q	3.84	4.09	0.151	0.161
R	24.64	26.16	0.970	0.030
U	2.29	2.79	0.090	0.110

CASE 63-03
Style 1

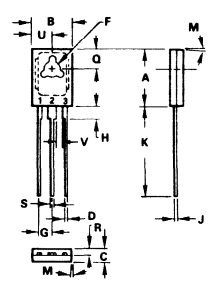


STYLE 1:
PIN 1. CATHODE
2. GATE
STUD: ANODE

NOTE
1. ALL RULES & NOTES ASSOCIATED WITH REFERENCED TO-64 OUTLINE SHALL APPLY

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	7.62	10.16	0.300	0.400
E	1.52	4.45	0.060	0.175
F	2.03	3.45	0.080	0.136
G	0.33	—	0.013	—
H	—	1.98	—	0.078
J	10.16	11.51	0.400	0.453
K	17.78	21.72	0.700	0.855
N	—	10.77	—	0.424
P	4.14	4.80	0.163	0.189
Q	1.02	1.91	0.040	0.075
R	10.16	—	0.400	—
S	4.212	4.310	0.1658	0.1697
T	1.52	—	0.060	—

CASE 77-05
TO-225AA
Styles 2, 5



NOTES:
1. MT = MAIN TERMINAL.
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION

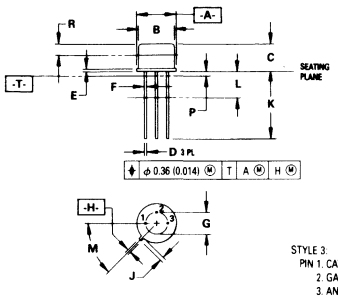
STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 5:
PIN 1. MT1
2. MT2
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

4

CASE 79-04
TO-205AD
Style 3

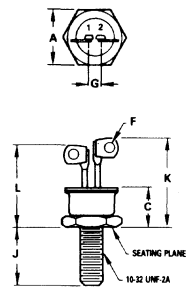


STYLE 3:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.41	0.53	0.016	0.021
E	0.23	1.04	0.009	0.041
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

CASE 86-01
Style 1

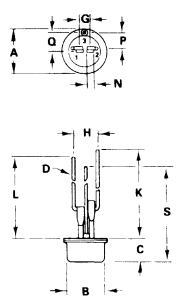


STYLE 1:
PIN 1. GATE
2. CATHODE
STUD: ANODE

NOTE:
1. DIM "G" MEASURED AT CAN.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	11.10	—	0.437
C	—	7.87	—	0.310
F	1.78 TYP		0.070 TYP	
G	2.29	2.79	0.090	0.110
J	10.72	11.48	0.422	0.452
K	—	16.76	—	0.660
L	—	15.49	—	0.610

CASE 87L-02
Style 1

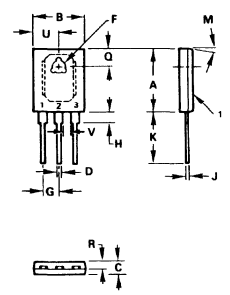


STYLE 1:
PIN 1. GATE
2. CATHODE
3. ANODE

NOTES:
1. DIM "G" MEASURED AT CAN.
2. LEAD NO. 3 ± 7.5° DISPLACEMENT.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	10.92	—	0.430
B	—	8.89	—	0.350
C	—	5.97	—	0.235
D	0.76	0.86	0.030	0.034
G	2.29	2.79	0.090	0.110
H	8.89	9.39	0.350	0.370
K	33.53	—	1.320	—
L	31.50 TYP		1.240 TYP	
N	1.65	1.91	0.065	0.075
P	3.43	3.68	0.135	0.145
Q	4.57	5.08	0.180	0.200
S	30.48	—	1.200	—

CASE 90-05
TO-225AB
Style 1



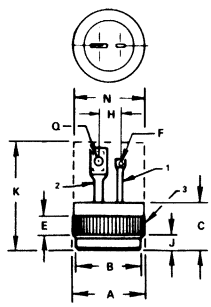
NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H".
2. DIM "F" DIA THRU.
3. HEAT SINK CONTACT AREA (BOTTOM).
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	—	0.080	—

4

CASE 174-04
Styles 1, 3

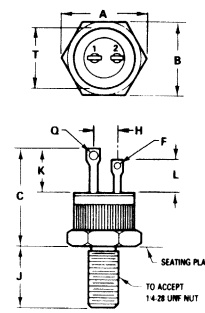


STYLE 1
TERM 1. GATE
2. CATHODE
3. ANODE

STYLE 3
TERM 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	—	0.100	—
F	0.89	2.16	0.035	0.085
H	3.75	4.41	0.148	0.174
J	2.04	2.46	0.080	0.097
K	—	20.32	—	0.800
N	—	12.95	—	0.510
Q	1.65	4.06	0.065	0.160

CASE 175-03
Styles 1, 3

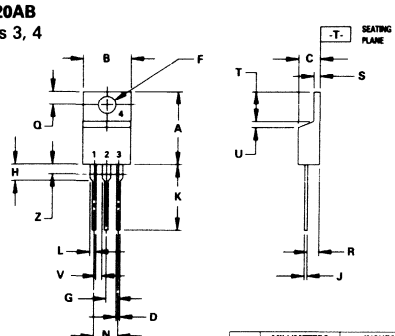


STYLE 1
TERM 1. CATHODE
2. GATE
STUD. ANODE

STYLE 3
TERM 1. MAIN TERMINAL 1
2. GATE
STUD. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	3.75	4.41	0.148	0.174
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.416
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
T	12.70	12.83	0.500	0.505

CASE 221A-04
TO-220AB
Styles 3, 4



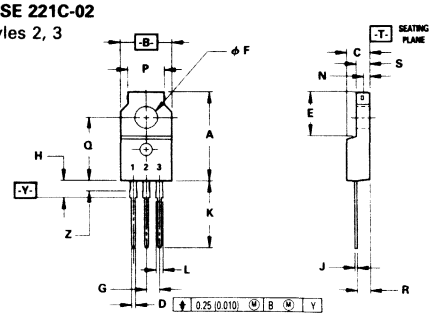
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221C-02
Styles 2, 3



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	17.28	17.78	0.680	0.700
B	9.86	10.36	0.388	0.408
C	4.45	4.95	0.175	0.195
D	0.64	1.01	0.025	0.040
E	8.64	9.01	0.340	0.355
F	3.56	3.81	0.140	0.150
G	2.54 BSC		0.100 BSC	
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	13.97	0.500	0.550
L	1.15	1.77	0.045	0.070
N	1.25	—	0.049	—
P	6.86	7.36	0.270	0.290
Q	12.20	12.70	0.480	0.500
R	2.29	3.04	0.090	0.120
S	2.67	2.92	0.105	0.115
Z	1.78	2.28	0.070	0.090

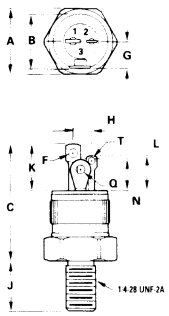
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD DIMENSION UNCONTROLLED WITHIN DIMENSION "Z".

STYLE 2:
PIN 1. CATHODE
2. NODE
3. GATE

STYLE 3:
PIN 1. MT 1
2. MT 2
3. GATE

4

CASE 235-03
Styles 1, 2

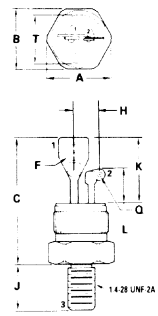


STYLE 1:
PIN 1: CATHODE
2: GATE
3: ANODE
STUD: ISOLATED

STYLE 2:
PIN 1: MAIN TERMINAL 1
2: GATE
3: MAIN TERMINAL 2
STUD: ISOLATED

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	—	26.16	—	1.030
F	1.65	4.06	0.065	0.160
G	—	6.48	—	0.255
H	3.75	4.41	0.148	0.174
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
T	0.89	2.16	0.035	0.086

CASE 263-04
Styles 1, 2

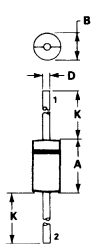


STYLE 1:
PIN 1: CATHODE
2: GATE
3: ANODE

STYLE 2:
PIN 1: MT 1
2: GATE
3: MT 2

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	—	6.73	—	0.265
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
T	12.73	12.83	0.501	0.505

CASE 267-03
Style 1

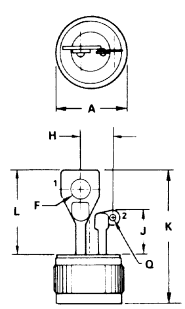


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	25.40	—	1.000	—

STYLE 1:
PIN 1: CATHODE
2: ANODE

CASE 310-02
Styles 1, 2



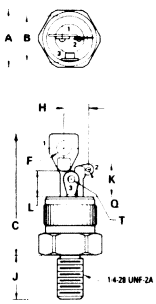
STYLE 1:
PIN 1: CATHODE
2: GATE
CASE: ANODE

STYLE 2:
PIN 1: MT 1
2: GATE
CASE: MT 2

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.73	12.83	0.501	0.505
F	—	4.06	—	0.160
H	—	6.73	—	0.265
J	7.62	8.89	0.300	0.350
K	—	26.67	—	1.050
L	—	17.02	—	0.670
Q	1.40	2.16	0.055	0.085

4

CASE 311-02
Styles 1, 2

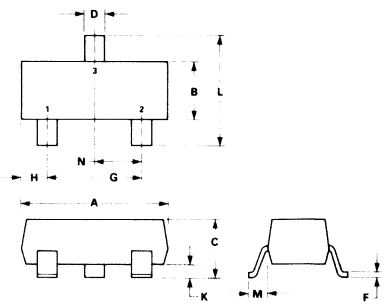


STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 2:
PIN 1. MT 1
2. GATE
3. MT 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	—	32.51	—	1.280
F	—	4.06	—	0.160
H	—	6.73	—	0.265
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 318-02
TO-236AA
Style 14

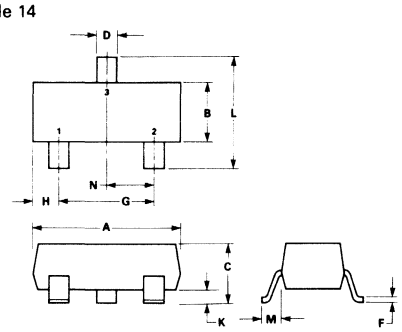


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
C	0.89	1.11	0.035	0.0440
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
K	0.013	0.10	0.0005	0.0040
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 318-03
TO-236AB
Style 14

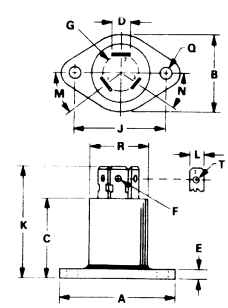


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.035	0.044
D	0.37	0.50	0.015	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.013	0.100	0.0005	0.0040
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.018	0.0236
N	0.89	1.02	0.0350	0.0401

NOTES:
1. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 326-01
Style 2



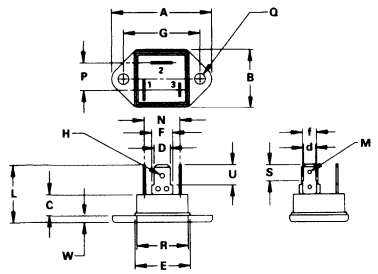
NOTE:
1. DIMENSIONS D AND F APPLY TO TERMINAL 1 AND 2.

STYLE 2:
PIN 1. MT 1
2. MT 2
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	26.67	—	1.050
C	—	27.30	—	1.075
D	6.22	6.48	0.245	0.255
E	3.02	3.33	0.119	0.131
F	1.52	2.03	0.060	0.080
G	12.19	12.70	0.480	0.500
J	29.90	30.40	1.177	1.197
K	35.56	37.08	1.400	1.460
L	4.57	4.95	0.180	0.195
M	35°	40°	38°	40°
N	30°	35°	30°	35°
Q	3.81	4.09	0.150	0.161
R	19.81	22.35	0.780	0.880
T	1.02	1.52	0.040	0.060

4

CASE 383-01
Style 1

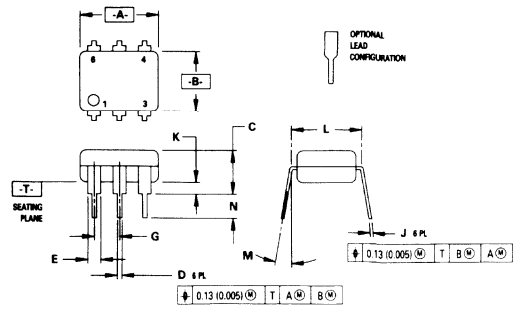


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.20	—	1.543
B	—	23.00	—	0.905
C	—	8.20	—	0.322
D	5.55	7.15	0.219	0.281
E	—	21.60	—	0.850
F	7.45	9.05	0.294	0.356
G	29.90	30.10	1.178	1.185
H	1.65	2.20	0.065	0.086
L	—	22.50	—	0.885
M	1.30	1.57	0.052	0.061
N	13.85	14.15	0.546	0.557
P	10.55	10.85	0.416	0.427
Q	4.10	4.30	0.162	0.169
R	—	20.10	—	0.791
S	6.20	6.50	0.244	0.255
U	7.80	8.10	0.307	0.318
W	2.30	2.90	0.091	0.114
d	4.58	5.08	0.180	0.200
f	5.34	5.58	0.210	0.220

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

STYLE 1:
PIN 1. MT1
2. MT2
3. GATE

CASE 730A-02
Style 6



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.13	8.89	0.320	0.350
B	6.10	6.60	0.240	0.260
C	2.93	5.08	0.115	0.200
D	0.41	0.50	0.016	0.020
E	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	0.38	2.54	0.015	0.100
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	2.54	3.81	0.100	0.150

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM L TO CENTER OF LEAD WHEN FORMED PARALLEL.

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
6. MAIN TERMINAL

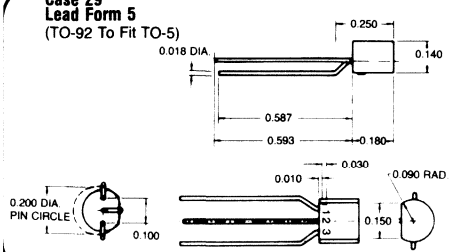
4

LEADFORM OPTIONS

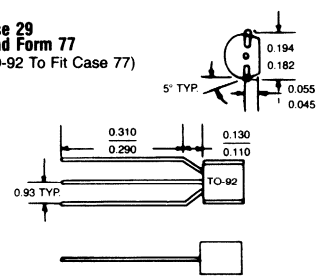
Plastic packaged semiconductors may be leadformed to a variety of configurations for insertion into sockets and boards designed for metal can devices. The following are standard thyristor and trigger leadforms offered by Motorola.

To order leadformed product, determine the form desired, and specify case number and applicable leadform number. A special device title will be assigned by the factory to process your order. Certain standard devices already incorporate a leadform, and may be purchased without consulting the factory.

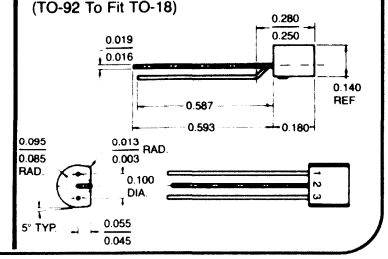
Case 29
Lead Form 5
(TO-92 To Fit TO-5)



Case 29
Lead Form 77
(TO-92 To Fit Case 77)



Case 29
Lead Form 18
(TO-92 To Fit TO-18)

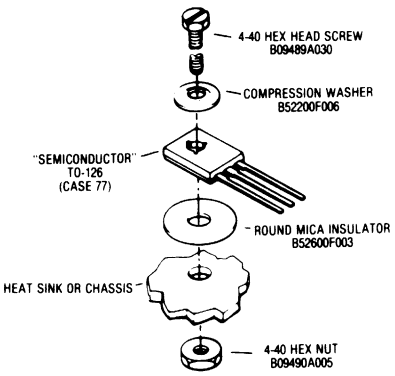


4

MOUNTING HARDWARE

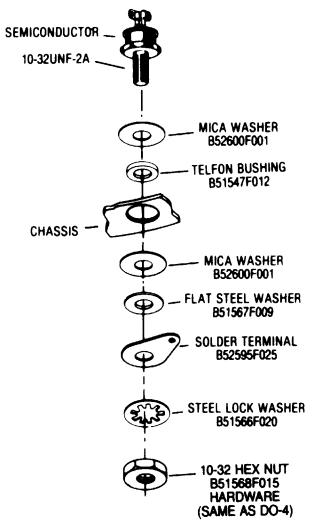
Information on recommended mounting techniques and hardware is available in data sheets listed for each package type, including part numbers for hardware items which may be purchased from Motorola.

CASE 77-05
TO-225AA
(Formerly TO-126)

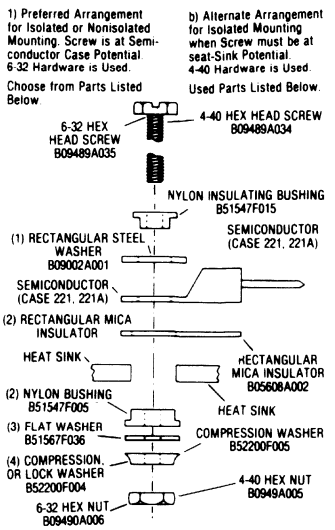


TORQUE REQUIREMENTS
0.68 N-m (6 IN. LBS.) MAX

CASE 86-01
(DO-4)



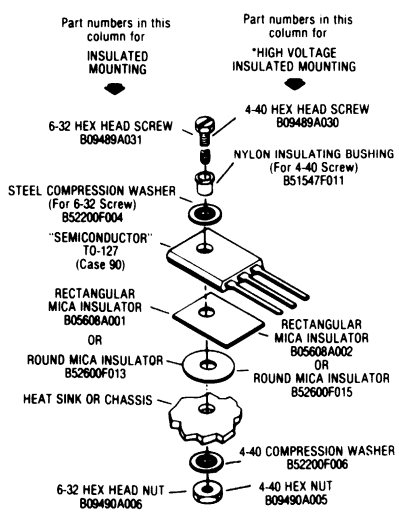
CASE 221A-04
TO-220AB



TORQUE REQUIREMENTS
Insulated 0.68 N-m (6 IN. LBS.) MAX
Noninsulated 0.9 N-m (8 IN. LBS.) MAX

(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing and lock washer are used.
(4) Compression washer preferred when plastic insulating material is used.

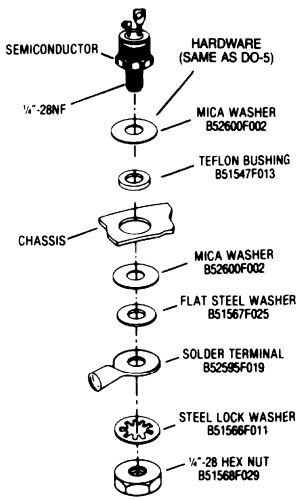
CASE 90-05
TO-225AB
(Formerly TO-127)

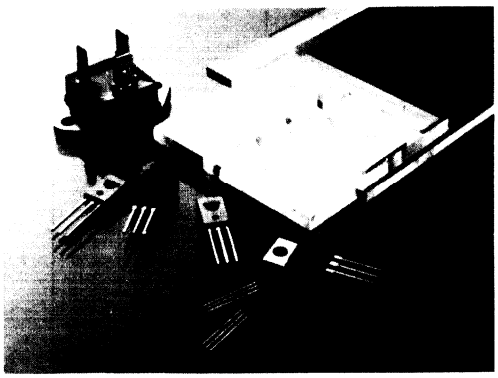


TORQUE REQUIREMENTS
Insulated 0.68 N-m (6 IN. LBS.) MAX
High Voltage Insulated 0.90 N-m (8 IN. LBS.) MAX

*High voltage mounting requirements depend on use environment. User is encouraged to make his own evaluation.

CASE 175-03
CASE 235-03
CASE 263-04
CASE 311-02
(DO-5)





Index and Cross Reference

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
0220100F		C228A	3-133
0220200F		C228B	3-133
0220300F		C228D	3-133
0220400F		C228D	3-133
0220500F		C228M	3-133
0220600F		C228M	3-133
0230100F		C228A	3-133
0230200F		C228B	3-133
0230300F		C228D	3-133
0230400F		C228D	3-133
0230500F		C228M	3-133
0230600F		C228M	3-133
1N5758		MBS4991	3-207
1N5758A		MBS4991	3-207
1N5759		MBS4991	3-207
1N5759A		MBS4991	3-207
1N5760		MBS4991	3-207
1N5761		MBS4991	3-207
1N5761A		MBS4991	3-207
1N5762		MBS4991	3-207
1N5762A		MBS4991	3-207
1N5779		MBS4991	3-207
1N5780		MBS4991	3-207
1N5781		MBS4991	3-207
1N5782		MBS4991	3-207
1N5783		MBS4991	3-207
1N5784		MBS4991	3-207
1N5785		MBS4991	3-207
1N5786		MBS4991	3-207
1N5787		MBS4991	3-207
1N5788		MBS4991	3-207
1N5789		MBS4991	3-207
1N5790		MBS4991	3-207
1N5791		MBS4991	3-207
1N5792		MBS4991	3-207
1N5793		MBS4991	3-207
2N681	2N682		3-2
2N682	2N682		3-2
2N683	2N683		3-2
2N684	2N685		3-2
2N685	2N685		3-2
2N686	2N688		3-2
2N687	2N688		3-2
2N688	2N688		3-2
2N689	2N680		3-2
2N690	2N690		3-2
2N691	2N692		3-2
2N692	2N692		3-2
2N876		MCR102	3-230
2N877		MCR102	3-230
2N878		MCR103	3-230
2N879		MCR100-3	3-228
2N880		MCR100-4	3-228
2N881		MCR100-4	3-228
2N882		MCR100-6	3-228
2N883		MCR100-6	3-228
2N884		MCR102	3-230
2N885		MCR102	3-230
2N886		MCR103	3-230
2N887		MCR100-3	3-228
2N888		MCR100-4	3-228
2N889		MCR100-4	3-228
2N890		MCR100-6	3-228
2N891		MCR100-6	3-228
2N948		MCR102	3-230
2N949		MCR103	3-230
2N950		MCR100-3	3-228
2N951		MCR100-4	3-228
2N1595	2N1595		3-6
2N1596	2N1596		3-6

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N1597	2N1597		3-6
2N1598	2N1599		3-6
2N1599	2N1599		3-6
2N1600		2N4168	3-27
2N1601		2N4169	3-27
2N1602		2N4170	3-27
2N1603		2N4172	3-27
2N1604		2N4172	3-27
2N1770		2N4168	3-27
2N1771		2N4168	3-27
2N1771A		2N4168	3-27
2N1772		2N4169	3-27
2N1772A		2N4169	3-27
2N1773		2N4170	3-27
2N1773A		2N4170	3-27
2N1774		2N4170	3-27
2N1774A		2N4170	3-27
2N1775		2N4172	3-27
2N1775A		2N4172	3-27
2N1776		2N4172	3-27
2N1776A		2N4172	3-27
2N1777		2N4172	3-27
2N1777A		2N4172	3-27
2N1778		2N4174	3-27
2N1778A		2N4174	3-27
2N1842	2N1843		3-8
2N1842A	2N1843A		3-11
2N1843	2N1843		3-8
2N1843A	2N1843A		3-11
2N1844	2N1844		3-8
2N1844A	2N1844A		3-11
2N1845	2N1846		3-8
2N1845A	2N1846A		3-11
2N1846	2N1846		3-8
2N1846A	2N1846A		3-11
2N1847	2N1849		3-8
2N1847A	2N1849A		3-11
2N1848	2N1849		3-8
2N1848A	2N1849A		3-11
2N1849	2N1849		3-8
2N1849A	2N1849A		3-11
2N1850		2N690	3-2
2N1850A		2N690	3-2
2N1869		2N4213	3-37
2N1869A		MCR1906-2	3-261
2N1870		2N4213	3-37
2N1870A		MCR1906-2	3-261
2N1871		2N4213	3-37
2N1871A		MCR1906-2	3-261
2N1872		2N4214	3-37
2N1872A		MCR1906-3	3-261
2N1873		2N4216	3-37
2N1873A		MCR1906-4	3-261
2N1874		2N4216	3-37
2N1874A		MCR1906-4	3-261
2N1875		2N2323	3-14
2N1875A		MCR1906-2	3-261
2N1876		2N2323	3-14
2N1876A		MCR1906-2	3-261
2N1877		2N2323	3-14
2N1877A		MCR1906-2	3-261
2N1878		2N2324	3-14
2N1878A		MCR1906-3	3-261
2N1879		2N2326	3-14
2N1879A		MCR1906-4	3-261
2N1880		2N2326	3-14
2N1880A		MCR1906-4	3-261
2N1881		MCR1906-2	3-261
2N1882		MCR1906-2	3-261

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N1883		MCR1906-3	3-261
2N1884		MCR1906-4	3-261
2N1885		MCR1906-4	3-261
2N2009		2N4213	3-37
2N2010		2N4213	3-37
2N2011		2N4214	3 37
2N2012		2N4216	3-37
2N2013		2N4219	3-37
2N2014		2N4219	3-37
2N2160		2N4853	3-43
2N2322	2N2323		3-14
2N2323	2N2323		3-14
2N2324	2N2324		3-14
2N2325	2N2326		3-14
2N2326	2N2326		3-14
2N2327	2N2329		3-14
2N2328	2N2329		3-14
2N2329	2N2329		3-14
2N2344		MCR1906-2	3-261
2N2345		MCR1906-2	3-261
2N2346		MCR1906-3	3-261
2N2347		MCR1906-4	3-261
2N2348		MCR1906-4	3-261
2N2573	2N2574		3-16
2N2574	2N2574		3-16
2N2575	2N2575		3-16
2N2576	2N2576		3-16
2N2577	2N2578		3-16
2N2578	2N2578		3-16
2N2579	MCR649AP8		—
2N2619		2N4174	3-27
2N2646	2N2646		3-19
2N2647	2N2647		3-19
2N2653		2N4172	3-27
2N2679		MCR102	3-230
2N2680		MCR103	3-230
2N2681		MCR100-3	3-228
2N2682		MCR100-4	3-228
2N2683		MCR102	3-230
2N2684		MCR103	3-230
2N2685		MCR100-3	3-228
2N2686		MCR100-4	3-228
2N2687		MCR102	3-230
2N2688		MCR103	3-230
2N2689		MCR100-3	3-228
2N2690		MCR100-4	3-228
2N2888		2N1846	3-8
2N2889		2N1849	3-8
2N3001		MCR102	3-230
2N3002		MCR103	3-230
2N3003		MCR100-3	3-228
2N3004		MCR100-4	3-228
2N3005		MCR102	3-230
2N3006		MCR103	3-230
2N3007		MCR100-3	3-228
2N3008		MCR100-4	3-228
2N3027		MCR102	3-230
2N3028		MCR103	3-230
2N3029		MCR100-3	3-228
2N3030		MCR102	3-230
2N3031		MCR103	3-230
2N3032		MCR100-3	3-228
2N3228		S2800B	3-305
2N3254		MCR102	3-230
2N3255		MCR102	3-230
2N3256		MCR103	3-230
2N3257		MCR102	3-230
2N3258		MCR102	3-230
2N3259		MCR103	3-230
2N3269		2N4169	3-27

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N3270		2N4170	3-27
2N3271		2N4172	3-27
2N3272		2N4172	3-27
2N3273		2N2324	3-14
2N3274		2N2326	3-14
2N3275		2N2329	3-14
2N3276		2N2329	3-14
2N3525		S2800D	3-305
2N3528		S2800B	3-305
2N3529		S2800D	3-305
2N3555		2N4213	3-37
2N3556		2N4213	3-37
2N3557		2N4214	3-37
2N3558		2N4216	3-37
2N3559		2N4213	3-37
2N3560		2N4213	3-37
2N3561		2N4214	3-37
2N3562		2N4216	3-37
2N3644		2N1843	3-11
2N3650		2N1844	3-11
2N3651		2N1846	3-11
2N3652		2N1849	3-11
2N3653		2N1849	3-11
2N3654		2N1843	3-11
2N3655		2N1844	3-11
2N3656		2N1846	3-11
2N3657		2N1849	3-11
2N3658		2N1849	3-11
2N3668		MCR649AP4	—
2N3669		MCR649AP4	—
2N3670		MCR649AP6	—
2N3870	2N3870		3-21
2N3871	2N3871		3-21
2N3872	2N3872		3-21
2N3873	2N3873		3-21
2N3896	2N3896		3-21
2N3897	2N3897		3-21
2N3898	2N3898		3-21
2N3899	2N3899		3-21
2N3936		2N4169	3-27
2N3937		2N4170	3-27
2N3938		2N4172	3-27
2N3939		2N4172	3-27
2N3940		2N4174	3-27
2N3980	2N3980		3-25
2N4096		MCR103	3-230
2N4097		MCR100-3	3-228
2N4098		MCR100-4	3-228
2N4101		S2800M	3-305
2N4102		S2800M	3-305
2N4103		MCR649AP8	—
2N4108		MCR103	3-230
2N4109		MCR100-3	3-228
2N4110		MCR100-4	3-228
2N4144		MCR102	3-230
2N4145		MCR102	3-230
2N4146		MCR102	3-230
2N4147		MCR103	3-230
2N4148		MCR100-3	3-228
2N4149		MCR100-4	3-228
2N4167	2N4168		3-27
2N4168	2N4168		3-27
2N4169	2N4169		3-27
2N4170	2N4170		3-27
2N4171	2N4172		3-27
2N4172	2N4172		3-27
2N4173	2N4174		3-27
2N4174	2N4174		3-27
2N4183	2N4184		3-27

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N4184	2N4184		3-27
2N4185	2N4185		3-27
2N4186	2N4186		3-27
2N4187	2N4188		3-27
2N4188	2N4188		3-27
2N4189	2N4190		3-27
2N4190	2N4190		3-27
2N4199	2N4199		3-31
2N4199JAN	2N4199JAN		3-31
2N4200	2N4200		3-31
2N4200JAN	2N4200JAN		3-31
2N4201	2N4201		3-31
2N4201JAN	2N4201JAN		3-31
2N4202	2N4202		3-31
2N4202JAN	2N4202JAN		3-31
2N4203	2N4203		3-31
2N4203JAN	2N4203JAN		3-31
2N4204	2N4204		3-31
2N4204JAN	2N4204JAN		3-31
2N4212	2N4213		3-37
2N4213	2N4213		3-37
2N4214	2N4214		3-37
2N4215	2N4215		3-37
2N4216	2N4216		3-37
2N4217	2N4219		3-37
2N4218	2N4219		3-37
2N4219	2N4219		3-37
2N4332		MCR102	3-230
2N4333		MCR103	3-230
2N4334		MCR100-3	3-228
2N4335		MCR100-4	3-228
2N4336		MCR100-4	3-228
2N4441	2N4441		3-39
2N4442	2N4442		3-39
2N4443	2N4443		3-39
2N4444	2N4444		3-39
2N4851	2N4851		3-43
2N4852	2N4852		3-43
2N4853	2N4853		3-43
2N4870	2N4870		3-48
2N4871	2N4871		3-48
2N4891		MU4891	3-303
2N4892		MU4892	3-303
2N4893		MU4893	3-303
2N4894		MU4894	3-303
2N4948	2N4948		3-53
2N4949	2N4949		3-53
2N4991		MBS4991	3-207
2N4992		MBS4992	3-207
2N4993		MBS4991	3-207
2N5060	2N5060		3-55
2N5061	2N5061		3-55
2N5062	2N5062		3-55
2N5063	2N5063		3-55
2N5064	2N5064		3-55
2N5164	2N5164		3-59
2N5165	2N5165		3-59
2N5166	2N5166		3-59
2N5167	2N5167		3-59
2N5168	2N5168		3-59
2N5169	2N5169		3-59
2N5170	2N5170		3-59
2N5171	2N5171		3-59
2N5204		2N3899	3-21
2N5205		MCR3935-10	3-268
2N5273		2N6160	3-92
2N5274		2N6161	3-92
2N5275		2N6162	3-92
2N5431	2N5431		3-64
2N5441	2N5441		3-67

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N5442	2N5442		3-67
2N5443	2N5443		3-67
2N5444	2N5444		3-67
2N5445	2N5445		3-67
2N5446	2N5446		3-67
2N5567	2N5567		3-71
2N5568	2N5568		3-71
2N5569	2N5569		3-71
2N5570	2N5570		3-71
2N5571	2N5571		3-75
2N5572	2N5572		3-75
2N5573	2N5573		3-75
2N5574	2N5574		3-75
2N5719		MCR103	3-230
2N5720		MCR100-3	3-228
2N5721		MCR100-4	3-228
2N5722		MCR100-6	3-228
2N5723		MCR100-6	3-228
2N5724		MCR103	3-230
2N5725		MCR100-3	3-228
2N5726		MCR100-4	3-228
2N5727		MCR100-6	3-228
2N5728		MCR100-6	3-228
2N5754		2N6070	—
2N5755		2N6071	3-83
2N5756		2N6073	3-83
2N5757		2N6073	3-83
2N5806		2N6160	3-92
2N5807		2N6161	3-92
2N5808		2N6162	3-92
2N5809		2N6162	3-92
2N6027	2N6027		3-79
2N6028	2N6028		3-79
2N6068	2N6071		3-83
2N6068A	2N6071A		3-83
2N6068B	2N6071B		3-83
2N6069	2N6071		3-83
2N6069A	2N6071A		3-83
2N6069B	2N6071B		3-83
2N6070	2N6071		3-83
2N6070A	2N6071A		3-83
2N6070B	2N6071B		3-83
2N6071	2N6071		3-83
2N6071A	2N6071A		3-83
2N6071B	2N6071B		3-83
2N6072	2N6072		3-83
2N6072A	2N6072A		3-83
2N6072B	2N6072B		3-83
2N6073	2N6073		3-83
2N6073A	2N6073A		3-83
2N6073B	2N6073B		3-83
2N6074	2N6074		3-83
2N6074A	2N6074A		3-83
2N6074B	2N6074B		3-83
2N6075	2N6075		3-83
2N6075A	2N6075A		3-83
2N6075B	2N6075B		3-83
2N6116	2N6116		3-88
2N6117	2N6117		3-88
2N6118	2N6118		3-88
2N6137		2N6116	3-88
2N6138		2N6116	3-88
2N6145	2N6145		3-75
2N6146	2N6146		3-75
2N6147	2N6147		3-75
2N6151		MAC210A4	3-153
2N6152		MAC210A6	3-153
2N6153		MAC210A8	3-153
2N6154		MAC210A4	3-153
2N6155		MAC210A6	3-153

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N6156		MAC210A8	3-153
2N6157	2N6157		3-92
2N6158	2N6158		3-92
2N6159	2N6159		3-92
2N6160	2N6160		3-92
2N6161	2N6161		3-92
2N6162	2N6162		3-92
2N6163	2N6163		3-92
2N6164	2N6164		3-92
2N6165	2N6165		3-92
2N6167	2N6167		3-96
2N6168	2N6168		3-96
2N6169	2N6169		3-96
2N6170	2N6170		3-96
2N6171	2N6171		–
2N6172	2N6172		–
2N6173	2N6173		–
2N6174	2N6174		–
2N6236	2N6237		3-100
2N6237	2N6237		3-100
2N6238	2N6238		3-100
2N6239	2N6239		3-100
2N6240	2N6240		3-100
2N6241	2N6241		3-100
2N6332		2N6237	3-100
2N6333		2N6237	3-100
2N6334		2N6238	3-100
2N6335		2N6239	3-100
2N6336		2N6240	3-100
2N6337		2N6240	3-100
2N6342	2N5342		3-103
2N6342A	2N6342A		3-107
2N6343	2N6343		3-103
2N6343A	2N6343A		3-107
2N6344	2N6344		3-103
2N6344A	2N6344A		3-107
2N6345	2N6345		3-103
2N6345A	2N6345A		3-107
2N6346	2N6346		3-103
2N6346A	2N6346A		3-107
2N6347	2N6347		3-103
2N6347A	2N6347A		3-107
2N6348	2N6348		3-103
2N6348A	2N6348A		3-107
2N6349	2N6349		3-103
2N6349A	2N6349A		3-107
2N6394	2N6394		3-111
2N6395	2N6395		3-111
2N6396	2N6396		3-111
2N6397	2N6397		3-111
2N6398	2N6398		3-111
2N6399	2N6399		3-111
2N6400	2N6400		3-115
2N6401	2N6401		3-115
2N6402	2N6402		3-115
2N6403	2N6403		3-115
2N6404	2N6404		3-115
2N6405	2N6405		3-115
2N6504	2N6504		3-119
2N6505	2N6505		3-119
2N6506	2N6506		3-119
2N6507	2N6507		3-119
2N6508	2N6508		3-119
2N6509	2N6509		3-119
2N6605		2N1595	3-6
2N6606		2N1595	3-6
2N6607		2N1596	3-6
2N6608		2N1597	3-6
10RIA10	2N1844		3-8
10RIA20	2N1846		3-8

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
10RIA40	2N1849		3-8
10RIA60	2N5171		3-59
10RIA80	2N692		3-2
10RIA10	2N683		3-2
16RIA20	2N685		3-2
16RIA40	2N688		3-2
16RIA60	2N690		3-2
16RIA80	2N692		3-2
50RIA10	MCR64-3		3-215
50RIA20	MCR64-4		3-215
50RIA40	MCR64-6		3-215
50RIA60	MCR64-8		3-215
50RIA80	MCR64-10		3-215
BRX44	BRX44		3-123
BRX45	BRX45		–
BRX46	BRX46		–
BRX47	BRX47		–
BRX49	BRX49		–
BRY55-30	BRY55-30		3-125
BRY55-60	BRY55-60		–
BRY55-100	BRY55-100		–
BRY55-200	BRY55-200		–
BRY55-300	BRY55-400		–
BRY55M-300	BRY55-400		–
BRY55-400	BRY55-400		–
BRY55M-400	BRY55-400		–
BRY55-500	BRY55-500		–
BRY55-600	BRY55-600		–
BRY55M-600	BRY55-600		–
BR136-500D		2N6074A	3-83
BT136-500D		2N6074A	3-83
BT137-500	MAC218A8	3-169	
BT137-500E		MAC228A8	3-184
BT137-500F		T2800M	3-322
BT137-500G		MAC228A8	3-184
BT137-600		MAC222A8	–
BT137-600E		MAC228A8	3-184
BT137-600F		T2800M	3-322
BT137-600G		MAC228A8	3-184
BT137-800		MAC222A10	–
BT137-800E		MAC228A10	3-184
BT137-800G		MAC228A10	3-184
BT138-500G		2N6348A	3-107
BT138-600G		2N6348A	3-107
BT138-800G		2N6349A	3-107
BT151-500R		2N6398	3-111
BT151-650R		2N6399	3-111
BT151-800A		2N6399	3-111
BTA20C	T2801D		3-324
BTA20D	T2801D		3-324
BTA20E	T2801D		3-324
BTA21C		T2802D	–
BTA21D		T2802D	–
BTA21E		T2802M	–
BTA22B		SC146B	3-309
BTA22C		SC146D	3-309
BTA22D		SC146D	3-309
BTA22E		SC146M	3-309
BTA22M		SC146M	3-309
BTA23B		2N6346A	3-307
BTA23C		2N6347A	3-307
BTA23D		2N6347A	3-307
BTA23E		2N6348A	3-307
BTA23M		2N6348A	3-307
BTA25-200		MAC25A4	3-146
BTA25-400		MAC25A6	3-146
BTA25-600		MAC25A8	3-146
BTA25-700		MAC25A-10	3-146
BTA40-200		MAC50A4	3-146
BTA40-400		MAC50A6	3-146
BTA40-600		MAC50A8	3-146

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
BTA40-700		MAC50A10	3-146
BTB06-200B		SC141B	3-309
BTB06-400B		SC141D	3-309
BTB06-700B		SC141N	3-309
BTB08-200B		MAC218A4	3-169
BTB08-200S		MAC228A4	3-169
BTB08-400B		MAC218A6	3-169
BTB08-400S		MAC228A6	3-169
BTB08-700B		MAC218A10	3-169
BTB08-700S		MAC228A10	3-184
BTB10-200B		SC146B	3-309
BTB10-400B		SC146D	3-309
BTB10-700B		SC146N	3-309
BTW39-50		C230F	3-135
BTW39-100		C230A	3-135
BTW39-200		C230B	3-135
BTW39-300		C230D	3-135
BTW39-400		C230D	3-135
BTW39-500		C230M	3-135
BTW39-600		C230M	3-135
BTW48-200		MCR64-4	3-215
BTW48-400		MCR64-6	3-215
BTW48-600		MCR64-8	3-215
BTW48-800		MCR64-10	3-215
BTW66-200N		MCR25-4	—
BTW66-400N		MCR25-6	—
BTW66-600N		MCR25-8	—
BTW66-800N		MCR25-10	—
C5A	2N2324		3-14
C5B	2N2326		3-14
C5F	2N2323		3-14
C5G	2N2326		3-14
C5U	2N2323		3-14
C6A		MCR1906-3	3-261
C6B		MCR1906-4	3-261
C6F		MCR1906-2	3-261
C6G		MCR1906-4	3-261
C6U		MCR1906-2	3-261
C7A		MCR1906-3	3-261
C7B		MCR1906-4	3-261
C7G		MCR1906-4	3-261
C7U		MCR1906-2	3-261
C10A		2N4169	3-27
C10B		2N4170	3-27
C10F		2N4168	3-27
C10G		2N4170	3-27
C10V		2N4168	3-27
C11A		2N4169	3-27
C11B		2N4170	3-27
C11C		2N4172	3-27
C11D		2N4172	3-27
C11E		2N4174	3-27
C11F		2N4168	3-27
C11G		2N4170	3-27
C11H		2N4172	3-27
C11M		2N4174	3-27
C11U		2N4168	3-27
C15A		2N4169	3-27
C15B		2N4170	3-27
C15C		2N4172	3-27
C15D		2N4172	3-27
C15F		2N4168	3-27
C15G		2N4170	3-27
C15H		2N4172	3-27
C15M		2N4174	3-27
C20A		2N4169	3-27
C20B		2N4170	3-27
C20C		2N4172	3-27
C20D		2N4172	3-27
C20F		2N4168	3-27

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
C20U		2N4168	3-27
C30A		2N683	3-2
C30B		2N685	3-2
C30C		2N688	3-2
C30D		2N688	3-2
C30F		2N682	3-2
C30U		2N682	3-2
C31A		2N683	3-2
C31B		2N685	3-2
C31C		2N688	3-2
C31D		2N688	3-2
C31F		2N682	3-2
C31U		2N682	3-2
C32A		2N683	3-2
C32B		2N685	3-2
C32C		2N688	3-2
C32D		2N688	3-2
C32F		2N682	3-2
C32U		2N682	3-2
C33A		MCR3818-3	3-263
C33B		2N5165	3-59
C33C		MCR3818-6	3-263
C33D		2N5166	3-59
C33F		2N5164	3-59
C33U		MCR3818-2	3-263
C35A	C35A		3-123
C35B	C35B		3-123
C35C	C35D		3-123
C35D	C35D		3-123
C35E	C35M		3-123
C35F	C35F		3-123
C35G	C35B		3-123
C35H	C35D		3-123
C35M	C35M		3-123
C35N	C35N		3-123
C35S	C35N		3-123
C35U	C35F		3-123
C36A	2N1844		3-8
C36B	2N1846		3-8
C36C	2N1849		3-8
C36D	2N1849		3-8
C36E	2N5171		3-59
C36F	2N1843		3-8
C36G	2N1846		3-8
C36H	2N1849		3-8
C36U	2N1843		3-8
C37A		MCR3918-3	3-263
C37B		2N5169	3-59
C37C		MCR3918-6	3-263
C37D		2N5170	3-59
C37E		MCR3918-8	3-263
C37F		2N5168	3-59
C37G		2N5169	3-59
C37H		MCR3918-6	3-263
C37M		2N5171	3-59
C37U		MCR3918-2	3-263
C38A		2N3896	3-21
C38B		2N3897	3-21
C38C		MCR3935-6	3-268
C38D		2N3898	3-21
C38E		MCR3935-8	3-268
C38F		MCR3935-2	3-268
C38G		2N3897	3-21
C38H		MCR3935-6	3-268
C38U		MCR3935-2	3-268
C103A		2N5062	3-55
C103B		2N5064	3-55
C103Y		2N5060	3-55
C103YY		2N5061	3-55
C106A	C106A		3-125

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
C106A1	C106A1		3-125
C106B	C106B		3-125
C106B1	C106B1		3-125
C106C	C106D		3-125
C106C1	C106D1		3-125
C106D	C106D		3-125
C106D1	C106D1		3-125
C106E	C106M		3-125
C106E1	C106M1		3-125
C106F	C106F		3-125
C106F1	C106F1		3-125
C106M	C106M		3-125
C106M1	C106M1		3-125
C106Q	C106F		3-125
C106Y	C106F		3-125
C106Y1	C106F1		3-125
C107A		C106A	3-125
C107B		C106B	3-125
C107C		C106D	3-125
C107D		C106D	3-125
C107E		C106M	3-125
C107F		C106F	3-125
C107M		C106M	3-125
C107Q		C106B	3-125
C107Y		C106F	3-125
C122A1	C122A1		3-128
C122B1	C122B1		3-128
C122C1	C122D1		3-128
C122D1	C122D1		3-128
C122E1	C122M1		3-128
C122F1	C122F1		3-128
C122M1	C122M1		3-128
C122N1	C122N1		3-128
C122S1	C122N1		3-128
C126A		2N6395	3-111
C126B		2N6396	3-111
C126C		2N6397	3-111
C126D		2N6397	3-111
C126E		2N6398	3-111
C126F		2N6394	3-111
C126M		2N6398	3-111
C127A		2N6401	3-115
C127B		2N6402	3-115
C127C		2N6403	3-115
C127D		2N6403	3-115
C127E		2N6404	3-115
C127F		2N6400	3-115
C127M		2N6404	3-115
C135A		2N3896	3-21
C135B		2N3897	3-21
C135C		2N3898	3-21
C135D		2N3898	3-21
C135E		MCR3935-8	3-268
C135F		MCR3935-2	3-268
C135M		2N3899	3-21
C137E		MCR3935-8	3-268
C137M		2N3899	3-21
C137N		MCR3935-10	3-268
C137S		MCR3935-10	3-268
C205A	C205A		3-131
C205B	C205B		3-131
C205C	C205D		3-131
C205D	C205D		3-131
C205Y	C205Y		3-131
C205YY	C205YY		3-131
C228A	C228A		3-133
C228A3	C228A3		3-133
C228B	C228B		3-133
C228B3	C228B3		3-133
C228C	C228D		3-133

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
C228C3	C228D3		3-133
C228D	C228D		3-133
C228D3	C228D3		3-133
C228E	C228M		3-133
C228E3	C228M3		3-133
C228F	C228A		3-133
C228F3	C228A3		3-133
C228M	C228M		3-133
C228M3	C228M3		3-133
C229A	C229A		3-133
C229A3	C228A3		3-133
C229B	C229B		3-133
C229B3	C228B3		3-133
C229C	C229D		3-133
C229C3	C228D3		3-133
C229D	C229D		3-133
C229D3	C228D3		3-133
C229E	C229M		3-133
C229E3	C228M3		3-133
C229F	C229A		3-133
C229F3	C228A3		3-133
C229M	C229M		3-133
C229M3	C228M3		3-133
C230A	C230A		3-135
C230A3	C230A3		3-135
C230B	C230B		3-135
C230B3	C230B3		3-135
C230C	C230D		3-135
C230C3	C230D3		3-135
C230D	C230D		3-135
C230D3	C230D3		3-135
C230E	C230M		3-135
C230E3	C230M3		3-135
C230F	C230F		3-135
C230F3	C230F3		3-135
C230M	C230M		3-135
C230M3	C230M3		3-135
C231A	C231A		3-135
C231A3	C231A3		3-135
C231B	C231B		3-135
C231B3	C231B3		3-135
C231C	C231D		3-135
C231C3	C231D3		3-135
C231D	C231D		3-135
C231D3	C231D3		3-135
C231E	C231M		3-135
C231E3	C231M3		3-135
C231F	C231F		3-135
C231F3	C231F3		3-135
C231M	C231M		3-135
C231M3	C231M3		3-135
C232A	C232A		3-135
C232B	C232B		3-135
C232C	C232D		3-135
C232D	C232D		3-135
C232E	C232M		3-135
C232F	C232F		3-135
C232M	C232M		3-135
C233A	C233A		3-135
C233B	C233B		3-135
C233C	C233D		3-135
C233D	C233D		3-135
C233E	C233M		3-135
C233F	C233F		3-135
C233M	C233M		3-135
CS72-3	CS72-3		—
CS72-4	CS72-4		—
CS72-5	CS72-6		—
CS72-6	CS72-6		—

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
CS72-7	CS72-8		—
CS72-8	CS72-8		—
CS122A	CS122A		—
CS122B	CS122B		—
CS122C	CS122D		—
CS122D	CS122D		—
CS122E	CS122M		—
CS122M	CS122M		—
CS122N	CS122N		—
CS122S	CS122N		—
CS220-5	CS6397		—
CS220-7	CS6398		—
CS220-9	CS6399		—
CS221-5	CS6403		—
CS221-7	CS6404		—
CS221-9	CS6405		—
D13Q500		MBS4991	3-207
D13T1	2N6027		3-79
D13T2	2N6028		3-79
D30		MBS4991	3-207
D3202U		MBS4991	3-207
D3202Y		MBS4991	3-207
EC103A		2N5062	3-55
EC103A1		MCR22-3	3-211
EC103A2		MCR22-3	3-211
EC103A3		MCR22-3	3-211
EC103B		MCR100-4	3-228
EC103B1		MCR22-4	3-211
EC103B2		MCR22-4	3-211
EC103B3		MCR22-4	3-211
EC103C	MCR100-6		3-228
EC103C1		MCR22-6	3-211
EC103C2		MCR22-6	3-211
EC103C3		MCR22-6	3-211
EC103D	MCR100-6		3-228
EC103D1		MCR22-6	3-211
EC103D2		MCR22-6	3-211
EC103D3		MCR22-6	3-211
EC103E		MCR22-8	3-211
EC103E1		MCR22-8	3-211
EC103E2		MCR22-8	3-211
EC103E3		MCR22-8	3-211
EC103M		MCR22-8	3-211
EC103M1		MCR22-8	3-211
EC103M2		MCR22-8	3-211
EC103M3		MCR22-8	3-211
EC103Y	MCR102		3-230
EC103Y1		MCR22-2	3-211
EC103Y2		MCR22-2	3-211
EC103Y3		MCR22-2	3-211
F0810BH		MCR218-4	3-239
F0810DH		MCR218-6	3-239
F0810MH		MCR218-8	3-239
F0810NH		MCR218-10	3-239
F1612BH		2N6402	3-115
F1612DH		2N6403	3-115
F1612MH		2N6404	3-115
F1612NH		2N6405	3-115
GT32		MBS4991	3-207
GT35		MBS4991	3-207
HT32		MBS4991	3-207
HT35		MBS4991	3-207
HT40		MBS4991	3-207
K1100E		MK1V115	3-279
K1200E		MK1V125	3-279
K1300E		MK1V135	3-279
K2200E		MK1V240	3-282
K2400E		MK1V240	3-282
KIV11		MK1V115	3-279
KIV12		MK1V125	3-279

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
KIV22		MK1V240	3-282
KIV24		MK1V240	3-282
KIV26		MK1V260	3-282
L200E3		MAC97B4	3-149
L200E5		MAC97A4	3-149
L200E7		MAC97-4	3-149
L200E9		MAC97-4	3-149
L400E3		MAC97B6	3-149
L400E5		MAC97A6	3-149
L400E7		MAC97-6	3-149
L400E9		MAC97-6	3-149
L2001F51		2N6071B	3-83
L2001F71		2N6071A	3-83
L2001F91		2N6071	3-83
L2001L3		2N6071A	3-83
L2001L5		T2322B	3-316
L2001L7		T2322B	3-316
L2001L9		T2322B	3-316
L2001M3		2N6071A	3-83
L2001M5		2N6071B	3-83
L2001M7		2N6071A	3-83
L2001M9		2N6071	3-83
L2003M3		2N6071A	3-83
L2003M5		2N6071B	3-83
L2003M7		2N6071A	3-83
L2003M9		2N6071	3-83
L2004F31		2N6071B	3-83
L2004F51		2N6071A	3-83
L2004F71		2N6071	3-83
L2004F91		2N6071	3-83
L2004L3		2N6071B	3-83
L2004L5		2N6071A	3-83
L2004L7		2N6071A	3-83
L2004L9		2N6071A	3-83
L2006L6		MAC228A4	3-184
L2006L7		MAC228A4	3-184
L2006L9		MAC218A4	3-169
L2008L6		MAC228A4	3-184
L2008L7		MAC228A4	3-184
L2008L9		MAC228A4	3-184
L4001F51		2N6073B	3-83
L4001F71		2N6073A	3-83
L4001F91		2N6073	3-83
L4001L7		T2322D	3-316
L4001L9		T2322D	3-316
L4001M5		2N6073B	3-83
L4001M7		2N6073A	3-83
L4001M9		2N6073	3-83
L4003M5		2N6073B	3-83
L4003M7		2N6073A	3-83
L4003M9		2N6073	3-83
L4004F31		2N6073B	3-83
L4004F51		2N6073A	3-83
L4004F71		2N6073	3-83
L4004F91		2N6073	3-83
L4004L3		2N6073B	3-83
L4004L5		2N6073A	3-83
L4004L7		2N6073A	3-83
L4004L9		2N6073A	3-83
L4006L6		MAC228A6	3-184
L4006L7		MAC228A6	3-184
L4006L9		MAC228A6	3-184
L4008L6		MAC228A6	3-184
L4008L7		MAC228A6	3-184
L4008L9		MAC228A6	3-184
M1713DP		2N5170	3-59
M1713MP		2N5171	3-59
M2513DP		2N688	3-2
M2513MP		2N690	3-2

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
M2513NP		2N692	3-2
M3013DP		C228D	3-133
M3013MP		C228M	3-133
M4013NP		MCR64-10	3-215
MAC10-4	MAC210A4		3-153
MAC10-6	MAC210A6		3-153
MAC10-8	MAC210A8		3-153
MAC11-4	MAC210A4		3-153
MAC11-6	MAC210A6		3-153
MAC11-8	MAC210A8		3-153
MAC15-4	MAC15A4		3-138
MAC15A4	MAC15A4		3-138
MAC15A4FP	MAC15A4FP		3-142
MAC15-5	MAC15A6		3-138
MAC15A5	MAC15A6		3-138
MAC15-6	MAC15A6		3-138
MAC15A6	MAC15A6		3-138
MAC15A6FP	MAC15A6FP		3-142
MAC15-7	MAC15A8		3-138
MAC15A7	MAC15A8		3-138
MAC15-8	MAC15A8		3-138
MAC15A8	MAC15A8		3-138
MAC15A8FP	MAC15A8FP		3-142
MAC15-9	MAC15A10		3-138
MAC15A9	MAC15A10		3-138
MAC15-10	MAC15A10		3-138
MAC15A10	MAC15A10		3-138
MAC15A10FP	MAC15A10FP		3-142
MAC20-4	MAC20A4		3-146
MAC20A4	MAC20A4		3-146
MAC20-5	MAC20A6		3-146
MAC20A5	MAC20A6		3-146
MAC20-6	MAC20A6		3-146
MAC20A6	MAC20A6		3-146
MAC20-7	MAC20A8		3-146
MAC20A7	MAC20A8		3-146
MAC20-8	MAC20A8		3-146
MAC20A8	MAC20A8		3-146
MAC20-9	MAC20A10		3-146
MAC20A9	MAC20A10		3-146
MAC20-10	MAC20A10		3-146
MAC20A10	MAC20A10		3-146
MAC25-4	MAC25A4		3-146
MAC25A4	MAC25A4		3-146
MAC25-5	MAC25A6		3-146
MAC25A5	MAC25A6		3-146
MAC25-6	MAC25A6		3-146
MAC25A6	MAC25A6		3-146
MAC25-7	MAC25A8		3-146
MAC25A7	MAC25A8		3-146
MAC25-8	MAC25A8		3-146
MAC25A8	MAC25A8		3-146
MAC25-9	MAC25A10		3-146
MAC25A9	MAC25A10		3-146
MAC25-10	MAC25A10		3-146
MAC25A10	MAC25A10		3-146
MAC35-1	2N6157		3-92
MAC35-2	2N6157		3-92
MAC35-3	2N6157		3-92
MAC35-4	2N6157		3-92
MAC35-5	2N6158		3-92
MAC35-6	2N6158		3-92
MAC35-7	2N6159		3-92
MAC35-8	2N6159		3-92
MAC36-1	2N6160		3-92
MAC36-2	2N6160		3-92
MAC36-3	2N6160		3-92
MAC36-4	2N6160		3-92
MAC36-5	2N6161		3-92
MAC36-6	2N6161		3-92

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MAC36-7	2N6162		3-92
MAC36-8	2N6162		3-92
MAC37-1	2N6157		3-92
MAC37-2	2N6157		3-92
MAC37-3	2N6157		3-92
MAC37-4	2N6157		3-92
MAC37-5	2N6158		3-92
MAC37-6	2N6158		3-92
MAC37-7	2N6159		3-92
MAC37-8	2N6159		3-92
MAC38-1	2N6160		3-92
MAC38-2	2N6160		3-92
MAC38-3	2N6160		3-92
MAC38-4	2N6160		3-92
MAC38-5	2N6161		3-92
MAC38-6	2N6161		3-92
MAC38-7	2N6162		3-92
MAC38-8	2N6162		3-92
MAC50-4	MAC50A4		3-146
MAC50A4	MAC50A4		3-146
MAC50-5	MAC50A6		3-146
MAC50A5	MAC50A6		3-146
MAC50-6	MAC50A6		3-146
MAC50A6	MAC50A6		3-146
MAC50-7	MAC50A8		3-146
MAC50A7	MAC50A8		3-146
MAC50-8	MAC50A8		3-146
MAC50A8	MAC50A8		3-146
MAC50-9	MAC50A10		3-146
MAC50A9	MAC50A10		3-146
MAC50-10	MAC50A10		3-146
MAC50A10	MAC50A10		3-146
MAC77-2	2N6071		3-83
MAC77-3	2N6071		3-83
MAC77-4	2N6071		3-83
MAC77-5	2N6072		3-83
MAC77-6	2N6073		3-83
MAC77-7	2N6074		3-83
MAC77-8	2N6075		3-83
MAC91-1	MAC97-4		3-149
MAC91A1	MAC97A4		3-149
MAC91-2	MAC97-4		3-149
MAC91A2	MAC97A4		3-149
MAC91-3	MAC97-4		3-149
MAC91A3	MAC97A4		3-149
MAC91-4	MAC97-4		3-149
MAC91A4	MAC97A4		3-149
MAC91-5	MAC97-6		3-149
MAC91A5	MAC97A6		3-149
MAC91-6	MAC97-6		3-149
MAC91A6	MAC97A6		3-149
MAC91-7	MAC97-8		3-149
MAC91A7	MAC97A8		3-149
MAC91-8	MAC97-8		3-149
MAC91A8	MAC97A8		3-149
MAC92-1	MAC97A4		3-149
MAC92A1		MAC97A4	3-149
MAC92-2	MAC97A4		3-149
MAC92A2		MAC97A4	3-149
MAC92-3	MAC97A4		3-149
MAC92A3		MAC97A4	3-149
MAC92-4	MAC97A4		3-149
MAC92A4		MAC97A4	3-149
MAC92-5	MAC97A6		3-149
MAC92A5		MAC97A6	3-149
MAC92-6	MAC97A6		3-149
MAC92A6		MAC97A6	3-149
MAC92-7	MAC97A8		3-149
MAC92A7		MAC97A8	3-149

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MAC92-8	MAC97A8		3-149
MAC92A8		MAC97A8	3-149
MAC93-1	MAC97B4		3-149
MAC93A1		MAC97B4	3-149
MAC93-2	MAC97B4		3-149
MAC93A2		MAC97B4	3-149
MAC93-3	MAC97B4		3-149
MAC93A3		MAC97B4	3-149
MAC93-4	MAC97B4		3-149
MAC93A4		MAC97B4	3-149
MAC93-5	MAC97B6		3-149
MAC93A5		MAC97B6	3-149
MAC93-6	MAC97B6		3-149
MAC93A6		MAC97B6	3-149
MAC93-7	MAC97B8		3-149
MAC93A7		MAC97B8	3-149
MAC93-8	MAC97B8		3-149
MAC93A8		MAC97B8	3-149
MAC94-1		MAC97-4	3-149
MAC94A1		MAC97-4	3-149
MAC94-2		MAC97-4	3-149
MAC94A2		MAC97-4	3-149
MAC94-3		MAC97-4	3-149
MAC94A3		MAC97-4	3-149
MAC94-4		MAC97-4	3-149
MAC94A4		MAC97-4	3-149
MAC94-5		MAC97-6	3-149
MAC94A5		MAC97-6	3-149
MAC94-6		MAC97-6	3-149
MAC94A6		MAC97-6	3-149
MAC94-7		MAC97-8	3-149
MAC94A7		MAC97-8	3-149
MAC94-8		MAC97-8	3-149
MAC94A8		MAC97-8	3-149
MAC95-1		MAC97A4	3-149
MAC95A1		MAC97A4	3-149
MAC95-2		MAC97A4	3-149
MAC95A2		MAC97A4	3-149
MAC95-3		MAC97A4	3-149
MAC95A3		MAC97A4	3-149
MAC95-4		MAC97A4	3-149
MAC95A4		MAC97A4	3-149
MAC95-5		MAC97A6	3-149
MAC95A5		MAC97A6	3-149
MAC95-6		MAC97A6	3-149
MAC95A6		MAC97A6	3-149
MAC95-7		MAC97A8	3-149
MAC95A7		MAC97A8	3-149
MAC95-8		MAC97A8	3-149
MAC95A8		MAC97A8	3-149
MAC96-1		MAC97B4	3-149
MAC96A1		MAC97B4	3-149
MAC96-2		MAC97B4	3-149
MAC96A2		MAC97B4	3-149
MAC96-3		MAC97B4	3-149
MAC96A3		MAC97B4	3-149
MAC96-4		MAC97B4	3-149
MAC96A4		MAC97B4	3-149
MAC96-5		MAC97B6	3-149
MAC96A5		MAC97B6	3-149
MAC96-6		MAC97B6	3-149
MAC96A6		MAC97B6	3-149
MAC96-7		MAC97B8	3-149
MAC96A7		MAC97B8	3-149
MAC96-8		MAC97B8	3-149
MAC96A8		MAC97B8	3-149
MAC97-1	MAC97-4		3-149
MAC97A1	MAC97A4		3-149
MAC97B1	MAC97B4		3-149
MAC97-2	MAC97-4		3-149

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MAC97A2	MAC97A4		3-149
MAC97B2	MAC97B4		3-149
MAC97-3	MAC97-4		3-149
MAC97A3	MAC97A4		3-149
MAC97B3	MAC97B4		3-149
MAC97-4	MAC97-4		3-149
MAC97A4	MAC97A4		3-149
MAC97B4	MAC97B4		3-149
MAC97-5	MAC97-6		3-149
MAC97A5	MAC97A6		3-149
MAC97B5	MAC97B6		3-149
MAC97-6	MAC97-6		3-149
MAC97A6	MAC97A6		3-149
MAC97B6	MAC97B6		3-149
MAC97-7	MAC97-8		3-149
MAC97A7	MAC97A8		3-149
MAC97B7	MAC97B8		3-149
MAC97-8	MAC97-8		3-149
MAC97A8	MAC97A8		3-149
MAC97B8	MAC97B8		3-149
MAC210-4	MAC210A4		3-153
MAC210A4	MAC210A4		3-153
MAC210A4FP	MAC210A4FP		3-157
MAC210-5	MAC210A6		3-153
MAC210A5	MAC210A6		3-153
MAC210-6	MAC210A6		3-153
MAC210A6	MAC210A6		3-153
MAC210A6FP	MAC210A6FP		3-157
MAC210-7	MAC210A8		3-153
MAC210A7	MAC210A8		3-153
MAC210-8	MAC210A8		3-153
MAC210A8	MAC210A8		3-153
MAC210A8FP	MAC210A8FP		3-157
MAC210-9	MAC210A10		3-153
MAC210A9	MAC210A10		3-153
MAC210-10	MAC210A10		3-153
MAC210A10	MAC210A10		3-153
MAC210A10FP	MAC210A10FP		3-157
MAC212-4	MAC212A4		3-161
MAC212-6	MAC212A6		3-161
MAC212-8	MAC212A8		3-161
MAC212-10	MAC212A10		3-161
MAC212A4	MAC212A4		3-161
MAC212A4FP	MAC212A4FP		3-165
MAC212A6	MAC212A6		3-161
MAC212A6FP	MAC212A6FP		3-165
MAC212A8	MAC212A8		3-161
MAC212A8FP	MAC212A8FP		3-165
MAC212A10	MAC212A10		3-161
MAC212A10FP	MAC212A10FP		3-165
MAC218-4	MAC218A4		3-169
MAC218A4	MAC218A4		3-169
MAC218A4FP	MAC218A4FP		3-172
MAC218-5	MAC218A6		3-169
MAC218A5	MAC218A6		3-169
MAC218-6	MAC218A6		3-169
MAC218A6	MAC218A6		3-169
MAC218A6FP	MAC218A6FP		3-172
MAC218-7	MAC218A8		3-169
MAC218A7	MAC218A8		3-169
MAC218-8	MAC218A8		3-169
MAC218A8	MAC218A8		3-169
MAC218A8FP	MAC218A8FP		3-172
MAC218-9	MAC218A10		3-169
MAC218A9	MAC218A10		3-169
MAC218-10	MAC218A10		3-169
MAC218A10	MAC218A10		3-169
MAC218A10FP	MAC218A10FP		3-172
MAC222-2	MAC218A4		3-169
MAC222A1	MAC218A4		3-169

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MAC222A2	MAC218A4		3-169
MAC222-3	MAC218A4		3-169
MAC222A3	MAC218A4		3-169
MAC222-4	MAC218A4		3-169
MAC222A4	MAC218A4		3-169
MAC222-5	MAC218A6		3-169
MAC222A5	MAC218A6		3-169
MAC222-6	MAC218A6		3-169
MAC222A6	MAC218A6		3-169
MAC222-7	MAC218A8		3-169
MAC222A7	MAC218A8		3-169
MAC222-8	MAC218A8		3-169
MAC222A8	MAC218A8		3-169
MAC222-9	MAC218A10		3-169
MAC222A9	MAC218A10		3-169
MAC222-10	MAC218A10		3-169
MAC222A10	MAC218A10		3-169
MAC223-1	MAC223A4		3-175
MAC223A1	MAC223A4		3-175
MAC223-2	MAC223A4		3-175
MAC223A2	MAC223A4		3-175
MAC223-3	MAC223A4		3-175
MAC223A3	MAC223A4		3-175
MAC223-4	MAC223A4		3-175
MAC223A4	MAC223A4		3-175
MAC223A4FP	MAC223A4FP		3-178
MAC223-5	MAC223A6		3-175
MAC223A5	MAC223A6		3-175
MAC223-6	MAC223A6		3-175
MAC223A6	MAC223A6		3-175
MAC223A6FP	MAC223A6FP		3-178
MAC223-7	MAC223A8		3-175
MAC223A7	MAC223A8		3-175
MAC223-8	MAC223A8		3-175
MAC223A8	MAC223A8		3-175
MAC223A8FP	MAC223A8FP		3-178
MAC223-9	MAC223A10		3-175
MAC223A9	MAC223A10		3-175
MAC223-10	MAC223A10		3-175
MAC223A10	MAC223A10		3-175
MAC223A10FP	MAC223A10FP		3-178
MAC224-4	MAC224A4		3-181
MAC224A4	MAC224A4		3-181
MAC224-5	MAC224A6		3-181
MAC224A5	MAC224A6		3-181
MAC224-6	MAC224A6		3-181
MAC224A6	MAC224A6		3-181
MAC224-7	MAC224A8		3-181
MAC224A7	MAC224A8		3-181
MAC224-8	MAC224A8		3-181
MAC224A8	MAC224A8		3-181
MAC224-9	MAC224A10		3-181
MAC224A9	MAC224A10		3-181
MAC224-10	MAC224A10		3-181
MAC224A10	MAC224A10		3-181
MAC228-2	MAC228A4		3-184
MAC228A2	MAC228A4		3-184
MAC228-3	MAC228A4		3-184
MAC228A3	MAC228A4		3-184
MAC228-4	MAC228A4		3-184
MAC228A4	MAC228A4		3-184
MAC228-5	MAC228A6		3-184
MAC228A5	MAC228A6		3-184
MAC228-6	MAC228A6		3-184
MAC228A6	MAC228A6		3-184
MAC228-7	MAC228A8		3-184
MAC228A7	MAC228A8		3-184
MAC228-8	MAC228A8		3-184
MAC228A8	MAC228A8		3-184

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MAC228-9	MAC228A10		3-184
MAC228A9	MAC228A10		3-184
MAC228-10	MAC228A10		3-184
MAC228A10	MAC228A10		3-184
MAC229A4	MAC229A4		3-186
MAC229A6	MAC229A6		3-186
MAC229A8	MAC229A8		3-186
MAC229A10	MAC229A10		3-186
MAC310A4	MAC310A4		3-188
MAC310A6	MAC310A6		3-188
MAC310A8	MAC310A8		3-188
MAC320-4	MAC320A4		3-190
MAC320A4	MAC320A4		3-190
MAC320A4FP	MAC320A4FP		3-194
MAC320-6	MAC320A6		3-190
MAC320A6	MAC320A6		3-190
MAC320A6FP	MAC320A6FP		3-194
MAC320-8	MAC320A8		3-190
MAC320A8	MAC320A8		3-190
MAC320A8FP	MAC320A8FP		3-194
MAC320-10	MAC320A10		3-190
MAC320A10	MAC320A10		3-190
MAC320A10FP	MAC320A10FP		3-194
MAC515-4		MAC20A4	3-146
MAC515A4		MAC20A4	3-146
MAC515-5		MAC20A6	3-146
MAC515A5		MAC20A6	3-146
MAC515-6		MAC20A6	3-146
MAC515A6		MAC20A6	3-146
MAC515-7		MAC20A8	3-146
MAC515A7		MAC20A8	3-146
MAC515-8		MAC20A8	3-146
MAC515A8		MAC20A8	3-146
MAC515-9		MAC20A10	3-146
MAC515A9		MAC20A10	3-146
MAC515-10		MAC20A10	3-146
MAC515A10		MAC20A10	3-146
MAC525-4		MAC25A4	3-146
MAC525A4		MAC25A4	3-146
MAC525-5		MAC25A6	3-146
MAC525A5		MAC25A6	3-146
MAC525-6		MAC25A6	3-146
MAC525A6		MAC25A6	3-146
MAC525-7		MAC25A8	3-146
MAC525A7		MAC25A8	3-146
MAC525-8		MAC25A8	3-146
MAC525A8		MAC25A8	3-146
MAC525-9		MAC25A10	3-146
MAC525A9		MAC25A10	3-146
MAC525-10		MAC25A10	3-146
MAC525A10		MAC25A10	3-146
MAC625-4	MAC625-4		3-198
MAC625-6	MAC625-6		3-198
MAC625-8	MAC625-8		3-198
MAC635-4	MAC635-4		3-198
MAC635-6	MAC635-6		3-198
MAC635-8	MAC635-8		3-198
MAC3010-4	MAC3010-4		3-202
MAC3010-8	MAC3010-8		3-202
MAC3010-15	MAC3010-15		3-202
MAC3010-25	MAC3010-25		3-202
MAC3010-40	MAC3010-40		3-202
MAC3010-40I	MAC3010-40I		3-202
MAC3020-4	MAC3020-4		3-202
MAC3020-8	MAC3020-8		3-202
MAC3020-15	MAC3020-15		3-202
MAC3020-25	MAC3020-25		3-202
MAC3020-40	MAC3020-40		3-202
MAC3020-40I	MAC3020-40I		3-202
MAC3030-4	MAC3030-4		3-202

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MAC3030-8	MAC3030-8		3-202
MAC3030-15	MAC3030-15		3-202
MAC3030-25	MAC3030-25		3-202
MAC3030-40	MAC3030-40		3-202
MAC3030-40I	MAC3030-40I		3-202
MAC3040-4	MAC3040-4		3-202
MAC3040-8	MAC3040-8		3-202
MAC3040-15	MAC3040-15		3-202
MAC3040-25	MAC3040-25		3-202
MAC3040-40	MAC3040-40		3-202
MAC3040-40I	MAC3040-40I		3-202
MAC3060-4	MAC3060-4		—
MAC3060-8	MAC3060-8		—
MAC3060-15	MAC3060-15		—
MAC3060-25	MAC3060-25		—
MAC3060-40	MAC3060-40		—
MAC3060-40I	MAC3060-40I		—
MAC5571	2N5571		3-75
MAC5572	2N5572		3-75
MAC5573	2N5573		3-75
MAC5574	2N5574		3-75
MAC40688	T6420B		3-328
MAC40689	T6420D		3-328
MAC40690	T6420M		3-328
MAC40795	T4101M		—
MAC40796	T4111M		—
MAC40799	T4121B		—
MAC40800	T4121D		—
MAC40801	T4121M		—
MAC40802	2N6145		3-75
MAC40803	2N6146		3-75
MAC40804	2N6147		3-75
MBS4991	MBS4991		3-207
MBS4992	MBS4992		3-207
MCR22-2	MCR22-2		3-211
MCR22-3	MCR22-3		3-211
MCR22-4	MCR22-4		3-211
MCR22-5	MCR22-6		3-211
MCR22-6	MCR22-6		3-211
MCR22-7	MCR22-8		3-211
MCR22-8	MCR22-8		3-211
MCR63-1	MCR63-2		3-215
MCR63-2	MCR63-2		3-215
MCR63-3	MCR63-3		3-215
MCR63-4	MCR63-4		3-215
MCR63-5	MCR63-6		3-215
MCR63-6	MCR63-6		3-215
MCR63-7	MCR63-8		3-215
MCR63-8	MCR63-8		3-215
MCR63-9	MCR63-10		3-215
MCR63-10	MCR63-10		3-215
MCR64-1	MCR64-2		3-215
MCR64-2	MCR64-2		3-215
MCR64-3	MCR64-3		3-215
MCR64-4	MCR64-4		3-215
MCR64-5	MCR64-6		3-215
MCR64-6	MCR64-6		3-215
MCR64-7	MCR64-8		3-215
MCR64-8	MCR64-8		3-215
MCR64-9	MCR64-10		3-215
MCR64-10	MCR64-10		3-215
MCR65-1	MCR65-2		3-215
MCR65-2	MCR65-2		3-215
MCR65-3	MCR65-3		3-215
MCR65-4	MCR65-4		3-215
MCR65-5	MCR65-6		3-215
MCR65-6	MCR65-6		3-215
MCR65-7	MCR65-8		3-215
MCR65-8	MCR65-8		3-215
MCR65-9	MCR65-10		3-215

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MCR65-10	MCR65-10		3-215
MCR67-1	MCR67-2		3-217
MCR67-2	MCR67-2		3-217
MCR67-3	MCR67-3		3-217
MCR67-6	MCR67-6		3-217
MCR68-1	MCR68-2		3-217
MCR68-2	MCR68-2		3-217
MCR68-3	MCR68-3		3-217
MCR68-6	MCR68-6		3-217
MCR69-1	MCR69-2		3-217
MCR69-2	MCR69-2		3-217
MCR69-3	MCR69-3		3-217
MCR69-6	MCR69-6		3-217
MCR70-1	MCR70-2		3-221
MCR70-2	MCR70-2		3-221
MCR70-3	MCR70-3		3-221
MCR70-6	MCR70-6		3-221
MCR71-1	MCR71-2		3-221
MCR71-2	MCR71-2		3-221
MCR71-3	MCR71-3		3-221
MCR71-6	MCR71-6		3-221
MCR72-1	MCR72-2		3-225
MCR72-2	MCR72-2		3-225
MCR72-3	MCR72-3		3-225
MCR72-4	MCR72-4		3-225
MCR72-5	MCR72-6		3-225
MCR72-6	MCR72-6		3-225
MCR72-7	MCR72-8		3-225
MCR72-8	MCR72-8		3-225
MCR100-3	MCR100-3		3-228
MCR100-4	MCR100-4		3-228
MCR100-5	MCR100-6		3-228
MCR100-6	MCR100-6		3-228
MCR100-7	MCR100-8		3-228
MCR100-8	MCR100-8		3-228
MCR101	MCR102		3-230
MCR102	MCR102		3-230
MCR103	MCR103		3-230
MCR104	MCR100-3		3-228
MCR106-1	MCR106-2		3-232
MCR106-2	MCR106-2		3-232
MCR106-3	MCR106-3		3-232
MCR106-4	MCR106-4		3-232
MCR106-5	MCR106-6		3-232
MCR106-6	MCR106-6		3-232
MCR106-7	MCR106-8		3-232
MCR106-8	MCR106-8		3-232
MCR107-1		MCR106-2	3-232
MCR107-2		MCR106-2	3-232
MCR107-3		MCR106-3	3-232
MCR107-4		MCR106-4	3-232
MCR107-5		MCR106-6	3-232
MCR107-6		MCR106-6	3-232
MCR107-7		MCR106-8	3-232
MCR107-8		MCR106-8	3-232
MCR115	MCR100-4		3-228
MCR120	MCR100-4		3-228
MCR201	MCR202		3-235
MCR202	MCR202		3-235
MCR203	MCR203		3-235
MCR204	MCR204		3-235
MCR205	MCR206		3-235
MCR206	MCR206		3-235
MCR218-2	MCR218-2		3-239
MCR218-3	MCR218-3		3-239
MCR218-4	MCR218-4		3-239
MCR218-5	MCR218-6		3-239
MCR218-6	MCR218-6		3-239
MCR218-7	MCR218-8		3-239

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MCR218-8	MCR218-8		3-239
MCR218-9	MCR218-10		3-239
MCR218-10	MCR218-10		3-239
MCR220-5	2N6397		3-111
MCR220-7	2N6398		3-111
MCR220-9	2N6399		3-111
MCR221-5	2N6403		3-115
MCR221-7	2N6404		3-115
MCR221-9	2N6405		3-115
MCR225-5	2N6507		3-119
MCR225-7	2N6508		3-119
MCR225-9	2N6509		3-119
MCR225-12	MCR225-12		—
MCR225FP-2	MCR225FP-2		3-245
MCR225FP-4	MCR225FP-4		3-245
MCR225FP-6	MCR225FP-6		3-245
MCR225FP-8	MCR225FP-8		3-245
MCR225FP-10	MCR225FP-10		3-245
MCR264-2	MCR264-2		3-249
MCR264-3	MCR264-3		3-249
MCR264-4	MCR264-4		3-249
MCR264-6	MCR264-6		3-249
MCR264-8	MCR264-8		3-249
MCR264-10	MCR264-10		3-249
MCR264-12	MCR264-12		3-249
MCR265-2	MCR265-2		3-252
MCR265-3	MCR265-3		3-252
MCR265-4	MCR265-4		3-252
MCR265-6	MCR265-6		3-252
MCR265-8	MCR265-8		3-252
MCR265-10	MCR265-10		3-252
MCR306-1	2N6237		3-100
MCR306-2	2N6237		3-100
MCR306-3	2N6238		3-100
MCR306-4	2N6239		3-100
MCR306-5	2N6240		3-100
MCR306-6	2N6240		3-100
MCR310-2	MCR310-2		—
MCR310-3	MCR310-3		—
MCR310-4	MCR310-4		—
MCR310-6	MCR310-6		—
MCR310-8	MCR310-8		—
MCR506-1	MCR506-2		3-255
MCR506-2	MCR506-2		3-255
MCR506-3	MCR506-3		3-255
MCR506-4	MCR506-4		3-255
MCR506-6	MCR506-6		3-255
MCR506-8	MCR506-8		3-255
MCR525-4		2N6506	3-119
MCR525-5		2N6507	3-119
MCR525-6		2N6507	3-119
MCR525-7		2N6508	3-119
MCR525-8		2N6508	3-119
MCR525-9		2N6509	3-119
MCR525-10		2N6509	3-119
MCR568-1		MCR68-2	3-217
MCR568-2		MCR68-2	3-217
MCR568-3		MCR68-3	3-217
MCR568-6		MCR68-6	3-217
MCR569-1		MCR69-2	3-217
MCR569-2		MCR69-2	3-217
MCR569-3		MCR69-3	3-217
MCR569-6		MCR69-6	3-217
MCR649AP1	MCR649AP1		—
MCR649AP2	MCR649AP2		—
MCR649AP3	MCR649AP3		—
MCR649AP4	MCR649AP4		—
MCR649AP5	MCR649AP6		—
MCR649AP6	MCR649AP6		—

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MCR649AP7	MCR649AP8		—
MCR649AP8	MCR649AP8		—
MCR649AP9	MCR649AP10		—
MCR649AP10	MCR649AP10		—
MCR729-5	MCR729-5		3-257
MCR729-6	MCR729-6		3-257
MCR729-7	MCR729-7		3-257
MCR729-8	MCR729-8		3-257
MCR729-9	MCR729-9		3-257
MCR729-10	MCR729-10		3-257
MCR808-1		MCR3818-2	3-263
MCR808-2		2N5164	3-59
MCR808-3		MCR3818-3	3-263
MCR808-4		2N5165	3-59
MCR808-5		MCR3818-6	3-263
MCR808-6		2N5166	3-59
MCR808-7		MCR3818-8	3-263
MCR808-8		2N5167	3-59
MCR808-9		MCR3818-10	3-263
MCR808-10		2N2647	3-19
MCR914-1		2N1595	3-6
MCR914-2		2N1595	3-6
MCR914-3		2N1596	3-6
MCR914-4		2N1597	3-6
MCR914-5		2N1599	3-6
MCR914-6		2N1599	3-6
MCR1308-1	MCR3918-2		3-263
MCR1308-2		2N5168	3-59
MCR1308-3	MCR3918-3		3-263
MCR1308-4		2N5169	3-59
MCR1308-5	MCR3918-6		3-263
MCR1308-6		2N5170	3-59
MCR1308-7	MCR3918-8		3-263
MCR1308-8		2N5170	3-59
MCR1308-9	MCR3918-10		3-263
MCR1330		2N6027	3-79
MCR1350		2N6028	3-79
MCR1604-1		2N4186	3-27
MCR1604-2		2N4184	3-27
MCR1604-3		2N4185	3-27
MCR1604-4		2N4186	3-27
MCR1604-5		2N4188	3-27
MCR1604-6		2N4188	3-27
MCR1604-7		2N4190	3-27
MCR1604-8		2N4190	3-27
MCR1718-5	MCR1718-5		3-259
MCR1718-6	MCR1718-6		3-259
MCR1718-7	MCR1718-7		3-259
MCR1718-8	MCR1718-8		3-259
MCR1906-1	MCR1906-2		3-261
MCR1906-2	MCR1906-2		3-261
MCR1906-3	MCR1906-3		3-261
MCR1906-4	MCR1906-4		3-261
MCR1906-5	MCR1906-6		3-261
MCR1906-6	MCR1906-6		3-261
MCR1906-7	MCR1906-8		3-261
MCR1906-8	MCR1906-8		3-261
MCR2305-1		2N4168	3-27
MCR2305-2		2N4168	3-27
MCR2305-3		2N4169	3-27
MCR2305-4		2N4170	3-27
MCR2305-5		2N4172	3-27
MCR2305-6		2N4172	3-27
MCR2305-7		2N4174	3-27
MCR2305-8		2N4174	3-27
MCR2315-1	2N4168		3-27
MCR2315-2	2N4168		3-27
MCR2315-3	2N4169		3-27
MCR2315-4	2N4170		3-27

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MCR2315-5	2N4172		3-27
MCR2315-6	2N4172		3-27
MCR2315-7	2N4174		3-27
MCR2315-8	2N4174		3-27
MCR2604-1		2N4184	3-27
MCR2604-2		2N4184	3-27
MCR2604-3		2N4185	3-27
MCR2604-5		2N4188	3-27
MCR2604-6		2N4188	3-27
MCR2604-7		2N4190	3-27
MCR2604-8		2N4190	3-27
MCR2604L1	2N4184		3-27
MCR2604L2	2N4184		3-27
MCR2604L3	2N4185		3-27
MCR2604L4	2N4186		3-27
MCR2604L5	2N4188		3-27
MCR2604L6	2N4188		3-27
MCR2604L7	2N4190		3-27
MCR2604L8	2N4190		3-27
MCR2818-1	MCR3818-2		3-263
MCR2818-2	MCR3818-2		3-263
MCR2818-3	MCR3818-3		3-263
MCR2818-4	MCR3818-4		3-263
MCR2818-5	MCR3818-6		3-263
MCR2818-6	MCR3818-6		3-263
MCR2818-7	MCR3818-8		3-263
MCR2818-8	MCR3818-8		3-263
MCR2835-1		2N3870	3-21
MCR2835-2		2N3870	3-21
MCR2835-3		2N3870	3-21
MCR2835-4		2N3871	3-21
MCR2835-5		2N3872	3-21
MCR2835-6		2N3872	3-21
MCR2835-7		2N3873	3-21
MCR2835-8		2N3873	3-21
MCR2918-1	MCR3918-2		3-263
MCR2918-2	MCR3918-2		3-263
MCR2918-3	MCR3918-3		3-263
MCR2918-4	MCR3918-4		3-263
MCR2918-5	MCR3918-6		3-263
MCR2918-6	MCR3918-6		3-263
MCR2918-7	MCR3918-8		3-263
MCR2918-8	MCR3918-8		3-263
MCR2935-1	2N3896		3-21
MCR2935-2	2N3896		3-21
MCR2935-3	2N3896		3-21
MCR2935-4	2N3897		3-21
MCR2935-5	2N3898		3-21
MCR2935-6	2N3898		3-21
MCR2935-7	2N3899		3-21
MCR2935-8	2N3899		3-21
MCR3000-1C		MCR218-2	3-239
MCR3000-2	MCR218-2		3-239
MCR3000-3C		MCR218-3	3-239
MCR3000-4	MCR218-4		3-239
MCR3000-5C		MCR218-6	3-239
MCR3000-6	MCR218-6		3-239
MCR3000-7C		MCR218-8	3-239
MCR3000-8	MCR218-8		3-239
MCR3000-9C		MCR218-10	3-239
MCR3000-10C		MCR218-10	3-239
MCR3818-1	MCR3818-2		3-263
MCR3818-2	MCR3818-2		3-263
MCR3818-3	MCR3818-3		3-263
MCR3818-4	MCR3818-4		3-263
MCR3818-5	MCR3818-6		3-263
MCR3818-6	MCR3818-6		3-263
MCR3818-7	MCR3818-8		3-263
MCR3818-8	MCR3818-8		3-263
MCR3818-9	MCR3818-10		3-263

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MCR3818-10	MCR3818-10		3-263
MCR3835-1	MCR3835-2		3-268
MCR3835-2	MCR3835-2		3-268
MCR3835-3	2N3870		3-21
MCR3835-4	2N3871		3-21
MCR3835-5	2N3872		3-21
MCR3835-6	2N3872		3-21
MCR3835-7	MCR3835-8		3-268
MCR3835-8	MCR3835-8		3-268
MCR3835-9	MCR3835-10		3-268
MCR3835-10	MCR3835-10		3-268
MCR3918-1	MCR3918-2		3-263
MCR3918-2	MCR3918-2		3-263
MCR3918-3	MCR3918-3		3-263
MCR3918-4	MCR3918-4		3-263
MCR3918-5	MCR3918-6		3-263
MCR3918-6	MCR3918-6		3-263
MCR3918-7	MCR3918-8		3-263
MCR3918-8	MCR3918-8		3-263
MCR3918-9	MCR3918-10		3-263
MCR3918-10	MCR3918-10		3-263
MCR3935-1	MCR3935-2		3-268
MCR3935-2	MCR3935-2		3-268
MCR3935-3	MCR3935-3		3-268
MCR3935-4	MCR3935-4		3-268
MCR3935-5	MCR3935-6		3-268
MCR3935-6	MCR3935-6		3-268
MCR3935-7	MCR3935-8		3-268
MCR3935-8	MCR3935-8		3-268
MCR3935-9	MCR3935-10		3-268
MCR3935-10	MCR3935-10		3-268
MCR4018-3		2N6167	3-96
MCR4018-4		2N6168	3-96
MCR4018-5		2N6169	3-96
MCR4018-6		2N6169	3-96
MCR4018-7		2N6170	3-96
MCR4018-8		2N6170	3-96
MCR4035-3		2N6171	—
MCR4035-4		2N6172	—
MCR4035-5		2N6173	—
MCR4035-6		2N6173	—
MCR4035-7		2N6174	—
MCR4035-8		2N6174	—
MGT01000	MGT01000		3-271
MGT01000M		MGT01000	3-271
MGT01200	MGT01200		3-271
MGT01200M	MGT01200		3-271
MK1V115	MK1V115		3-279
MK1V125	MK1V125		3-279
MK1V135	MK1V135		3-279
MK1V240	MK1V240		3-282
MK1V260	MK1V260		3-282
MK1V270	MK1V270		3-282
MKP9V120	MKP9V120		3-285
MKP9V130	MKP9V130		3-285
MKP9V240	MKP9V240		3-285
MKP9V260	MKP9V260		3-285
MKP9V270	MKP9V270		3-285
MMBPU131	MMBPU131		—
MMBPU6027	MMBPU6027		—
MMBPU6028	MMBPU6028		—
MMBS5060	MMBS5060		3-288
MMBS5061	MMBS5061		3-288
MMBS5062	MMBS5062		3-288
MPT20		MBS4991	3-207
MPT24		MBS4991	3-207
MPT28		MBS4991	3-207
MPT32		MBS4991	3-207

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MPT36		MBS4991	3-207
MPU131	2N6027		3-79
MPU132	2N6028		3-79
MPU133	2N6028		3-79
MPU231		2N6116	3-88
MPU232		2N6117	3-88
MPU233		2N6118	3-88
MPU6027	2N6027		3-79
MPU6028	2N6028		3-79
MU10	MU10		3-79
MU20	MU20		3-79
MU970		2N2646	3-19
MU971		2N2647	3-19
MU2646		2N2646	3-19
MU4891	MU4891		3-303
MU4892	MU4892		3-303
MU4893	MU4893		3-303
MU4894	MU4894		3-303
MUS4987		MBS4991	3-207
MUS4988		MBS4992	3-207
P0100BA		MCR100-4	3-228
P0100DA		MCR100-6	3-228
P0100MA		MCR100-8	3-228
P0102AA		MCR100-4	3-228
P0102BA		MCR100-4	3-228
P0102CA		MCR100-6	3-228
P0102DA		MCR100-6	3-228
P0103AD		2N2324	3-14
P0103BA		MCR100-4	3-228
P0103BD		2N2326	3-14
P0103CD		2N2329	3-14
P0103DA		MCR100-6	3-228
P0103DD		2N2329	3-14
P0103MA		MCR100-8	3-228
Q200E3		MAC97-4	3-149
Q200E4		MAC97-4	3-149
Q201E3		MAC97-4	3-149
Q201E4		MAC97-4	3-149
Q400E3		MAC97-6	3-149
Q400E4		MAC97-6	3-149
Q2001L3		T2322B	3-316
Q2001L4		T2322B	3-316
Q2001M3		T2322B	3-316
Q2001M4		2N6071	3-83
Q2003L3		2N6071A	3-83
Q2003L4		2N6071A	3-83
Q2003M3		2N6071A	3-83
Q2003M4		2N6071	3-83
Q2003P3		2N6071A	3-83
Q2003P4		2N6071	3-83
Q2004F31		2N6071A	3-83
Q2004F41		2N6071	3-83
Q2004L3		2N6071A	3-83
Q2004L4		2N6071A	3-83
Q2006F31		2N6071	3-83
Q2006F41		2N6071	3-83
Q2006L4		T2500FP	3-320
Q2006L5		SC141B	3-309
Q2006R4		T2500B	3-318
Q2008F41		T2800B	3-222
Q2008L4		T2800B	3-322
Q2008L4		MAC218A4FP	3-172
Q2008L5		MAC218A4	3-169
Q2008R4		T2800B	3-322
Q2010F41		SC146B	3-309
Q2010L4		MAC210A4FP	3-157
Q2010L5		SC146B	3-309
Q2010R4		SC146B	3-309
Q2012L5		MAC212A4FP	3-165
Q2012R5		2N6346A	3-103

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
Q2015G		SC251B	3-312
Q2015H		SC250B	3-312
Q2015L5		MAC15A4FP	3-142
Q2015R5		MAC15A4	3-138
Q2025		SC261B	3-314
Q2025D		SC260B3	3-314
Q2025G		SC261B	3-314
Q2025H		SC260B	3-314
Q2025L5		MAC223A4FP	3-178
Q2025P		MAC25A4	3-146
Q2025R5	MAC223A4		3-175
Q2040		T6401B	3-330
Q2040D		T6420B	3-328
Q2040P		MAC50A4	3-146
Q4001L3		2N6073B	3-83
Q4001L4		T2322D	3-316
Q4001M3		2N6073A	3-83
Q4001M4		2N6073	3-83
Q4003L3		2N6073A	3-83
Q4003L4		2N6073A	3-83
Q4003M3		2N6073A	3-83
Q4003M4		2N6073	3-83
Q4003P3		2N6073A	3-83
Q4003P4		2N6073	3-83
Q4004F31		2N6073A	3-83
Q4004F41		2N6073	3-83
Q4004L3		2N6073A	3-83
Q4004L4		2N6073A	3-83
Q4006F41		2N6073	3-83
Q4006L4		T2500D	3-318
Q4006L5		SC141D	3-309
Q4006R4		T2500D	3-318
Q4008F41		T2800D	3-322
Q4008L4		MAC218A6FP	3-172
Q4008L4A		T2800D	3-322
Q4008L5		MAC218A6	3-169
Q4008R4		T2800D	3-322
Q4010F41		SC146D	3-309
Q4010L4		MAC210A6FP	3-157
Q4010L5		SC146D	3-309
Q4010R4		SC146D	3-309
Q4012L5		MAC212A6FP	3-165
Q4012R5		2N6347A	3-107
Q4015G		SC251D	3-312
Q4015H		SC250D	3-312
Q4015L5		MAC15A6FP	3-142
Q4015R5		MAC15A6	3-138
Q4025		SC261D	3-314
Q4025D		SC260D3	3-314
Q4025G		SC261D	3-314
Q4025H		SC260D	3-314
Q4025L6		MAC223A6FP	3-178
Q4025P		MAC25A6	3-146
Q4025R5	MAC223A6		3-175
Q4040		T6401D	3-330
Q4040D		T6420D	3-328
Q4040P		MAC50A6	3-146
Q5004F41		2N6075	3-83
Q5004L4		2N6074A	3-83
Q5006F41		T2500M	3-318
Q5006L4		T2500M	3-318
Q5006L5		SC141M	3-309
Q5006R4		T2500M	3-318
Q5008F41		T2800D	3-322
Q5008L4		T2800M	3-322
Q5008L4A		T2800M	3-322
Q5008L5		MAC218A8	3-169
Q5008R4		T2800M	3-322
Q5010F41		SC146M	3-309

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
Q5010L4		SC146M	3-309
Q5010L5		SC146M	3-309
Q5010R4		SC146M	3-309
Q5012L5		2N6348A	3-107
Q5012R5		2N6348A	3-107
Q5015G		SC251M	3-312
Q5015H		SC250M	3-312
Q5015L5		MAC15A8	3-138
Q5015R5		MAC15A8	3-138
Q5025		SC261M	3-314
Q5025G		SC261M	3-314
Q5025H		SC260M	3-314
Q5025L5		MAC223A8	3-175
Q5025P		MAC25A8	3-146
Q5025R5		MAC223A8	3-175
Q5040		T6401M	3-330
Q5040D		T6420M	3-328
Q5040P		MAC50A8	3-146
Q6004F41		2N6075	3-83
Q6004L4		2N6074A	3-83
Q6006F51		2N6075	3-83
Q6006L5		SC141M	3-309
Q6006R5		SC141M	3-309
Q6008F51		T2802M	3-322
Q6008L5		MAC218A8FP	3-172
Q6008L5A		MAC218A8	3-169
Q6008R5		MAC218A8	3-169
Q6010F51		SC146M	3-309
Q6010L5		MAC210A8FP	3-157
Q6010R5		SC146M	3-309
Q6012L5		MAC212A8FP	3-165
Q6012R5		2N6348A	3-103
Q6015G		SC251M	3-312
Q6015H		SC250M	3-312
Q6015L5		MAC15A8FP	3-142
Q6015R5		MAC15A8	3-138
Q6025		SC261M	3-314
Q6025D		SC261M	3-314
Q6025G		SC261M	3-314
Q6025H		SC260M	3-314
Q6025L5		MAC223A8FP	3-178
Q6025P		MAC25A8	3-146
Q6025R5	MAC223A8		3-175
Q6040		T6400M	3-328
Q6040D		T6420M	3-328
Q6040P		MAC50A8	3-146
Q8010L5		SC146N	3-309
Q8010R5		SC146N	3-309
Q8012L5		2N6349A	3-107
Q8012R5		2N6349A	3-107
Q8015L5		MAC15A10	3-138
Q8015R5		MAC15A10	3-138
S0301L		MCR106-2	3-232
S0301LS1		MCR106-2	3-232
S0301LS2		MCR106-2	3-232
S0301LS3		MCR106-2	3-232
S0301M	2N1595		3-6
S0301MS1	2N4213		3-37
S0301MS2	2N2323		3-14
S0301MS3	MCR1906-2		3-261
S0303L		MCR106-2	2-232
S0303LS1		MCR106-2	3-232
S0303LS2		MCR106-2	3-232
S0303LS3		MCR106-2	3-232
S0303MS2		2N6237	3-100
S0303MS3		2N6237	3-100
S0306FS21		MCR72-2	3-225
S0306FS31		MCR72-2	3-225
S0306L		S2800F	3-305

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
S0306LS2		MCR72-2	3-225
S0306LS3		MCR72-2	3-225
S0308F1		MCR218-2	3-239
S0308F3		MCR218-2	3-239
S0308FS4		MCR72-2	3-225
S0308FS21		MCR72-2	3-225
S0308FS31		MCR72-2	3-225
S0308L		S2800F	3-305
S0308LS2		MCR72-2	3-225
S0308LS3		MCR72-2	3-225
S0308R		S2800A	3-305
S0310F1		2N6394	3-111
S0310L		2N6394	3-111
S0312L		2N6394	3-111
S0312R		2N6394	3-111
S0315H		2N1843	3-11
S0315L		2N6400	3-115
S0316R		2N6400	3-115
S0320L		2N6504	3-119
S0325D		C230F3	3-135
S0325H	2N682		3-2
S0325R		2N6504	3-119
S0335D		C228A	3-133
S0335G	MCR3835-2		3-268
S0335H	MCR3935-2		3-268
S0501L		MCR106-2	3-232
S0501LS1		MCR106-2	3-232
S0501LS2		MCR106-2	3-232
S0501LS3		MCR106-2	3-232
S0501M	2N1595		3-6
S0501MS1	2N4213		3-37
S0501MS2	2N2323		3-14
S0501MS3	MCR1906-2		3-261
S0503L		MCR106-2	3-232
S0503LS1		MCR106-2	3-232
S0503LS2		MCR106-2	3-232
S0503LS3		MCR106-2	3-232
S0503MS2		2N6238	3-100
S0503MS3		2N6238	3-100
S0505FS21		MCR72-2	3-225
S0505FS31		MCR72-2	3-225
S0506FS21		MCR72-2	3-225
S0506FS31		MCR72-2	3-225
S0506L		S2800A	3-305
S0506LS2		MCR72-2	3-225
S0506LS3		MCR72-2	3-225
S0508F1		MCR218-2	3-239
S0508F3		MCR218-2	3-239
S0508FS31		MCR72-2	3-225
S0508L		S2800A	3-305
S0508LS2		MCR72-2	3-225
S0508LS3		MCR72-2	3-225
S0508R		S2800A	3-305
S0508S21		MCR72-2	3-225
S0510L		2N6394	3-111
S0512L		2N6394	3-111
S0512R		2N6394	3-111
S0515L		2N6400	3-115
S0516R		2N6400	3-115
S0520L		2N6504	3-119
S0525D		C230F3	3-135
S0525H	2N682		3-2
S0535D		C228A3	3-133
S0535G	2N3870		3-21
S0535H	2N3870		3-21
S106A	C106A1		3-125
S106B	C106B1		3-125
S106C	C106C1		3-125

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
S106D	C106D1		3-125
S106E	C106E1		3-125
S106F	C106F1		3-125
S106M	C106M		3-125
S107A		C106A	3-125
S107B		C106B	3-125
S107C		C106D	3-125
S107D		C106D	3-125
S107E		C106A	3-125
S107F		C106F	3-125
S107M		C106M	3-125
S1001L		MCR106-3	3-232
S1001LS1		MCR106-3	3-232
S1001LS3		MCR106-3	3-232
S1001M	2N1596		3-6
S1001MS1	2N4214		3-37
S1001MS2	2N2324		3-14
S1001MS3	MCR1906-3		3-261
S1003L		MCR106-3	3-232
S1003LS1		MCR106-3	3-232
S1003LS2		MCR106-3	3-232
S1003LS3		MCR106-3	3-232
S1003MS2		2N6238	3-100
S1003MS3		2N6238	3-100
S1006FS21		MCR72-3	3-225
S1006FS31		MCR72-3	3-225
S1006L		S2800A	3-305
S1006LS2		MCR72-3	3-225
S1006LS3		MCR72-3	3-225
S1008F1		MCR218-3	3-239
S1008F3		MCR218-3	3-239
S1008FS21		MCR72-3	3-225
S1008FS31		MCR72-3	3-225
S1008L		MCR218-3	3-239
S1008LS2		MCR72-3	3-225
S1008LS3		MCR72-3	3-225
S1008R		S2800A	3-305
S1010F1		2N6395	3-111
S1010L		2N6395	3-111
S1012L		2N6395	3-111
S1012R		2N6395	3-111
S1015L		2N6401	3-115
S1016R		2N6401	3-115
S1020L		2N6505	3-115
S1025D		C230A3	3-135
S1025H	2N683		3-2
S1025R		2N6505	3-119
S1035D		C228A3	3-133
S1035G	2N3870		3-21
S1035H	2N3896		3-21
S2001L		MCR106-4	3-232
S2001LS1		MCR106-4	3-232
S2001LS2		MCR106-4	3-232
S2001LS3		MCR106-4	3-232
S2001M	2N1597		3-6
S2001MS1	2N4216		3-37
S2001MS2	2N2326		3-14
S2001MS3		MCR1906-4	3-261
S2003L		MCR106-4	3-232
S2003LS1		MCR106-4	3-232
S2003LS2		MCR106-4	3-232
S2003LS3		MCR106-4	3-232
S2003MS2		2N6239	3-100
S2003MS3		2N6239	3-100
S2006FS21		MCR72-4	3-225
S2006FS31		MCR72-4	3-225
S2006L		S2800B	3-305
S2006LS2		MCR72-4	3-225
S2006LS3		MCR72-4	3-225

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
S2008F1		MCR218-4	3-239
S2008F3		MCR218-4	3-239
S2008FS21		MCR72-4	3-225
S2008FS31		MCR72-4	3-225
S2008LS2		MCR72-4	3-225
S2008LS3		MCR72-4	3-225
S2008R		S2800B	3-305
S2010L		2N6396	3-111
S2012L		2N6396	3-111
S2012R		2N6396	3-111
S2015L		2N6402	3-115
S2016R		2N6402	3-115
S2020L		2N6506	3-119
S2025D		C230B3	3-135
S2025H	2N685		3-2
S2025R		2N6506	3-119
S2035D		C228B3	3-133
S2035G	2N3871		3-21
S2035H	2N3897		3-21
S2060A	2N6238		3-100
S2060B	2N6239		3-100
S2060C	MCR106-6		3-232
S2060D	2N6240		3-100
S2060E	MCR106-8		3-232
S2060F	2N6237		3-100
S2060M	2N6241		3-100
S2060Q	2N6237		3-100
S2060Y	2N6237		3-100
S2061A	2N6238		3-100
S2061B	2N6239		3-100
S2061C	MCR106-6		3-232
S2061D	2N6240		3-100
S2061E	MCR106-8		3-232
S2061F	2N6237		3-100
S2061M	2N6241		3-100
S2061Q	2N6237		3-100
S2061Y	2N6237		3-100
S2062A	2N6238		3-100
S2062B	2N6239		3-100
S2062C	MCR106-6		3-232
S2062D	2N6240		3-100
S2062E	MCR106-8		3-232
S2062F	2N6237		3-100
S2062M	2N6241		3-100
S2062Q	2N6237		3-100
S2062Y	2N6237		3-100
S2600B		C122B1	3-128
S2600D		C122D1	3-128
S2600M		C122M1	3-128
S2610B		S2800B	3-305
S2610D		S2800D	3-305
S2610M		S2800M	3-305
S2620B		S2800B	3-305
S2620D		S2800D	3-305
S2620M		S2800M	3-305
S2710B		S2800B	3-305
S2710D		S2800D	3-305
S2710M		S2800M	3-305
S2800A	S2800A		3-305
S2800B	S2800B		3-305
S2800C	S2800D		3-305
S2800D	S2800D		3-305
S2800E	S2800M		3-305
S2800F	S2800F		3-305
S2800M	S2800M		3-305
S2800N	S2800N		3-305
S2800S	S2800N		3-305
S4001L		MCR106-6	3-232
S4001LS1		MCR106-6	3-232

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
S4001LS2		MCR106-6	3-232
S4001LS3		MCR106-6	3-232
S4001M	2N1599		3-6
S4001MS1	2N4219		3-37
S4001MS2	2N2329		3-14
S4001MS3	MCR1906-6		3-261
S4003L		MCR106-6	3-232
S4003LS1		MCR106-6	3-232
S4003LS2		MCR106-6	3-232
S4003LS3		MCR106-6	3-232
S4003MS2		2N6240	3-100
S4003MS3		2N6240	3-100
S4006B		MCR729-6	3-257
S4006FS21		MCR72-6	3-225
S4006FS31		MCR72-6	3-225
S4006L		S2800D	3-305
S4006LS2		MCR72-6	3-225
S4006LS3		MCR72-6	3-225
S4008F1		MCR218-6	3-239
S4008F3		MCR218-6	3-239
S4008FS21		MCR72-6	3-225
S4008FS31		MCR72-6	3-225
S4008L		MCR218-6	3-239
S4008LS2		MCR72-6	3-225
S4008LS3		MCR72-6	3-225
S4008R		S2800D	3-305
S4010L		2N6397	3-111
S4012L		2N6397	3-111
S4012R		2N6397	3-111
S4015L		2N6403	3-115
S4016R		2N6403	3-115
S4020L		2N6507	3-119
S4025D		C230D3	3-135
S4025H	2N688		3-2
S4025R		2N6507	3-119
S4035D		C228D3	3-133
S4035G	2N3872		3-21
S4035H	2N3898		3-21
S5006B		MCR729-7	3-257
S5008L		MCR218-8	3-239
S5025C		MCR649-8	—
S5025G		MCR3835-8	3-268
S5025H		MCR3935-8	3-268
S5035G	MCR3835-8		3-268
S5035H	MCR3935-8		3-268
S6000C	2N6397		3-111
S6000E	2N6398		3-111
S6000S	2N6399		3-111
S6001L		MCR106-8	3-232
S6003L		MCR106-8	3-232
S6006L		S2800M	3-305
S6008F		MCR218-8	3-239
S6008F1		S2800M	3-305
S6008F3		MCR218-8	3-239
S6008L		S2800M	3-305
S6008R		S2800M	3-305
S6010L		2N6398	3-111
S6012L		2N6398	3-111
S6012R		2N6398	3-111
S6015L		2N6404	3-115
S6016R		2N6404	3-115
S6020L		2N6508	3-119
S6025D		C230M3	3-135
S6025H	2N690		3-2
S6025R		2N6508	3-119
S6035D		C228M3	3-133
S6035G	2N3873		3-21
S6035H	2N3899		3-21
S6100C	2N6403		3-115

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
S6100E	2N6404		3-115
S6100S	2N6405		3-115
S6200A	S6200A		3-307
S6200B	S6200B		3-307
S6200D	S6200D		3-307
S6200M	S6200M		3-307
S6210A	S6210A		3-307
S6210B	S6210B		3-307
S6210D	S6210D		3-307
S6210M	S6210M		3-307
S6220A	S6220A		3-307
S6220B	S6220B		3-307
S6220D	S6220D		3-307
S6220M	S6220M		3-307
S6420A		2N6171	—
S6420D		2N6172	—
S6420M		2N6174	—
S6493M		MCR1718-8	3-259
S8015L		2N6405	3-115
S8016R		2N6405	3-115
S8020L		2N6509	3-119
S8025R		2N6509	3-119
SC92A	MAC97A4		3-149
SC92B	MAC97A4		3-149
SC92D	MAC97A6		3-149
SC92F	MAC97A4		3-149
SC129B		MAC223A4	3-175
SC129D		MAC223A6	3-175
SC129E		MAC223A8	3-175
SC129M		MAC223A8	3-175
SC136A	2N6070		—
SC136B	2N6071		3-83
SC136C	2N6073		3-83
SC136D	2N6073		3-83
SC136E	2N6075		3-83
SC136M	2N6075		3-83
SC141A	SC141B		3-309
SC141B	SC141B		3-309
SC141C	SC141D		3-309
SC141D	SC141D		3-309
SC141E	SC141M		3-309
SC141M	SC141M		3-309
SC141N	SC141N		3-309
SC143B	SC143B		
SC143D	SC143D		—
SC143E	SC143M		—
SC143M	SC143M		—
SC146A	SC146B		3-309
SC146B	SC146B		3-309
SC146C	SC146D		3-309
SC146D	SC146D		3-309
SC146E	SC146M		3-309
SC146F	SC146B		3-309
SC146M	SC146M		3-309
SC146N	SC146N		3-309
SC146S	SC146N		3-309
SC149B	SC149B		—
SC149D	SC149D		
SC149F	SC149B		—
SC149M	SC149M		—
SC151B		MAC15A4	3-138
SC151D		MAC15A6	3-138
SC151E		MAC15A8	3-138
SC151M		MAC15A8	3-138
SC160B		MAC25A4	3-146
SC160D		MAC25A6	3-146
SC160E		MAC25A8	3-146
SC160M		MAC25A8	3-146
SC240B		T4121B	3-71

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
SC240D		T4121D	3-71
SC240E		T4121M	3-71
SC240M		T4121M	3-71
SC241B		T4101B	3-71
SC241D		T4101D	3-71
SC241E		T4101M	3-71
SC241M		T4101M	3-71
SC245A	SC245B		—
SC245B	SC245B		—
SC245C	SC245D		—
SC245D	SC245D		—
SC245E	SC245M		—
SC245F	SC245B		—
SC245M	SC245M		—
SC245N	SC245N		—
SC245S	SC245N		—
SC246A	SC246B		—
SC246B	SC246B		—
SC246C	SC246D		—
SC246D	SC246D		—
SC246E	SC246M		—
SC246F	SC246B		—
SC246M	SC246M		—
SC246N	SC246N		—
SC246S	SC246N		
SC250A	SC250B		3-312
SC250B	SC250B		3-312
SC250B3	SC250B3		3-312
SC250C	SC250D		3-312
SC250D	SC250D		3-312
SC250D3	SC250D3		3-312
SC250E	SC250M		3-312
SC250E3	SC250M3		3-312
SC250F	SC250B		3-312
SC250M	SC250M		3-312
SC250M3	SC250M3		3-312
SC250N	SC250N		3-312
SC250S	SC250N		3-312
SC251A	SC251B		3-312
SC251B	SC251B		3-312
SC251C	SC251D		3-312
SC251D	SC251D		3-312
SC251E	SC251M		3-312
SC251F	SC251B		3-312
SC251M	SC251M		3-312
SC251N	SC251N		3-312
SC251S	SC251N		3-312
SC260A	SC260B		3-314
SC260B	SC260B		3-314
SC260B3	SC260B3		3-314
SC260C	SC260D		3-314
SC260D	SC260D		3-314
SC260D3	SC260D3		3-314
SC260E	SC260M		3-314
SC260E3	SC260M3		3-314
SC260F	SC260B		3-314
SC260M	SC260M		3-314
SC260M3	SC260M3		3-314
SC261A	SC261B		3-314
SC261B	SC261B		3-314
SC261C	SC261D		3-314
SC261D	SC261D		3-314
SC261E	SC261M		3-314
SC261F	SC261B		3-314
SC261M	SC261M		3-314
SC265B		2N5444	3-67
SC265D		2N5445	3-67
SC265E		2N5446	3-67
SC265M		2N5446	3-67

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
SC266B		2N5441	3-67
SC266D		2N5442	3-67
SC266E		2N5443	3-67
SC266M		2N5443	3-67
SISC122C		C122D1	3-128
SISC122D		C122D1	3-128
SISC122E		C122M1	3-128
SISC122M		C122M1	3-128
SISC122N		C122N1	3-128
SISC141C		SC141D	3-309
SISC141D		SC141D	3-309
SISC141E		SC141M	3-309
SISC141M		SC141M	3-309
SISC141N		SC141N	3-309
SISC141S		SC141N	3-309
SISC143C		MAC218A6	3-169
SISC143D		MAC218A6	3-169
SISC143E		MAC218A8	3-169
SISC143M		MAC218A8	3-169
SISC143N		MAC218A10	3-169
SISC143S		MAC218A10	3-169
SISC146C		SC146D	3-309
SISC146D		SC146D	3-309
SISC146E		SC146M	3-309
SISC146M		SC146M	3-309
SISC146N		SC146N	3-309
SISC146S		SC146N	3-309
SISC149C		2N6347A	3-103
SISC149D		2N6347A	3-103
SISC149E		2N6348A	3-103
SISC149M		2N6348A	3-103
SISC149N		2N6349A	3-103
SISC149S		2N6349A	3-103
T106A1		C106A	3-125
T106B1		C106B	3-125
T106C1		C106D	3-125
T106D1		C106D	3-125
T106E1		C106M	3-125
T106F1		C106F	3-125
T106M1		C106M	3-125
T106Q1		C106F	3-125
T106Y1		C106F	3-125
T107A1		C106A	3-125
T107B1		C106B	3-125
T107C1		C106D	3-125
T107D1		C106D	3-125
T107E1		C106M	3-125
T107F1		C106F	3-125
T107M1		C106M	3-125
T107Q1		C106F	3-125
T107Y1		C106F	3-125
T1145A0		2N1595	3-6
T1145A1		2N1596	3-6
T1145A2		2N1597	3-6
T1145A3		2N1599	3-6
T1145A4		2N1599	3-6
T2301A		2N6070B	—
T2301B		2N6070B	—
T2301C		2N6073B	3-83
T2301D		2N6073B	3-83
T2301E		2N6075B	3-83
T2301F		2N6075B	3-83
T2301M		2N6075B	3-83
T2301PA		2N6070B	—
T2301PB		2N6070B	—
T2301PC		2N6073B	3-83
T2301PD		2N6073B	3-83
T2301PE		2N6075B	3-83
T2301PF		2N6075B	3-83

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
T2301PM		2N6075B	3-83
T2302A		2N6070A	—
T2302B		2N6070A	—
T2302C		2N6073A	3-83
T2302D		2N6073A	3-83
T2302E		2N6075A	3-83
T2302F		2N6070A	—
T2302M		2N6075A	3-83
T2302PA		2N6070A	—
T2302PB		2N6070A	—
T2302PC		2N6073A	3-83
T2302PD		2N6073A	3-83
T2302PE		2N6075A	3-83
T2302PF		2N6070A	—
T2302PM		2N6075A	3-83
T2303F		2N6070A	—
T2304B		2N6070A	—
T2304D		2N6073A	3-83
T2305B		2N6071A	3-83
T2305D		2N6073A	3-83
T2306A		2N6070A	—
T2306B		2N6071A	3-83
T2306D		2N6073A	3-83
T2311A		2N6070B	—
T2311B		2N6070B	—
T2311D		2N6071B	3-83
T2311F		2N6070B	—
T2312A		2N6070A	—
T2312B		2N6070A	—
T2312D		2N6071A	3-83
T2312F		2N6070A	—
T2313A		2N6070A	—
T2313B		2N6070A	—
T2313D		2N6071A	3-83
T2313F		2N6071A	3-83
T2313M		2N6075A	3-83
T2322A	T2322B		3-316
T2322B	T2322B		3-316
T2322C	T2322D		3-316
T2322D	T2322D		3-316
T2322E	T2322M		3-316
T2322F	T2322B		3-316
T2322M	T2322M		3-316
T2323A	T2323B		3-316
T2323B	T2323B		3-316
T2323C	T2323D		3-316
T2323D	T2323D		3-316
T2323E	T2323M		3-316
T2323F	T2323B		3-316
T2323M	T2323M		3-316
T2500A	T2500B		3-318
T2500B	T2500B		3-318
T2500BFP	T2500BFP		3-320
T2500C	T2500D		3-318
T2500D	T2500D		3-318
T2500DFP	T2500DFP		3-320
T2500E	T2500M		3-318
T2500M	T2500M		3-318
T2500MFP	T2500MFP		3-320
T2500N	T2500N		3-318
T2500NFP	T2500NFP		3-320
T2500S	T2500N		3-318
T2506B	T2500B		3-318
T2506D	T2500D		3-318
T2800A	T2800B		3-322
T2800B	T2800B		3-322
T2800C	T2800D		3-322
T2800D	T2800D		3-322
T2800E	T2800M		3-322

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
T2800F	T2800B		3-322
T2800M	T2800M		3-322
T2801A	T2801B		3-324
T2801B	T2801B		3-324
T2801C	T2801D		3-324
T2801D	T2801D		3-324
T2801E	T2801M		3-324
T2801M	T2801M		3-324
T2801N	T2801N		3-324
T2801S	T2801N		3-324
T2802A	T2802B		3-322
T2802B	T2802B		3-322
T2802C	T2802D		3-322
T2802D	T2802D		3-322
T2802E	T2802M		3-322
T2802F	T2802B		3-322
T2802M	T2802M		3-322
T2806B	T2800B		3-322
T2806C	T2800D		3-322
T2806D	T2800D		3-322
T2806M	T2800M		3-322
T2806N		MAC218A10FP	3-172
T2850A		2N6346A	3-103
T2850B		2N6346A	3-103
T2850D		2N6347A	3-103
T2850E		2N6347A	3-103
T2851B	T2801B		3-324
T2851C	T2801D		3-324
T2851D	T2801D		3-324
T2851E	T2801M		3-324
T2856B	T2800B		3-322
T2856C	T2800D		3-322
T2856D	T2800D		3-322
T4100A	2N5571		3-75
T4100B	2N5571		3-75
T4100C	2N5572		3-75
T4100D	2N5572		3-75
T4100E	T4100M		3-75
T4100F	2N5571		3-75
T4100M	T4100M		3-75
T4101A	2N5567		3-71
T4101B	2N5567		3-71
T4101C	2N5568		3-71
T4101D	2N5568		3-71
T4101E	T4101M		3-71
T4101F	2N5567		3-71
T4101M	T4101M		3-71
T4106B	2N5571		3-75
T4106D	2N5572		3-75
T4106M	T4100M		3-75
T4107B	2N5567		3-71
T4107D	2N5568		3-71
T4107M	T4101M		3-71
T4110A	2N5573		3-75
T4110B	2N5573		3-75
T4110C	2N5574		3-75
T4110D	2N5574		3-75
T4110E	T4110M		3-75
T4110F	2N5573		3-75
T4110M	T4110M		3-75
T4111A	2N5569		3-71
T4111B	2N5569		3-71
T4111C	2N5570		3-71
T4111D	2N5570		3-71
T4111E	T4111M		3-71
T4111F	2N5569		3-71
T4111M	T4111M		3-71
T4116B	2N5573		3-75
T4116D	2N5574		3-75

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
T4116M	T4110M		3-75
T4117B	2N5569		3-71
T4117D	2N5570		3-71
T4117M	T4111M		3-71
T4120A	T4120B		3-326
T4120B	T4120B		3-326
T4120C	T4120D		3-326
T4120D	T4120D		3-326
T4120E	T4120M		3-326
T4120F	T4120B		3-326
T4120M	T4120M		3-326
T4120N	T4120N		3-326
T4120S	T4120N		3-326
T4121A	T4121B		3-71
T4121B	T4121B		3-71
T4121C	T4121D		3-71
T4121D	T4121D		3-71
T4121E	T4121M		3-71
T4121F	T4121B		3-71
T4121M	T4121M		3-71
T4121N	T4121N		3-71
T4121S	T4121N		3-71
T4126B	T4120B		3-326
T4126D	T4120D		3-326
T4126M	T4120M		3-326
T4127B	T4121B		3-71
T4127D	T4121D		3-71
T4127M	T4121M		3-71
T4700B		MAC15A4	3-138
T4700C		MAC15A6	3-138
T4700E		MAC15A8	3-138
T4700F		MAC15A4	3-138
T4706B		MAC15A4	3-138
T4706D		MAC15A6	3-138
T6000A		MAC15A4	3-138
T6000B		MAC15A4	3-138
T6000C		MAC15A6	3-138
T6000D		MAC15A6	3-138
T6000E		MAC15A8	3-138
T6000F		MAC15A4	3-138
T6000M		MAC15A8	3-138
T6001A		MAC15A4	3-138
T6001B		MAC15A4	3-138
T6001C		MAC15A6	3-138
T6001D		MAC15A6	3-138
T6001E		MAC15A8	3-138
T6001F		MAC15A4	3-138
T6001M		MAC15A8	3-138
T6006A		MAC15A4	3-138
T6006B		MAC15A4	3-138
T6006C		MAC15A6	3-138
T6006D		MAC15A6	3-138
T6006E		MAC15A8	3-138
T6006F		MAC15A4	3-138
T6006M		MAC15A8	3-138
T6260B		MAC25A4	3-146
T6260C		MAC25A6	3-146
T6260D		MAC25A6	3-146
T6260E		MAC25A8	3-146
T6260M		MAC25A8	3-146
T6261B		MAC25A4	3-146
T6261C		MAC25A6	3-146
T6261E		MAC25A8	3-146
T6261M		MAC25A8	3-146
T6400A	T6400B		3-328
T6400B	T6400B		3-328
T6400C	T6400D		3-328
T6400D	T6400D		3-328
T6400E	T6400M		3-328

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
T6400M	T6400M		3-328
T6400N	T6400N		3-328
T6400S	T6400N		3-328
T6401A	T6401B		3-330
T6401B	T6401B		3-330
T6401C	T6401D		3-330
T6401D	T6401D		3-330
T6401E	T6401M		3-330
T6401M	T6401M		3-330
T6401N	T6401N		3-330
T6401S	T6401N		3-330
T6402E	2N5443		3-67
T6402F	2N5441		3-67
T6406B	2N5441		3-67
T6406D	2N5442		3-67
T6406E	2N5443		3-67
T6406M	2N5443		3-67
T6407B	T6401B		3-330
T6407D	T6401D		3-330
T6407E	T6401M		3-330
T6407M	T6401M		3-330
T6410A	T6410B		3-328
T6410B	T6410B		3-328
T6410C	T6410D		3-328
T6410D	T6410D		3-328
T6410E	T6410M		3-328
T6410M	T6410M		3-328
T6410N	T6410N		3-328
T6410S	T6410N		3-328
T6411A	T6411B		3-330
T6411B	T6411B		3-330
T6411C	T6411D		3-330
T6411D	T6411D		3-330
T6411E	T6411M		3-330
T6411M	T6411M		3-330
T6411N	T6411N		3-330
T6411S	T6411N		3-330
T6412E	2N5446		3-67
T6412F	2N5444		3-67
T6420A	T6420B		3-328
T6420B	T6420B		3-328
T6420C	T6420D		3-328
T6420D	T6420D		3-328
T6420E	T6420M		3-328
T6420M	T6420M		3-328
T6420N	T6420N		3-328
T6420S	T6420N		3-328
T6421A	T6421B		3-330
T6421B	T6421B		3-330
T6421C	T6421D		3-330
T6421D	T6421D		3-330
T6421E	T6421M		3-330
T6421M	T6421M		3-330
T6421N	T6421N		3-330
T6421S	T6421N		3-330
T6426B	T6420B		3-328
T6426D	T6420D		3-328
T6426M	T6420M		3-328
T6427B	T6421B		3-330
T6427D	T6421D		3-330
T6427M	T6421M		3-330
TE205		MCR100-4	3-228
TE305		MCR100-6	3-228
TE405		MCR100-6	3-228
TE505		MCR100-8	3-228
TE605		MCR100-8	3-228
TIC20		2N5567	3-71
TIC21		2N5568	3-71
TIC22		2N5569	3-71

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
TIC23		2N5570	3-71
TIC39A	2N6238		3-100
TIC39B	2N6239		3-100
TIC39C	MCR100-6		3-228
TIC39D	2N6240		3-100
TIC39E	MCR100-8		3-228
TIC39F	2N6237		3-100
TIC39Y	2N6237		3-100
TIC44	2N5060		3-55
TIC45	2N5061		3-55
TIC46	2N5062		3-55
TIC47	2N5064		3-55
TIC60	2N5060		3-55
TIC61	2N5061		3-55
TIC62	2N5062		3-55
TIC63	2N5064		3-55
TIC64	2N5064		3-55
TIC116A		C122A1	3-128
TIC116B		C122B1	3-128
TIC116C		C122D1	3-128
TIC116D		C122D1	3-128
TIC116E		C122M1	3-128
TIC116F		C122F1	3-128
TIC116M		C122M1	3-128
TIC126A		2N6395	3-111
TIC126B		2N6396	3-111
TIC126C		2N6397	3-111
TIC126D		2N6397	3-111
TIC126E		2N6398	3-111
TIC126F		2N6394	3-111
TIC126M		2N6398	3-111
TIC205A		2N6070B	—
TIC205B		2N6070B	—
TIC205D		2N6073B	3-83
TIC206A		2N6070A	—
TIC206B		2N6071A	3-83
TIC206D		2N6073A	3-83
TIC215A		2N6070A	—
TIC215B		2N6071A	3-83
TIC215D		2N6073A	3-83
TIC216A		MAC228A4	3-184
TIC216B		MAC228A4	3-184
TIC216D		MAC228A6	3-184
TIC220B		2N5567	3-71
TIC220D		2N5568	3-71
TIC220E		T4101M	3-71
TIC221B		T4121B	3-71
TIC221D		T4121D	3-71
TIC221E		T4121M	3-71
TIC222B		2N5569	3-71
TIC222D		2N5570	3-71
TIC222E		T4111M	3-71
TIC226B		SC141B	3-309
TIC226D		SC141D	3-309
TIC230B		2N5567	3-71
TIC230D		2N5568	3-71
TIC230E		T4101M	3-71
TIC231B		T4121B	3-71
TIC231D		T4121D	3-71
TIC231E		T4121M	3-71
TIC232B		2N5569	3-71
TIC232D		2N5570	3-71
TIC232E		T4111M	3-71
TIC236B		2N6342A	3-107
TIC236D		2N6343A	3-107
TIC240B		2N5571	3-75
TIC240D		2N5572	3-75
TIC240E		T4100M	3-75
TIC241B		T4120B	3-326

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
TIC241D		T4120D	3-326
TIC241E		T4120M	3-326
TIC242B		2N5573	3-75
TIC242D		2N5574	3-75
TIC242E		T4110M	3-75
TIC246B		MAC15A4	3-138
TIC246D		MAC15A6	3-138
TIC252B		T6411B	3-330
TIC252D		T6411D	3-330
TIC252E		T6411M	3-330
TIC252M		T6411M	3-330
TIC253B		MAC20A4	3-146
TIC253D		MAC20A6	3-146
TIC253E		MAC20A8	3-146
TIC253M		MAC20A8	3-146
TIC260B		T6401B	3-330
TIC260D		T6401D	3-330
TIC260E		T6401M	3-330
TIC260M		T6401M	3-330
TIC262D		T6411D	3-330
TIC262E		T6411M	3-330
TIC262M		T6411M	3-330
TIC263B		MAC25A4	3-146
TIC263D		MAC25A6	3-146
TIC263E		MAC25A8	3-146
TIC263M		MAC25A8	3-146
TIC270B		2N5441	3-67
TIC270D		2N5442	3-67
TIC270E		2N5443	3-67
TIC270M		2N5444	3-67
TIC272B		2N5444	3-67
TIC272D		2N5445	3-67
TIC272E		2N5446	3-67
TIC272M		2N5446	3-67
TL106-05		MCR106-2	3-232
TL106-1		MCR106-3	3-232
TL106-2		MCR106-4	3-232
TL106-4		MCR106-6	3-232
TL106-6		MCR106-8	3-232
TL107-05		MCR106-2	3-232
TL107-1		MCR106-3	3-232
TL107-2		MCR106-4	3-232
TL107-4		MCR106-6	3-232
TL107-6		MCR106-8	3-232
TL1003		MCR218-3	3-239
TL1006		MCR218-3	3-239
TL2003		MCR218-4	3-239
TL2006		MCR218-4	3-239
TL4003		MCR218-6	3-239
TL4006		MCR218-6	3-239
TL6003		MCR218-8	3-239
TL6006		MCR218-8	3-239
TL8003		MCR218-10	3-239
TL8006		MCR218-10	3-239
TLC111A		T2322B	3-316
TLC111B		T2322B	3-316
TLC113A		T2322B	3-316
TLC113B		T2322B	3-316
TLC221A		T2322B	3-316
TLC221B		T2322D	3-316
TLC223A		T2322B	3-316
TLC223B		T2322B	3-316
TLS106-05		MCR106-2	3-232
TLS106-1		MCR106-3	3-232
TLS106-2		MCR106-4	3-232
TLS106-4		MCR106-6	3-232
TLS106-6		MCR106-8	3-232
TLS107-05		MCR106-2	3-232
TLS107-1		MCR106-3	3-232

5

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
TLS107-2		MCR106-4	3-232
TLS107-4		MCR106-6	3-232
TLS107-6		MCR106-8	3-232
TM507		2N4168	3-27
TM1007		2N4169	3-27
TM2007		2N4170	3-27
TM3007		2N4171	3-27
TM4007		2N4172	3-27
TM5007		2N4173	3-27
TM6007		2N4174	3-27
TRAL1125D		SC260B	3-314
TRAL1135D		T6420B	3-328
TRAL2225D		SC260D	3-314
TRAL2235D		T6420B	3-328
TRAL3835D		T6420N	3-328
TS135		2N3896	3-21
TS235		2N3897	3-21
TS435		2N3898	3-21
TS635		2N3899	3-21
TS835		MCR3935-10	3-268
TY504		MCR218-2	3-239
TY508		MCR218-2	3-239
TY510		2N6394	3-111
TY1004		MCR218-3	3-239
TY1008		MCR218-3	3-239
TY1010		2N6395	3-111
TY2004		MCR218-4	3-239
TY2008		MCR218-4	3-239
TY2010		2N6396	3-111
TY3004		MCR218-6	3-239
TY3008		MCR218-6	3-239
TY3010		MCR220-6	—
TY4004		MCR218-6	3-239
TY4008		MCR218-6	3-239
TY4010		2N6397	3-111
TY5004		MCR218-8	3-239
TY5008		MCR218-8	3-239
TY5010		2N6398	3-111
TY6004		MCR218-8	3-239
TY6008		MCR218-8	3-239
TY6010		2N6398	3-111
TY8008		MCR218-10	3-239
TY8010		2N6398	3-111
TYAL-118B		MAC218A4	3-169
TYAL-118M		T2802B	3-322
TYAL-228B		MAC218A6	3-169
TYAL-228C		T2800B	3-322
TYAL-228M		T2802D	3-322
TYAL-388B		MAC218A10	3-169
TYAL1110B		SC146B	3-309
TYAL1110M		SC146B	3-309
TYAL1115B		MAC15A4	3-138
TYAL1115M		MAC15A4	3-138
TYAL2210B		SC146D	3-309
TYAL2210M		SC146D	3-309
TYAL2215B		MAC15A6	3-138
TYAL2215M		MAC15A6	3-138
TYAL3810B		SC146N	3-309
TYAL3810M		SC146N	3-309
TYAL3815B		MAC15A10	3-138
TYAL3815M		MAC15A10	3-138

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #

5

1 Theory and Applications (Chapters 1 thru 9)

2 Selector Guide

3 Data Sheets

4 Outline Dimensions and Leadform Options

5 Index and Cross Reference

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